REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Z. Editorial changes throughout. - tvn	98-12-10	Monica L. Poelking

REV	A																		
SHEET	35																		
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Monica L. Poelking

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
98-05-18

REVISION LEVEL
A

MICROCIRCUIT, DIGITAL, CMOS, RADIATION HARDENED MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-98552

SHEET 1 OF 35

DSCC FORM 2233
APR 97

5962-E074-99

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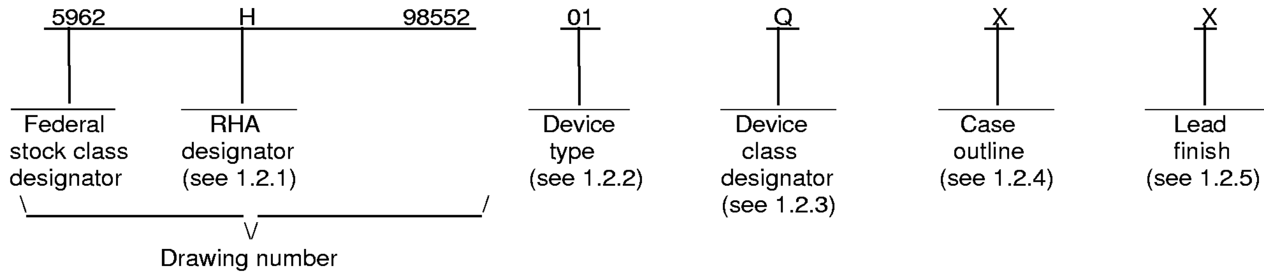
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT69R000-12 MHz	Radiation hardened microcontroller, 12-MHz operating frequency
02	UT69R000-16 MHz	Radiation hardened microcontroller, 16-MHz operating frequency

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA7-P145	145 1/	Pin grid array
Y	CQCC1-F132	132	Flat pack, unformed leads
Z	See figure 1	132	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Pin D4 is an index pin.

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1.3 Absolute maximum ratings. 1/

DC supply voltage (V_{DD}) .... -0.3 V to +7.0 V
Voltage on any pin ($V_{I/O}$) .... -0.3 V to V_{DD} +0.3 V
DC input current (I_I) .... ±10 mA
Storage temperature (T_{STG}) .... -65°C to +150°C
Latchup immunity (I_{LU}) .... ±150 mA 2/
Maximum power dissipation (P_D) .... 600 mW
Maximum junction temperature (T_J) .... +175°C
Thermal resistance, junction-to-case (θ_{JC}) .... 10°C/W 2/

1.4 Recommended operating conditions.

DC supply voltage (V_{DD})........................ 4.5 V to 5.5 V
Temperature range (T_C) .... -55°C to +125°C
DC input voltage (V_{IN}) .... 0 V to V_{DD}
Radiation features:
Total dose........................ $\geq 1 \times 10^6$ Rads (Si)
Single event phenomenon (SEP) effective
linear energy threshold, no upsets or latchup (see 4.4.4.4) .... 55 MeV/(mg/cm^2)
Dose rate upset (20 ns pulse)........................ 3/
Dose rate latchup........................ 3/
Dose rate survivability........................ 3/
Neutron irradiation .... $> 1 \times 10^{14}$ neutron/cm^2

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) .... 83.7 percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Test per MIL-STD-883, method 1012.
3/ When characterized as a result of the procuring activities request, the condition will be specified.

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HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as pecified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure connections. The radiation exposure connections shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

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3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE IA. Electrical performance characteristics.

Test	Symbol 1/	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Low level input voltage, TTL inputs 3/	V_{IL1}		1, 2, 3	All		0.8	V
Low level input voltage, OSC inputs 3/	V_{IL2}					1.2	
High level input voltage, TTL inputs 3/ 4/	V_{IH1}		1, 2, 3	All	2.0		V
High level input voltage, OSC inputs 3/	V_{IH2}				3.6		
High level output voltage, TTL outputs	V_{OH1}	I_{OH} = -400 µA	1, 2, 3	All	2.4		V
		I_{OH} = -800 µA 5/			2.4		
High level output voltage, OSC outputs	V_{OH2}	I_{OH} = -100 µA	1, 2, 3	All	3.5		
Low level output voltage, TTL outputs	V_{OL1}	I_{OL} = 3.2 mA	1, 2, 3	All		0.4	V
		I_{OL} = 6.4 mA 5/				0.4	
Low level output voltage, OSC outputs	V_{OL2}	I_{OL} = 100 µA	1, 2, 3	All		1.0	
Input leakage current, inputs without resistors	I_{IN1}	$V_{IN} = V_{DD}$ or V_{SS}	1, 2, 3	All	-10	10	µA
Input leakage current, inputs with pull-up resistors	I_{IN2}	$V_{IN} = V_{SS}$			-900	-80	
Input leakage current, inputs with pull-down resistors	I_{IN3}	$V_{IN} = V_{DD}$			80	900	
Three-state output leakage current	I_{OZ}	$V_O = V_{DD}$ or V_{SS}	1, 2, 3	All	-10	+10	µA
					-20 5/	+20 5/	
Short circuit output current 6/ 7/	I_{OS}	V_{DD} = 5.5 V, V_O = 0 V to V_{DD}	1, 2, 3	All	-100	100	mA
		V_{DD} = 5.5 V, V_O = 0 V			-200 5/	200 5/	
Average operating current 6/ 8/	I_{DD}	f = 12 MHz, C_L = 50 pF	1, 2, 3	All		50	mA
		f = 16 MHz, C_L = 50 pF				75	
Quiescent current 9/	QI_{DD}		1, 2, 3	All		1	mA
Input capacitance	C_{IN}	f = 1 MHz at 0 V See 4.4.1c	4	All		10	pF
Output capacitance	C_{OUT}		4	All		15	pF
Bidirect I/O capacitance	$C_{I/O}$		4	All		20	pF
Functional tests 3/		See 4.4.1b	7, 8	All			

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol 1/	Test conditions 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
I/O READ CYCLE							
OSCIN low to $\overline{STATE1}$ high	t34a*	See figure 4	9, 10, 11	01	0	42	ns
				02	0	33	
OSCIN low to $\overline{STATE1}$ low	t34b*		9, 10, 11	01	0	39	
				02	0	33	
OSCIN low to $\overline{DS}$ inactive	t34f*		9, 10, 11	01	0	54	
				02	0	45	
OSCIN low to $\overline{DS}$ active	t34g*		9, 10, 11	01	0	37	
				02	0	35	
OSCIN high to $\overline{DS}$ inactive	t34h*		9, 10, 11	01	0	50	
				02	0	38	
OSCIN low to $\overline{DS}$ high Z	t34i		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to R/$\overline{WR}$ active	t34j*		9, 10, 11	01	0	54	
				02	0	41	
OSCIN low to R/$\overline{WR}$ high Z	t34k		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to M/$\overline{IO}$ low	t34l*		9, 10, 11	01	0	51	
				02	0	42	
OSCIN high to M/$\overline{IO}$ HIGH	t34m*		9, 10, 11	01	0	73	
				02	0	55	
OSCIN low to M/$\overline{IO}$ high Z	t34n		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to address valid	t34r*		9, 10, 11	01	0	57	
				02	0	45	
OSCIN high to address invalid	t34s		9, 10, 11	01	---	55	
				02	---	41	
Data setup time	t34t		9, 10, 11	01	0	---	
				02	0	---	
Data hold time	t34u		9, 10, 11	01	34	---	
				02	26	---	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol 1/	Test conditions 2/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
I/O WRITE CYCLE							
OSCIN low to $\overline{STATE1}$ high	t35a*	See figure 4	9, 10, 11	01	0	42	ns
				02	0	33	
OSCIN low to $\overline{STATE1}$ low	t35b*		9, 10, 11	01	0	39	
				02	0	33	
OSCIN low to $\overline{DS}$ inactive	t35f*		9, 10, 11	01	0	54	
				02	0	45	
OSCIN low to $\overline{DS}$ active	t35g*		9, 10, 11	01	0	37	
				02	0	35	
OSCIN high to $\overline{DS}$ inactive	t35h*		9, 10, 11	01	0	50	
				02	0	38	
OSCIN low to $\overline{DS}$ high Z	t35i		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to R/$\overline{WR}$ inactive	t35j*		9, 10, 11	01	0	51	
				02	0	42	
OSCIN low to R/$\overline{WR}$ high Z	t35k		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to M/$\overline{IO}$ low	t35l*		9, 10, 11	01	0	51	
				02	0	42	
OSCIN high to M/$\overline{IO}$ high	t35m*		9, 10, 11	01	0	73	
				02	0	55	
OSCIN low to M/$\overline{IO}$ high Z	t35n		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to address valid	t35r*		9, 10, 11	01	0	57	
				02	0	45	
OSCIN high to address invalid	t35s		9, 10, 11	01	---	55	
				02	---	41	
OSCIN low to data valid	t35t*		9, 10, 11	01	0	64	
				02	0	48	
OSCIN high to data invalid (high Z)	t35u		9, 10, 11	01	---	80	
				02	---	60	
OSCIN high to R/$\overline{WR}$ high	t35v*		9, 10, 11	01	0	72	
				02	0	54	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol 1/	Test conditions 2/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
OPERAND PORT READ CYCLE							
OSCIN low to $\overline{\text{STATE1}}$ high	t36a*	See figure 4	9, 10, 11	01	0	42	ns
				02	0	33	
OSCIN low to $\overline{\text{STATE1}}$ low	t36b*		9, 10, 11	01	0	39	
				02	0	33	
OSCIN low to $\overline{\text{DS}}$ inactive	t36f*		9, 10, 11	01	0	54	
				02	0	45	
OSCIN low to $\overline{\text{DS}}$ active	t36g*		9, 10, 11	01	0	37	
				02	0	35	
OSCIN high to $\overline{\text{DS}}$ inactive	t36h*		9, 10, 11	01	0	50	
				02	0	38	
OSCIN low to $\overline{\text{DS}}$ high Z	t36i		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to R/$\overline{\text{WR}}$ inactive	t36j*		9, 10, 11	01	0	54	
				02	0	42	
OSCIN low to R/$\overline{\text{WR}}$ high Z	t36k		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to M/$\overline{\text{IO}}$ high	t36l*		9, 10, 11	01	0	53	
				02	0	42	
OSCIN low to M/$\overline{\text{IO}}$ high Z	t36n		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to address valid	t36r*		9, 10, 11	01	0	57	
				02	0	45	
OSCIN high to address invalid	t36s		9, 10, 11	01	---	55	
				02	---	41	
Data setup time	t36t		9, 10, 11	01	0	---	
				02	0	---	
Data hold time	t36u		9, 10, 11	01	34	---	
				02	26	---	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol 1/	Test conditions 2/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
OPERAND PORT WRITE CYCLE							
OSCIN low to $\overline{\text{STATE1}}$ high	t37a*	See figure 4	9, 10, 11	01	0	42	ns
				02	0	33	
OSCIN low to $\overline{\text{STATE1}}$ low	t37b*		9, 10, 11	01	0	39	
				02	0	33	
OSCIN low to $\overline{\text{DS}}$ inactive	t37f*		9, 10, 11	01	0	54	
				02	0	45	
OSCIN low to $\overline{\text{DS}}$ active	t37g*		9, 10, 11	01	0	37	
				02	0	35	
OSCIN high to $\overline{\text{DS}}$ inactive	t37h*		9, 10, 11	01	0	50	
				02	0	38	
OSCIN low to $\overline{\text{DS}}$ high Z	t37i		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to R/$\overline{\text{WR}}$ active	t37j*		9, 10, 11	01	0	51	
				02	0	42	
OSCIN low to R/$\overline{\text{WR}}$ high Z	t37k		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to M/$\overline{\text{IO}}$ high	t37l*		9, 10, 11	01	0	53	
				02	0	42	
OSCIN low to M/$\overline{\text{IO}}$ high Z	t37n		9, 10, 11	01	---	50	
				02	---	38	
OSCIN low to address valid	t37r*		9, 10, 11	01	0	57	
				02	0	45	
OSCIN high to address invalid	t37s		9, 10, 11	01	---	55	
				02	---	41	
OSCIN low to data valid	t37t*		9, 10, 11	01	0	64	
				02	0	48	
OSCIN high to data invalid (high Z)	t37u		9, 10, 11	01	---	80	
				02	---	60	
OSCIN high to R/$\overline{\text{WR}}$ high	t37v*		9, 10, 11	01	0	72	
				02	0	54	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol 1/	Test conditions 2/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DMA NO WAIT STATE							
OSCIN low to $\overline{STATE1}$ high	t38a*	See figure 4	9, 10, 11	01	0	42	ns
				02	0	33	
OSCIN low to $\overline{STATE1}$ low	t38b*		9, 10, 11	01	0	39	
				02	0	33	
OSCIN high to $\overline{BRQ}$ low	t38c*		9, 10, 11	01	0	54	
				02	0	41	
OSCIN low to $\overline{BRQ}$ high	t38d*		9, 10, 11	01	0	58	
				02	0	44	
$\overline{BGNT}$ setup time	t38e		9, 10, 11	01	15	---	
				02	15	---	
$\overline{BGNT}$ hold time	t38f		9, 10, 11	01	0	---	
				02	0	---	
OSCIN low to $\overline{BGACK}$ active	t38g*		9, 10, 11	01	0	53	
				02	0	42	
OSCIN low to $\overline{BGACK}$ high Z	t38h		9, 10, 11	01	---	55	
				02	---	41	
$\overline{DTACK}$ setup time	t38i		9, 10, 11	01	10	---	
				02	10	---	
$\overline{DTACK}$ hold time	t38j		9, 10, 11	01	0	---	
				02	0	---	
$\overline{BUSY}$ setup time	t38k		9, 10, 11	01	15	---	
				02	10	---	
$\overline{BUSY}$ hold time	t38l		9, 10, 11	01	10	---	
				02	10	---	
STRI COMMAND TIMING							
OSCIN low to $\overline{STATE1}$ low	t39a*	See figure 4	9, 10, 11	01	0	39	ns
				02	0	33	
OSCIN low to $\overline{STATE1}$ high	t39b*		9, 10, 11	01	0	42	
				02	0	33	
OSCIN high to $\overline{OE}$ high	t39c*		9, 10, 11	01	0	52	
				02	0	39	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol 1/	Test conditions 2/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
STRI COMMAND TIMING – Continued							
OSCIN low to $\overline{OE}$ low	t39d*	See figure 4	9, 10, 11	01	0	46	ns
				02	0	37	
OSCIN high to $\overline{WE}$ low	t39e*		9, 10, 11	01	0	50	
				02	0	40	
OSCIN high to $\overline{WE}$ high	t39f*		9, 10, 11	01	0	49	
				02	0	37	
OSCIN low to address valid	t39g*		9, 10, 11	01	0	65	
				02	0	49	
OSCIN low to address high Z	t39h		9, 10, 11	01	---	50	
				02	---	38	
OSCIN high to data valid	t39i		9, 10, 11	01	---	55	
				02	---	41	
OSCIN low to data high Z	t39j		9, 10, 11	01	---	52	
				02	---	39	
LRI COMMAND TIMING							
OSCIN low to $\overline{STATE1}$ low	t40a*	See figure 4	9, 10, 11	01	0	39	ns
				02	0	33	
OSCIN low to $\overline{STATE1}$ high	t40b*		9, 10, 11	01	0	42	
				02	0	33	
OSCIN high to $\overline{OE}$ low	t40c		9, 10, 11	01	0	46	
				02	0	35	
OSCIN low to $\overline{OE}$ high	t40d		9, 10, 11	01	0	52	
				02	0	39	
OSCIN high to $\overline{WE}$ high	t40e		9, 10, 11	01	0	49	
				02	0	37	
OSCIN low to $\overline{WE}$ low	t40f		9, 10, 11	01	0	47	
				02	0	35	
OSCIN low to address valid	t40g*		9, 10, 11	01	0	65	
				02	0	49	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol 1/	Test conditions 2/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LRI COMMAND TIMING – Continued							
OSCIN low to address high Z	t40h	See figure 4	9, 10, 11	01	---	50	ns
				02	---	38	
Data setup time	t40i		9, 10, 11	01	0	---	
				02	0	---	
Data hold time	t40j		9, 10, 11	01	27	---	
				02	20	---	
UART AND TIMER A/B TIMCLK TIMING							
TIMCLK low time	t41a	See figure 4	9, 10, 11	01	32	---	ns
				02	24	---	
TIMCLK high time	t41b		9, 10, 11	01	---	50	
				02	---	38	
MASTER RESET TIMING							
$\overline{MRST}$ pulse width	t42a	See figure 4	9, 10, 11	01	83	---	ns
				02	62	---	
MASTER RESET TIMING WHEN $\overline{TEST}$ IS ACTIVE							
$\overline{MRST}$ timing with $\overline{TEST}$ active	t42b	See figure 4	9, 10, 11	01	83	---	ns
				02	62	---	

1/ Those test symbols marked with asterisks (*) will be guaranteed by test.

2/ Devices supplied to this drawing are characterized at all levels M, D, L, R, F, G. and H of irradiation. However, this device only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

3/ Functional test shall be conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$ (min) +20%, -0%; $V_{IL} = V_{IL}$ (max) +0%, -50% as specified herein, for TTL or CMOS compatiable inputs. Devices may be tested using any input voltage within the above specified range, but shall be guaranteed to V_{IH} (min) and V_{IL} (max).

4/ Radiation hardened technology shall have a V_{IH} pre-irradiation of 2.2 V.

5/ Double buffer output pins (i.e. $\overline{DS}$, R/$\overline{WR}$, M/$\overline{IO}$).

6/ Guaranteed to the limit specified in table IA, if not tested.

7/ Not more than one output may be shorted at a time for a maximum duration of one second.

8/ Includes current through input pull-ups. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.

9/ All inputs with internal pull-ups or pull-downs should be left open circuit, all other inputs tied low or high. $\overline{TEST}$ input pin asserted.

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TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	T_A = Temperature ±10°C 4/	V_{DD} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET 4/
		Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section (LET = 80) (cm^2)	
All	+25°C	= 55	6.7 x 10^{-5}	> 80

1/ Devices that contain cross coupled resistance must be tested at the maximum rated T_A. For SEP test conditions, see 4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line. Test plan must be approved by TRB and qualifying activity.

3/ Values will be added when they become available. Rad hard devices have not yet been tested for SEP.

4/ Worst case temperature T_A = +125°C.

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Case Z

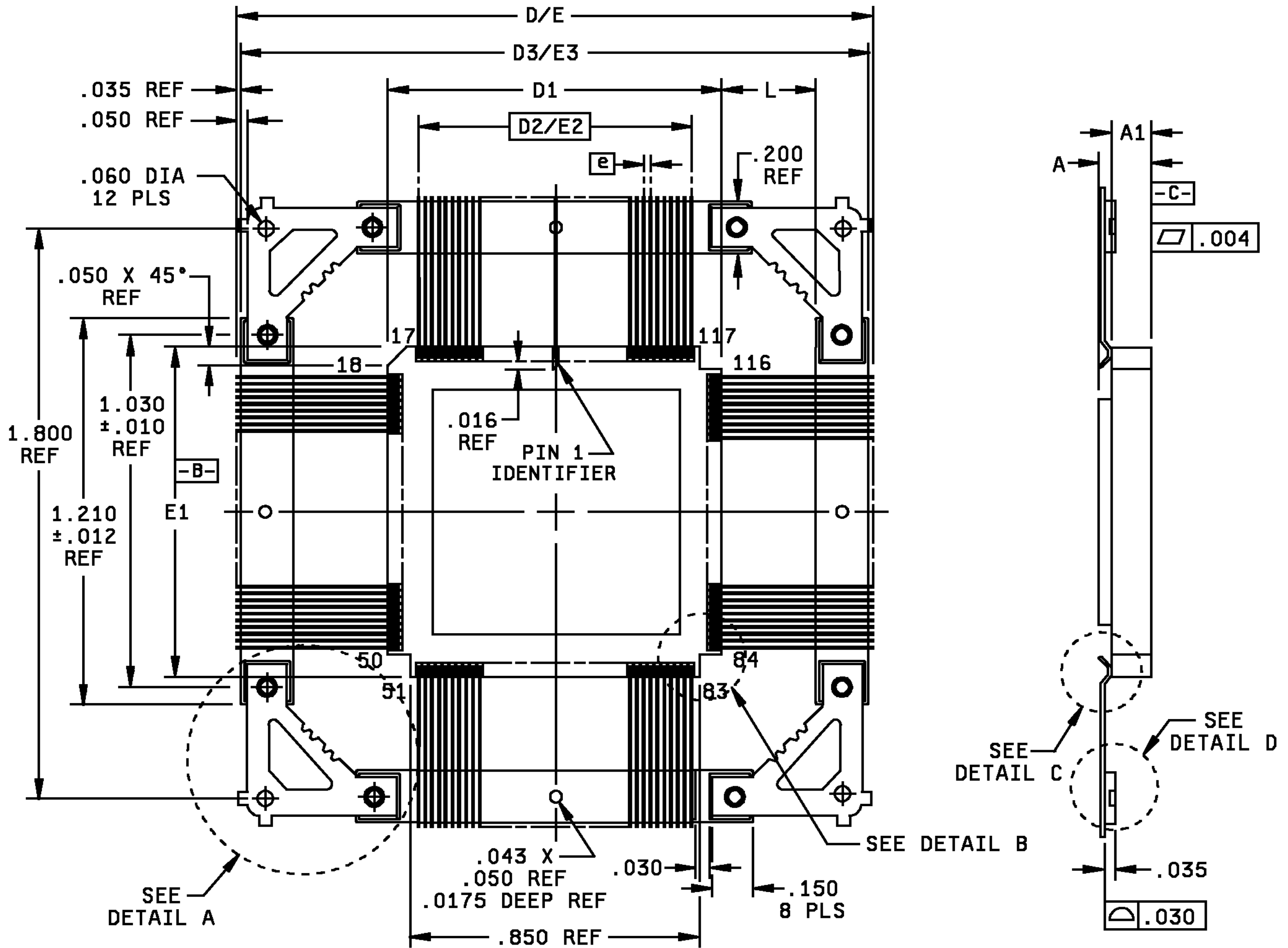

FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-98552
		REVISION LEVEL A	SHEET 15

DSCC FORM 2234
APR 97

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Case Z

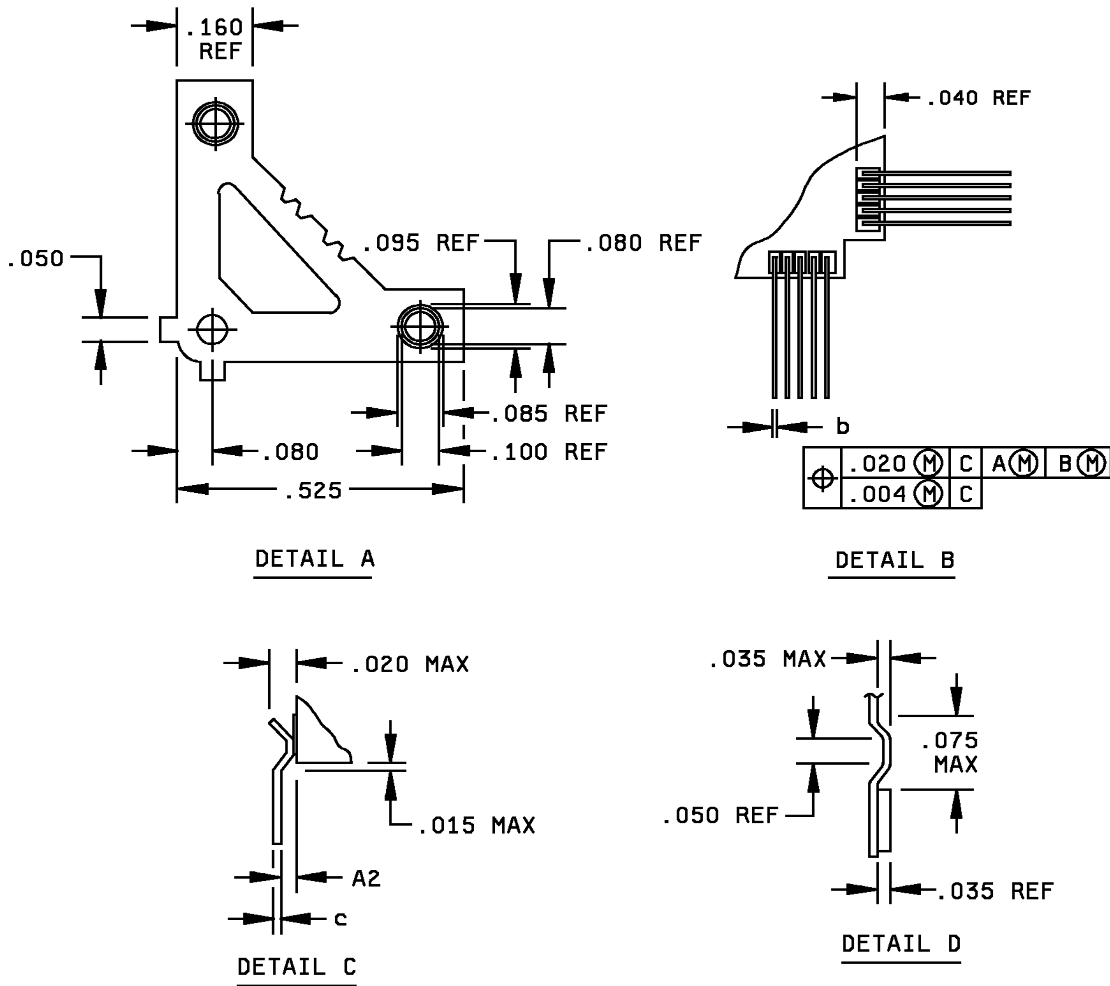

FIGURE 1. Case outline - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-98552
		REVISION LEVEL A	SHEET 16

DSCC FORM 2234
APR 97

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Case Z

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		.150		3.810
A1		.130		3.302
A2	.005	.011	0.127	0.279
b	.009	.013	0.229	0.330
c	.0035	.0075	0.089	0.191
D/E		2.070		52.578
D1/E1	.94	.96	23.876	24.384
D2/E2	.800 BSC		20.320 BSC	
D3/E3	1.990	2.010	50.546	51.054
e	.025 BSC		0.635 BSC	
L	.290		7.366	

NOTES:

1. All exposed metalized area must be gold plated 100 to 225 microinches thick over electroplated nickel undercoating 100 to 359 microinches thick.
2. All V_{DD} pads are connected to the V_{DD} (power) plane which is connected to external leads 34, 67, 100, and 132.
3. All V_{SS} pads are connected to the V_{SS} (ground) plane which is connected to external leads 1, 33, 66, 99, and the seal ring.
4. The die-attach pad must be electrically connected to the power plane.

FIGURE 1. Case outline - Continued.

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Device type	All								
Case outline	X								
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	NC	B15	D12	F1	UARTIN	K15	NUI4	P2	RD15
A2	NUO1	C1	$\overline{\text{BUSY}}$	F2	MCHNE2	L1	RD6	P3	NC
A3	OD5	C2	NC	F3	MPROT	L2	NC	P4	RA1
A4	OD4	C3	NUO2	F13	D5	L3	RD10	P5	RA4
A5	OD3	C4	R/$\overline{\text{WR}}$	F14	D4	L13	TIMCLK	P6	RA7
A6	A15	C5	OD7	F15	D2	L14	$\overline{\text{PFAIL}}$	P7	RA8
A7	A14	C6	OD2	G1	UARTOUT	L15	NC	P8	RA12
A8	A13	C7	V_{DD}	G2	MCHNE1	M1	RD7	P9	RA16
A9	A11	C8	V_{SS}	G3	NUO3	M2	RD9	P10	RA17
A10	A10	C9	A9	G13	V_{DD}	M3	RD13	P11	NC
A11	NC	C10	A6	G14	D3	M13	NC	P12	NUI2
A12	A5	C11	A2	G15	D1	M14	SYSCLK	P13	$\overline{\text{TEST}}$
A13	A3	C12	NC	H1	RD0	M15	$\overline{\text{INT0}}$	P14	OSCIN
A14	A0	C13	D14	H2	NUI1	N1	RD8	P15	OSCOUT
A15	NC	C14	D11	H3	V_{DD}	N2	RD11	R1	NC
B1	$\overline{\text{BGACK}}$	C15	D8	H13	V_{SS}	N3	RD14	R2	RA0
B2	$\overline{\text{DS}}$	D1	$\overline{\text{BTERR}}$	H14	$\overline{\text{INT6}}$	N4	NC	R3	RA3
B3	M/$\overline{\text{IO}}$	D2	$\overline{\text{BRQ}}$	H15	D0	N5	RA2	R4	RA5
B4	OD6	D3	NC	J1	RD1	N6	RA6	R5	NC
B5	NC	D4	INDEX PIN	J2	RD3	N7	RA9	R6	RA10
B6	OD1	D13	D13	J3	V_{SS}	N8	V_{SS}	R7	RA11
B7	OD0	D14	D9	J13	$\overline{\text{INT4}}$	N9	V_{DD}	R8	RA13
B8	A12	D15	D7	J14	$\overline{\text{INT3}}$	N10	RA18	R9	RA14
B9	A8	E1	NC	J15	$\overline{\text{INT5}}$	N11	NUI3	R10	RA15
B10	A7	E2	$\overline{\text{DTACK}}$	K1	RD2	N12	DI2	R11	RA19
B11	A4	E3	$\overline{\text{BGNT}}$	K2	RD4	N13	DI1	R12	$\overline{\text{OE}}$
B12	A1	E13	D10	K3	RD5	N14	NC	R13	$\overline{\text{WE}}$
B13	NC	E14	NC	K13	$\overline{\text{INT1}}$	N15	$\overline{\text{STATE1}}$	R14	$\overline{\text{MRST}}$
B14	D15	E15	D6	K14	$\overline{\text{INT2}}$	P1	RD12	R15	NC

FIGURE 2. Terminal connections.

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Device type	All								
Case outline	Y, Z								
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{SS}	28	RA10	55	$\overline{PFAIL}$	82	D14	109	OD5
2	NC	29	RA11	56	$\overline{INT0}$	83	D15	110	OD6
3	RD1	30	RA12	57	$\overline{INT1}$	84	A0	111	OD7
4	RD2	31	RA13	58	$\overline{INT2}$	85	A1	112	$M/\overline{IO}$
5	RD3	32	NC	59	$\overline{INT3}$	86	A2	113	NUO1
6	RD4	33	V_{SS}	60	$\overline{INT4}$	87	A3	114	$R/\overline{WR}$
7	RD5	34	V_{DD}	61	NUI4	88	A4	115	NUO2
8	RD6	35	NC	62	$\overline{INT5}$	89	A5	116	$\overline{DS}$
9	RD7	36	RA14	63	$\overline{INT6}$	90	A6	117	$\overline{BGACK}$
10	RD8	37	RA15	64	D0	91	A7	118	$\overline{BRQ}$
11	RD9	38	RA16	65	NC	92	A8	119	$\overline{BGNT}$
12	RD10	39	RA17	66	V_{SS}	93	A9	120	$\overline{BUSY}$
13	RD11	40	RA18	67	V_{DD}	94	A10	121	$\overline{DTACK}$
14	RD12	41	RA19	68	NC	95	A11	122	$\overline{BTERR}$
15	RD13	42	$\overline{OE}$	69	D1	96	A12	123	MPROT
16	RD14	43	$\overline{WE}$	70	D2	97	A13	124	MCHNE2
17	RD15	44	NUI2	71	D3	98	NC	125	MCHNE1
18	RA0	45	NUI3	72	D4	99	V_{SS}	126	NUO3
19	RA1	46	$\overline{TEST}$	73	D5	100	V_{DD}	127	UARTIN
20	RA2	47	$\overline{MRST}$	74	D6	101	NC	128	UARTOUT
21	RA3	48	DI2	75	D7	102	A14	129	NUI1
22	RA4	49	DI1	76	D8	103	A15	130	RD0
23	RA5	50	OSCIN	77	D9	104	OD0	131	NC
24	RA6	51	OSCOUT	78	D10	105	OD1	132	V_{DD}
25	RA7	52	SYSCLK	79	D11	106	OD2		
26	RA8	53	TIMCLK	80	D12	107	OD3		
27	RA9	54	$\overline{STATE1}$	81	D13	108	OD4		

FIGURE 2. Terminal connections - Continued.

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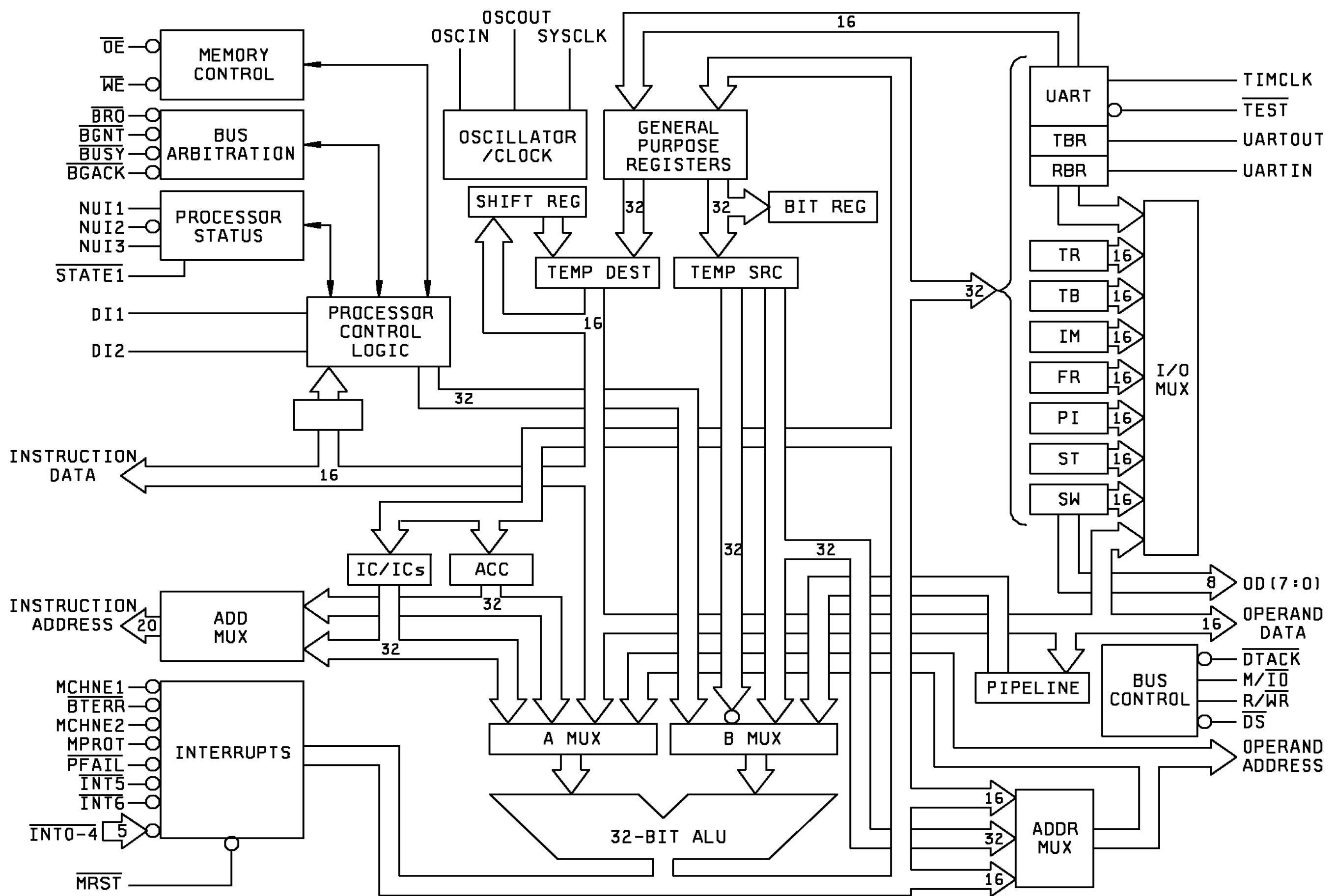

FIGURE 3. Block diagram.

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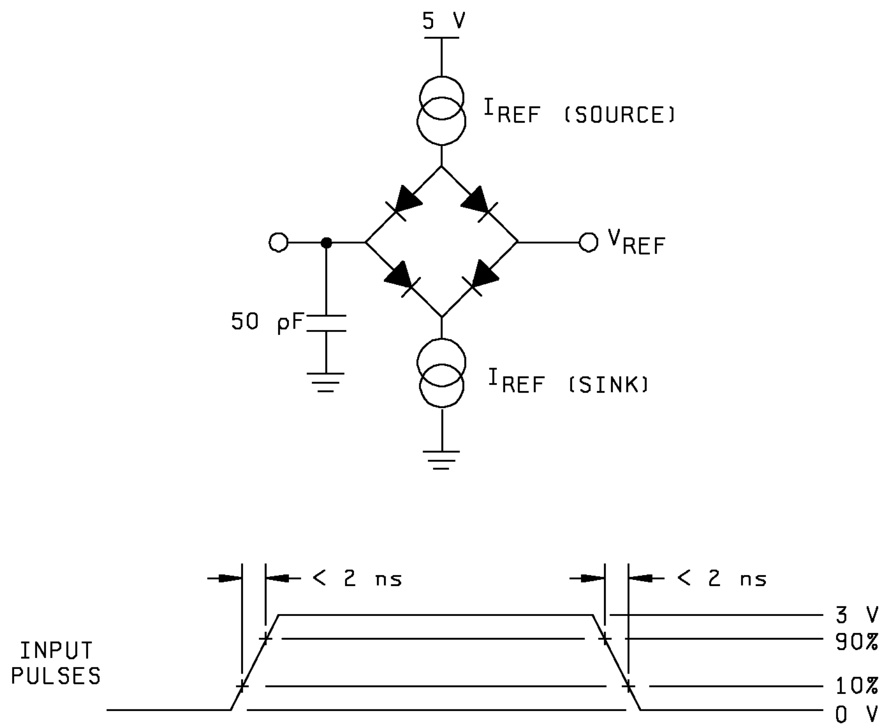

FIGURE 4. Test circuit and timing waveforms.

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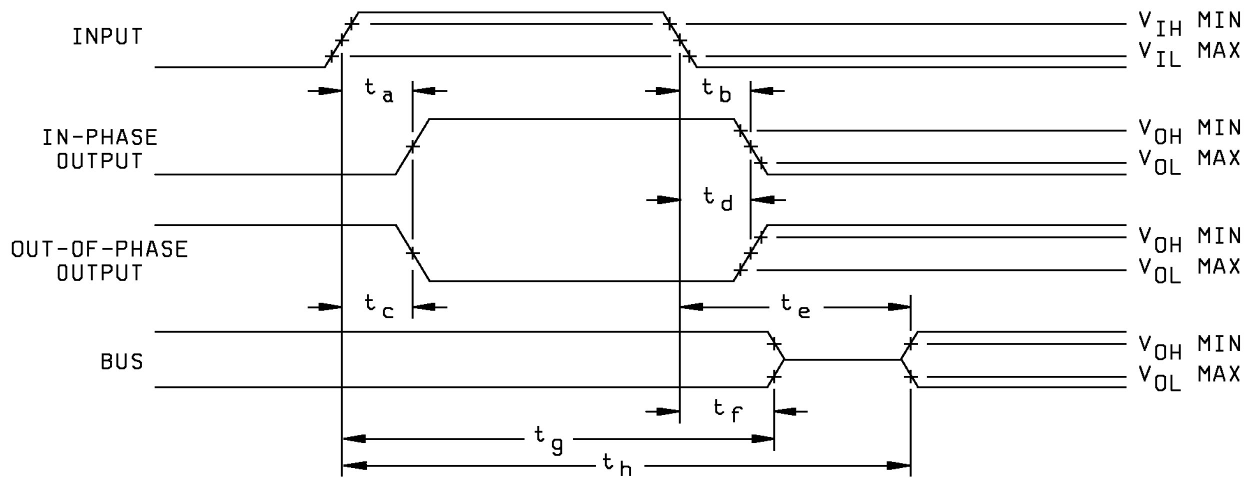

SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

FIGURE 4. Test circuit and timing waveforms - Continued.

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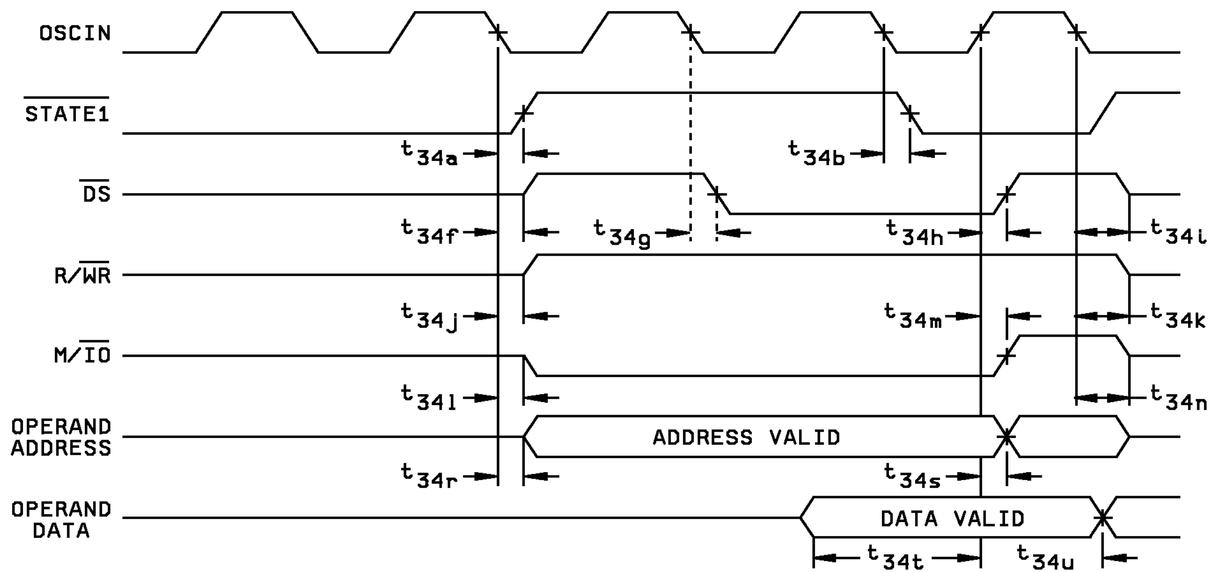

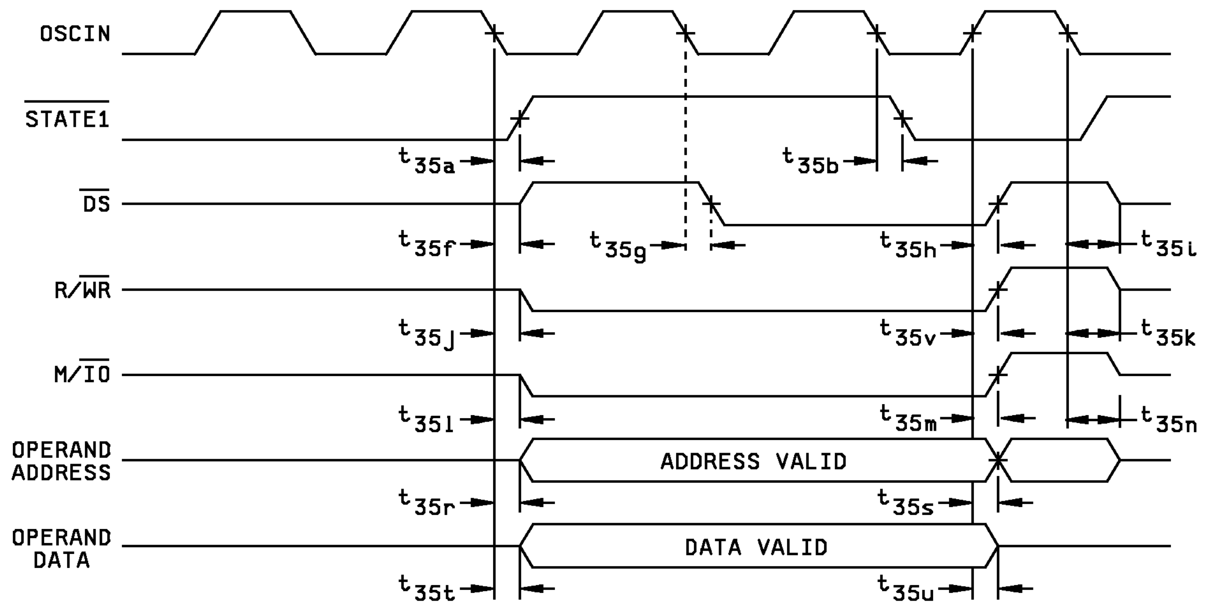

FIGURE 4. Test circuit and timing waveforms - Continued.

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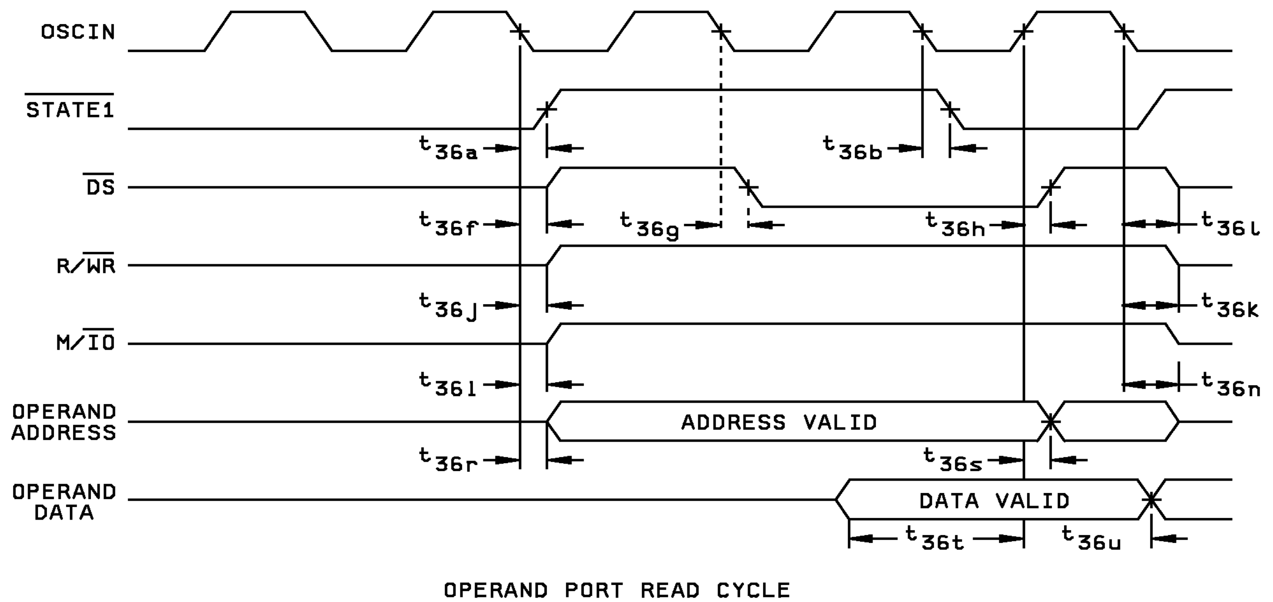

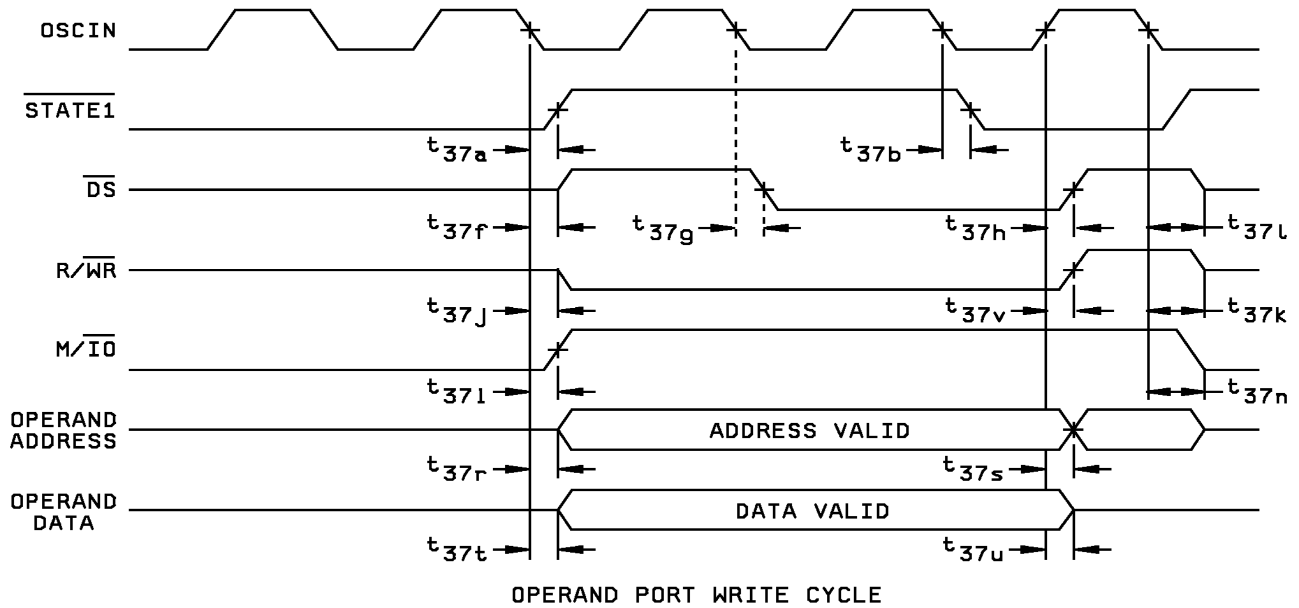

FIGURE 4. Test circuit and timing waveforms - Continued.

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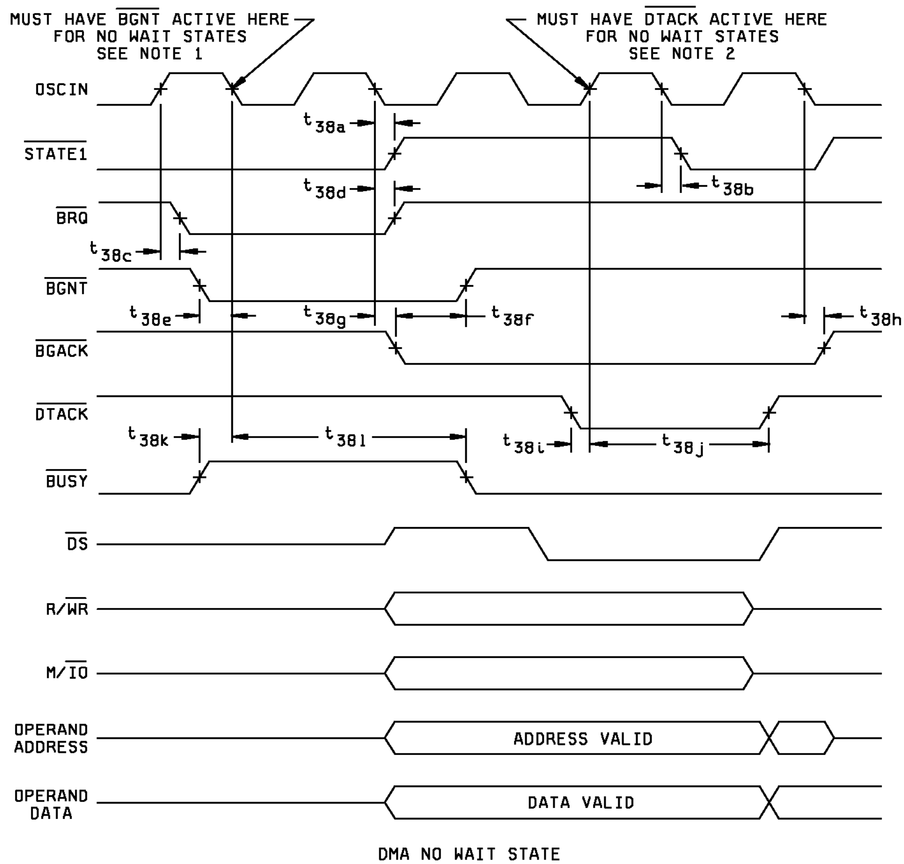

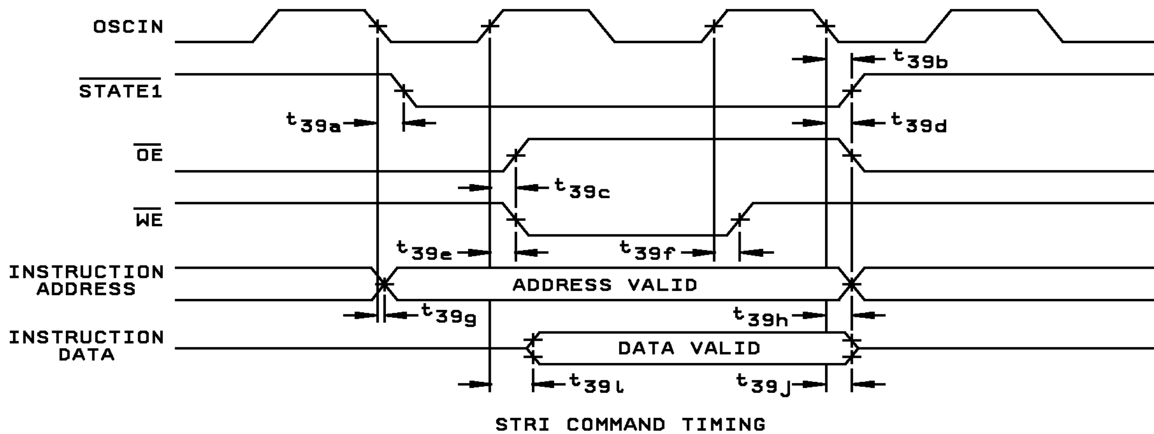

NOTES:

1. BGNT must be active and BUSY high at this clock edge or wait states will occur.
2. To avoid wait states, DTACK must be active here.

FIGURE 4. Test circuit and timing waveforms - Continued.

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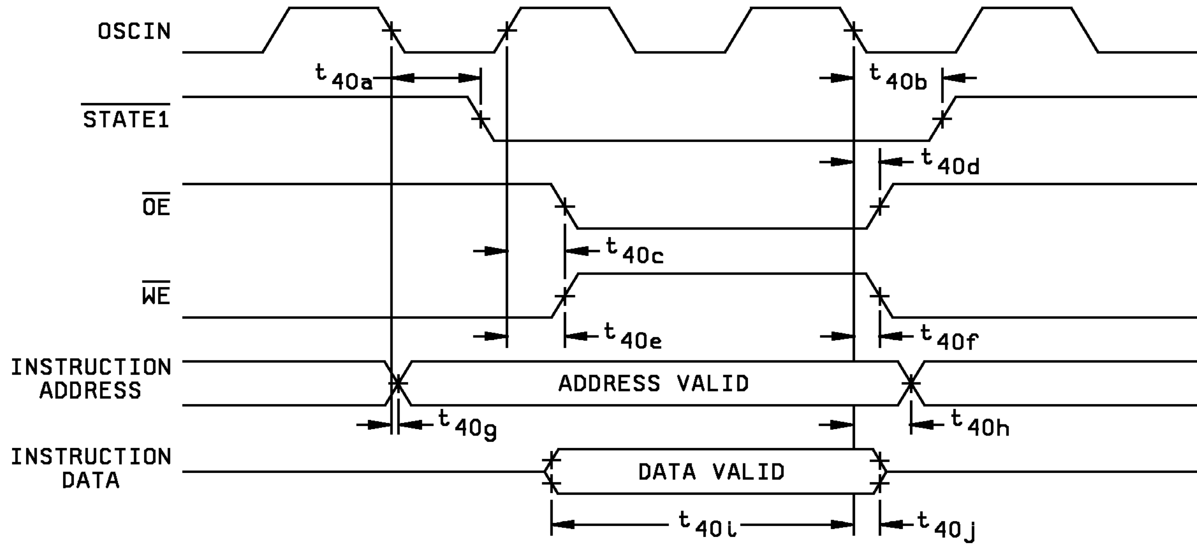
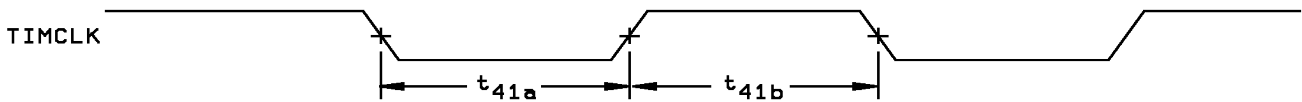
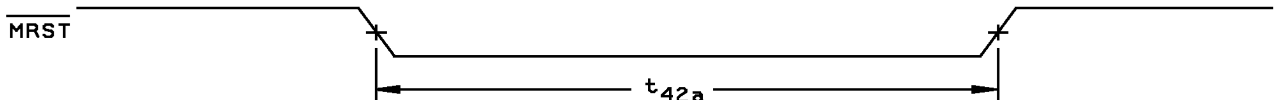


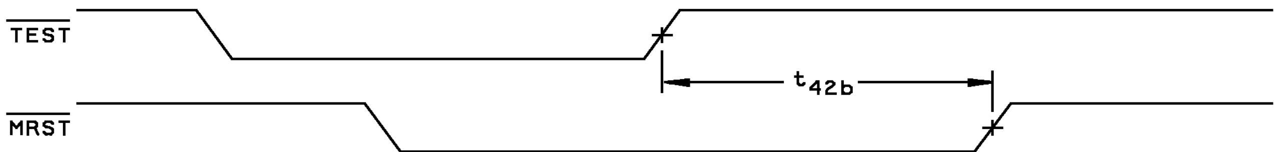
LRI COMMAND TIMING



UART AND TIMER A/B TIMCLK TIMING



MASTER RESET TIMING



MASTER RESET TIMING WHEN TEST IS ACTIVE

FIGURE 4. Test circuit and timing waveforms - Continued.

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Case outline	Open	V_{DD} = 5 V ± 0.5 V	Ground
X	A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, C2, C3, C4, C5, C6, C9, C10, C11, C12, C13, C14, C15, D2, D3, D4, D13, D14, D15, E1, E13, E14, E15, F13, F14, F15, G1, G3, G14, G15, H1, H2, H15, J1, J2, K1, K2, K3, L1, L2, L3, L15, M1, M2, M3, M13, M14, N1, N2, N3, N4, N5, N6, N7, N10, N14, N15, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P15, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R15	C1, C7, D1, F1, F2, G13, H3, H14, J14, K13, K15, L14, N9, N12, P12, P13, P14	C8, E2, E3, F3, G2, H13, J3, J13, J15, K14, L13, M15, N8, N11, N13, R14
Y, Z	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 41, 42, 43, 51, 52, 54, 64, 65, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 126, 128, 129, 130, 131	34, 44, 46, 48, 50, 55, 57, 59, 61, 63, 67, 100, 120, 122, 124, 127, 132	1, 33, 45, 47, 49, 53, 56, 58, 60, 62, 66, 99, 119, 121, 123, 125

Each pin except C7, C8, G13, H3, H13, J3, N8, and N9 (for case outline X) and 1, 33, 34, 66, 67, 99, 100, and 132 (for case outlines Y and Z) will have a resistor of 2.49 kΩ ±5% for irradiation testing.

FIGURE 5. Radiation exposure connections.

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4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25EC " 5EC, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 7, 8	1, 2, 7, 8	1, 2, 7, 8 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 8	1, 2, 7, 8	1, 2, 7, 8
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits, as specified in table IIB herein, shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in delta parameters (+25°C).

Parameter	Symbol	Condition	Limits
Quiescent current	Q_{IDD}	T_A = 25°C	± 10% of measured value or 35 µA whichever is greater

NOTE: If device is tested at or below 35 µA, no deltas are required. Deltas are performed at room temperture.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelarated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accoradance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

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4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accoradance with test method 1021 of MIL-STD883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehice as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upse or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

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6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as shown in table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

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TABLE III. Pin Descriptions.

Pin Name	Active 1/	Type 2/	Description
OSCILLATOR AND CLOCK SIGNALS			
OSCIN	---	OSC	Oscillator Input. A 50% duty cycle crystal-drive input for driving the device.
OSCOUT	---	CO	Oscillator Output. A 50% duty cycle, single-phase clock output at the same frequency as the OSCIN input.
SYSCLK	---	TO	System Output. The buffered equivalent of the OSCOUT signal.
PROCESSOR STATUS			
NUI1	---	TI	Not used input 1. Tie either high or low.
NUI2	---	TUI	Not used input 2. Tie low.
NUI4	---	TUI	Not used input 4. Tie high.
NUI3	---	TDI	Not used input 3. Tie low.
NUO1	---	TTO	Not Used Output 1, for internal use only. Float or leave open circuit.
NUO2	---	TTO	Not Used Output 2, for internal use only. Float or leave open circuit.
NUO3	---	TTO	Not used output 3. NUO3 enter high impedance state when the device is in the test mode ($\overline{\text{TEST}}$ = 0).
$\overline{\text{STATE1}}$	---	TTO	Processor State. This signal indicates the internal state of the device. A low on $\overline{\text{STATE1}}$ indicates the device is executing a new instruction. A high on $\overline{\text{STATE1}}$ indicates the device is fetching an instruction. $\overline{\text{STATE1}}$ enters a high impedance state when the device is in the test mode ($\overline{\text{TEST}}$ = 0).
OPERAND DATA BUS ARBITRATION			
$\overline{\text{BRQ}}$	AL	TTO	Bus Request. The device asserts this signal to indicate it is requesting control of the Operand data bus (D0-D15). $\overline{\text{BRQ}}$ enters a high-impedance state when the device is in the test mode ($\overline{\text{TEST}}$ = 0).
$\overline{\text{BGNT}}$	AL	TUI	Bus Grant. When asserted, this signal indicates the device may take control of the Operand data bus. It is tied to an internal pull-up resistor.
$\overline{\text{BUSY}}$	AL	TUI	Bus Busy. A bus master asserts this input to inform the device that another bus master is using the Operand data bus. It is tied to an internal pull-up resistor.
$\overline{\text{BGACK}}$	AL	TTO	Bus Grant Acknowledge Output. The device asserts this signal to indicate it is the current bus master. When low, $\overline{\text{BGACK}}$ inhibits other devices from becoming the bus master. When the device relinquishes control of the bus, $\overline{\text{BGACK}}$ enters a high-impedance state.

See footnotes at end of table.

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TABLE III. Pin Descriptions - Continued.

Pin Name	Active 1/	Type 2/	Description
OPERAND DATA BUS CONTROL			
$\overline{DTACK}$	AL	TUI	Data Transfer Acknowledge. This signal tells the device that a data transfer has been acknowledged and the device can complete the bus cycle. To assure the device operates with no wait states, $\overline{DTACK}$ can be tied low. $\overline{DTACK}$ is tied to an internal pull-up resistor.
M/$\overline{IO}$	---	TTO	Memory or $\overline{I/O}$. Indicates whether the current bus cycle is for memory (high) or $\overline{I/O}$ (low). It remains in the high-impedance state during bus cycles when the device does not control the Operand buses.
R/$\overline{RW}$	---	TTO	Read /Write. Indicates the direction of data flow with respect to the device. R/$\overline{RW}$ high means the device is attempting to read data from an external device, and R/$\overline{RW}$ low means the device is attempting to write data to an external device. R/$\overline{RW}$ remains in a high-impedance state when the device does not control the Operand buses.
$\overline{DS}$	AL	TTO	Data Strobe. Indicates valid data is on the Operand Data bus. The device places $\overline{DS}$ in a high-impedance state when it does not control the Operand buses.
INSTRUCTION MEMORY CONTROL			
$\overline{OE}$	AL	TTO	Output Enable Instruction Memory. This signal allows memory to place data on the instruction data bus. The Store Register to Instruction Memory (STRI) instruction removes $\overline{OE}$ during the CK2 internal clock cycle. $\overline{OE}$ enters a high-impedance state when the device is in test mode ($\overline{TEST}$ = 0).
$\overline{WE}$	AL	TTO	Write Enable Memory. This signal allows the device to write to instruction memory. The Store Register to Instruction Memory (STRI) instruction assets $\overline{WE}$ during the CK2 internal clock cycle. $\overline{WE}$ enters a high-impedance state when the device is in the test mode ($\overline{TEST}$ = 0).
UART CONTROL/TIMER CLOCK			
UARTIN	AH	TUI	UART Input. The device receives serial data through tihis input. The serial data is stored in the device's Receiver Buffer Register (RCVR). It is tied to an internal pull-up resistor.
UARTOUT	AH	TTO	UART Output. The serial data stored in the device's Transmitter Buffer Register (TXMT) is transmitted through this output. The UART output is fixed at 9600 baud, with eight data bits, odd-parity, and one stop bit. UARTOUT enters a high-impedance state when the device is in the test mode ($\overline{TEST}$ = 0). (9600 baud @ TIMCLK = 12 MHz).
TIMCLK	---	TI	Timer Clock. This 12 MHz clock input generates the baud rate for the device's internal UART. The input also provides the clock for the device's two internal timers (TIMER A and TIMER B).

See footnotes at end of table.

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TABLE III. Pin Descriptions - Continued.

Pin Name	Active 1/	Type 2/	Description
UART CONTROL/TIMER CLOCK – Continued			
DI2	---	TDI	Discrete Input 2. Asserting this input sets bit 3 in the System Status Register, Bit 3 is read with the Input Register Instruction (INR). Tied to an internal pull-down resistor. (asynchronous input).
$\overline{TEST}$	AL	TUI	Test (Input). Asserting this input places the device into a test mode. In this mode, all the device's outputs, except OSCOUT and SYSCLK, enter a high-impedance state. When using $\overline{TEST}$, the device must have a $\overline{MRST}$. $\overline{MRST}$ must be held active for at least one SYSCLK period after $\overline{TEST}$ is deasserted to assure proper operation . $\overline{TEST}$ is tied to an internal pull-up resistor.
DI1	---	TDI	Discrete Input 1. Asserting this input sets bit 8 in the System Status Register. Bit 8 is read with the Input Register Instruction (INR). Tie to a internal pull-down resistor. (asynchronous input).
PROCESSOR MODE			
OD0 - OD7	---	TTO	Output Discrete Bus (OD(7:0)). These outputs reflect the status of bits 0 through 7 of the Status/Output Discrete Register. Write to this register using Output Register Instruction (OTR). Outputs enter a high-impedance state when the device is placed in the test mode ($\overline{TEST}$ = 0).
INTERRUPTS/EXCEPTIONS			
MCHNE1	AH	TUI	System Fault. This positive edge-triggered input sets bit 8 (MCHNE1) in the device's Fault Register. Under no circumstances should MCHNE1 be tied in its active state. It is tied to an internal pull-up resistor. Interrupt is not cleared via software until the negation of the input signal.
$\overline{BTERR}$	AL	TUI	Bus Time Error. It is asserted when a bus error or a timeout occurs. During I/O bus cycles, an active $\overline{BTERR}$ sets bit 10 of the Fault Register. During Memory bus cycles, an active $\overline{BTERR}$ sets bit 7 of the Fault Register. Under no circumstances should $\overline{BTERR}$ be tied in its active state. It is tied to an internal pull-up resistor. Interrupt is not cleared via software until the negation of the input signal
MCHNE2	AH	TDI	Memory Parity (Error). Asserting this input indicates a machine error. Bit 13 of the device's Fault Register is set when MCHNE2 is active. Under no circumstances should MCHNE2 be tied in its active state. It is tied to an internal pull-down resistor. Interrupt is not cleared via software until the negation of the input signal.
MPROT	AH	TUI	Memory Protect Fault. When asserted, it informs the device that a memory-protect fault has occurred on the Operand Data Bus. An access fault, a write-protect fault, or an execute-protect fault causes a memory-protect fault. If the device is using the bus and MPROT is asserted, bit 15 of the Fault Register (CPU Fault) is set. If the device is not using the bus and MPROT is asserted, bit 14 of the Fault Register (DMA Error) is set. It is tied to an internal pull-up resistor. Interrupt is not cleared via software until the negation of the input signal.

See footnotes at end of table.

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TABLE III. Pin Descriptions - Continued.

Pin Name	Active 1/	Type 2/	Description
INTERRUPTS/EXCEPTIONS – Continued			
$\overline{INT0}$ - $\overline{INT6}$	AL	TUI	User Interrupts. These interrupts are active on a negative-going edge and each will set, when active, its associated bit in the Pending Interrupt Register. The interrupts are maskable by setting the associated bits in the Interrupt Mask Register. Asserting $\overline{MRST}$ resets all interrupts. They are tied to an internal pull-up resistor.
$\overline{PFAIL}$	AL	TUI	Power Fail (Interrupt). Asserting this input informs the device that a powere failure has occured and the present process will be interrupted. This input sets bit 15 in the Pending Interrupt Register. A Power Fail Interrupt (bit 15) cannot be disabled or masked. It is tied to an internal pull-up resistor.
$\overline{MRST}$	AL	TUI	Master Reset. This input initializes the device to a reset state. The device must be reset after power (V_{CC}) is within specification and stable to ensure proper operation. The system must hold $\overline{MRST}$ active for at least one period of SYSCLK to assure the device will be reset. It is tied to an internal pull-up resistor.
OPERAND BUSES			
A0 - A15	---	TTO	Address Bus-Operand. When asserted, this bus is unidirectional and represents the Operand Address. The bus is in the high-impedance state when the device does not control the bus. A15 is the most significant bit. The Operand Address enters a high-impedance state when the device is in the test mode ($\overline{TEST}$ = 0).
D0 - D15	---	TTB	Data Bus-Operand. This bidirectional data bus remains in a high-impedance state when the device does not control the bus. D15 is the most significant bit. The Operand Data Bus enters a high-impedance state when the device is in the test mode ($\overline{TEST}$ = 0).
INSTRUCTION BUSES			
RA0 - RA19	---	TTO	Instruction Address Bus. This unidirectional bus represents the address of the data in instruction memory. RA19 is the most significant bit. The address enters a high-impedance state only ehen the device is in the test mode ($\overline{TEST}$ = 0).
RD0 - RD15	---	TTB	Instruction Data Bus. This bidirectional data bus is the interface with the memory. RD15 is the most significant bit. The Data Bus enters a high-impedance state only when the device is in the test mode ($\overline{TEST}$ = 0).
POWER AND GROUND			
V_{DD}	---	---	+5 V DC Power. Power supply input.
V_{SS}	---	---	Reference Ground. Zero Volts DC, logic ground.

1/ AH = Active High; AL = Active Low.

2/ TO = TTL output; TI = TTL input; TUI = TTL input (pull-up); TDI = TTL input (pull-down); TTO = Three-state TTL output; TTB = Three-state TTL bidirectional; CO = CMOS output; OSC = Oscillator input to a Pierce Oscillator inverter.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-12-10

Approved sources of supply for SMD 5962-98552 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9855201QXA	65342	UT69R00012GCA
5962-9855201QXC	65342	UT69R00012GCC
5962-9855201QYC	65342	UT69R00012WCC
5962-9855201QZA	65342	UT69R00012FCA
5962-9855201QZC	65342	UT69R00012FCC
5962H9855201QXA	65342	UT69R00012GCAH
5962H9855201QXC	65342	UT69R00012GCCH
5962H9855201QYC	65342	UT69R00012WCCH
5962H9855201QZA	65342	UT69R00012FCAH
5962H9855201QZC	65342	UT69R00012FCCH
5962H9855201VXA	65342	UT69R00012GCAH
5962H9855201VXC	65342	UT69R00012GCCH
5962H9855201VYC	65342	UT69R00012WCCH
5962-9855201VZA	65342	UT69R00012FCAH
5962-9855201VZC	65342	UT69R00012FCCH
5962-9855202QXA	65342	UT69R00016GCA
5962-9855202QXC	65342	UT69R00016GCC
5962-9855202QYC	65342	UT69R00016WCC
5962-9855202QZA	65342	UT69R00016FCA
5962-9855202QZC	65342	UT69R00016FCC
5962H9855202QXA	65342	UT69R00016GCAH
5962H9855202QXC	65342	UT69R00016GCCH

See footnotes at end of table.

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STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9855202QYC	65342	UT69R00016WCCH
5962H9855202QZA	65342	UT69R00016FCAH
5962H9855202QZC	65342	UT69R00016FCCH
5962H9855202VXA	65342	UT69R00016GCAH
5962H9855202VXC	65342	UT69R00016GCCH
5962H9855202VYC	65342	UT69R00016WCCH
5962H9855202VZA	65342	UT69R00016FCAH
5962H9855202VZC	65342	UT69R00016FCCH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronic Systems Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486

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