Dual High-Voltage Driver

FEATURES

- 33 V Output at ±40 mA
- Variable Input Threshold
- 70 ns Delay Time
- Complementary Outputs

BENEFITS

- Wide Output Swing
- Logic Family Flexibility
- Fast Switching
- Drive Coupler H Bridge Power Circuit

APPLICATIONS

- Analog Multiplexing
- Interface Logic to MOS Power
- Logic Level Translation
- Driver for PIN Diodes and FET Switches
- Line Driver

DESCRIPTION

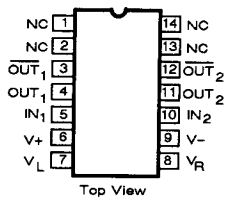
The D169 is a versatile high-voltage dual driver designed with complementary outputs making it excellent for driving capacitive loads. By combining a wide output voltage swing (33 V) with fast switching (100 ns delay) make this device well suited for driving power MOSFET configurations.

A differential input stage with adjustable threshold provides high input impedance and easy interfacing to low level logic or analog inputs. Current-source coupling to the output stage allows flexibility in output voltage levels, while the complementary emitter-follower outputs can source and sink currents of up to ±40 mA. Each channel of the D169 has 2 separate outputs that are complementary (OUT and $\overline{OUT}$) allowing easier driving of MOSPOWER devices. The output can be operated by single or split supplies.

The D169 is especially adept in driving capacitive loads such as power MOSFETS, long cables, timing capacitors, and PIN diodes. Analog mulitplexing is simplified by the wide range of interface logic levels accepted, and wide output voltage swing.

Packaging for this device includes 14-pin side-braze, CerDIP, and plastic DIP options. Performance grades include military, A suffix (–55 to 125°C) and commercial, C suffix (0 to 70°C) temperature ranges.

PIN CONFIGURATION

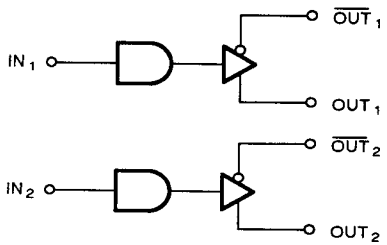


Top View

Order Numbers:

Side Braze: D169AP, D169AP/883
CerDIP: D169AK, D169AK/883
Plastic: D169CJ

FUNCTIONAL BLOCK DIAGRAM



LOGIC	OUT	$\overline{OUT}$
0	V–	V+
1	V+	V–

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

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ABSOLUTE MAXIMUM RATINGS

V+ to V−, V+ to V_R, V+ to V_O ..... 36 V

V_L to V_R, V_{IN} to V_R, and V_L to V_{IN} ..... 10 V

V_R to V−, V_L to V−, and V_O to V− ..... 36 V

Current (Any Terminal) DC ..... 40 mA
Peak (Pulsed 1 ms, 10% Duty Cycle) ..... 150 mA

Operating Temperature (A Suffix) ..... −55 to 125°C
(C Suffix) ..... 0 to 70°C

Storage Temperature (A Suffix) ..... −65 to 150°C
(C Suffix) ..... −65 to 125°C

Power Dissipation*
14-Pin Side braze DIP** ..... 825 mW
14-Pin CerDIP*** ..... 825 mW
14-Pin Plastic DIP**** ..... 470 mW

Thermal Resistance (θ_{JA} , J Package) .... 0.16°C /mW

* All leads soldered or welded to PC board.
** Derate 11 mW/°C above 75°C.
*** Derate 11 mW/°C above 75°C.
**** Derate 6.5 mW /°C above 25°C.

ELECTRICAL CHARACTERISTICS [a]

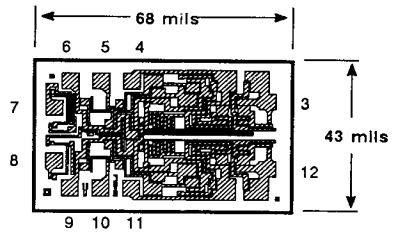
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V_L = 5 V, V− = −15 V, V_R = 0 V		LIMITS 1=25°C 2=125,70°C 3=−55, 0°C TEMP	TYP [c]	A SUFFIX −55 to 125°C MIN [b]	A SUFFIX −55 to 125°C MAX [b]	C SUFFIX 0 TO 70°C MIN [b]	C SUFFIX 0 TO 70°C MAX [b]	UNIT
OUTPUT										
Output Voltage HIGH (V_+ to V_O)	$V_{OH}/V_{\overline{OH}}$	V_{IH} = 2.0 V or V_{IL} = 0.8	I_{OUT} = 1 mA	1,2 3	0.7		1 1.1		1 1.1	V
			I_{OUT} = 40 mA	1,3 2	1.5		2.5 3.1		2.5 3.1	
Output Voltage LOW (V_O to V−)	$V_{OL}/V_{\overline{OL}}$		I_{OUT} = 1 mA	1,2,3	−0.75	−1.2		−1.2		
			I_{OUT} = 40 mA	1,3 2	−2.2	−3 −4		−3 −4		
INPUT										
Input Current Voltage HIGH	I_{INH}	V_{IN} = 3 V		1 2	1		5 5000		5 5000	nA
Input Current Voltage LOW	I_{INL}	V_{IN} = 0 V		1,2 3	−25	−50 −100		−50 −100		µA
DYNAMIC										
Switching Time Low to High, Delay Plus Rise Time	$t_{(+)}$	See Switching Time Test Circuit (C_L = 35 pF)		1	80		170		170	ns
Switching Time High to Low, Delay Plus Fall Time	$t_{(-)}$			1	90		200		200	

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V_L = 5 V, V− = −15 V, V_R = 0 V	LIMITS 1=25°C 2=125,70°C 3=−55, 0 °C TEMP	TYP [c]	A SUFFIX −55 to 125°C MIN [b]	A SUFFIX −55 to 125°C MAX [b]	C SUFFIX 0 TO 70°C MIN [b]	C SUFFIX 0 TO 70°C MAX [b]	UNIT
SUPPLY									
Switching Crossover Level	V_{XO}	C_L = 200 pF	1	0.9					V
Positive Supply Current	I+	$V_{IN1} = V_{IN2}$ = 0 V, No Load	1			0.1		0.1	mA
Logic Supply Current	I_L		1	3.2		4		4	
Negative Supply Current	I−		1	−2.2	−3.0		−3.0		
Reference Supply Current	I_R		1	1.0		1.5		1.5	

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

DIE TOPOGRAPHY



20X

CMOB
4 Diodes
4 Capacitors
7 Resistors
4 P-Channel Enhancement MOSFE¯s
10 PNP Bipolar Transistors
8 NPN Bipolar Transistors

Pad No.	Function
3	$\overline{OUT}_1$
4	OUT_1
5	IN_1
6	V+
7	V_L
8	V_R
9	V− (Substrate)
10	IN_2
11	OUT_2
12	$\overline{OUT}_2$

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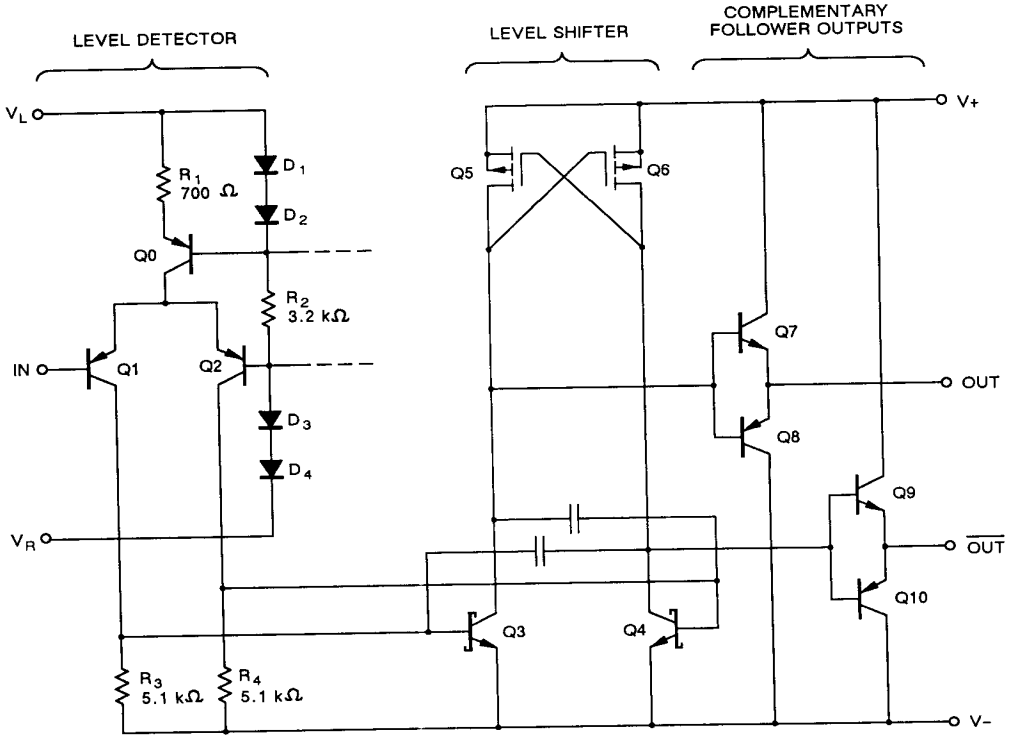
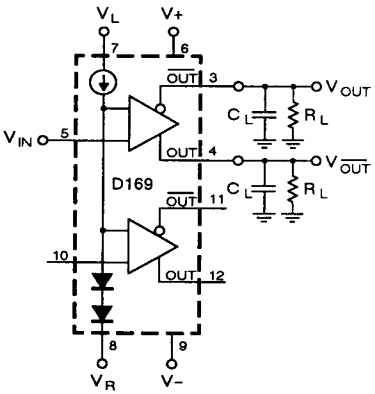
SCHEMATIC DIAGRAM (One Channel)



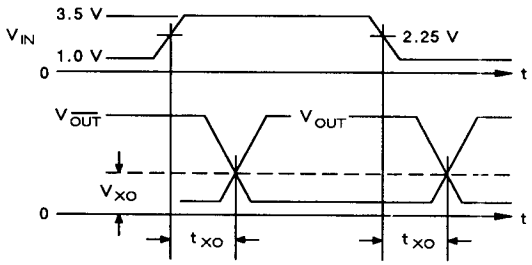
SWITCHING TIME TEST CIRCUITS

TEST #	V_L	V_R	V+	V-	C_L	R_L	V_{IN}		WAVE-FORMS
							V_{IL}	V_{IH}	
1	5 V	0.7 V	10 V	0	200 pF	–	1 V	3.5 V	A
2	5 V	0.7 V	15 V	0	0	510 Ω	1 V	3.5 V	B
3	5 V	0.7 V	10 V	0	200 pF	–	1 V	3.5 V	B
4	5 V	0.7 V	10 V	0	1000 pF	–	1 V	3.5 V	B
5	5 V	0	15 V	-15 V	200 pF	–	0	3.5 V	B
6	5 V	0	15 V	-15 V	1000 pF	–	0	3.5 V	B

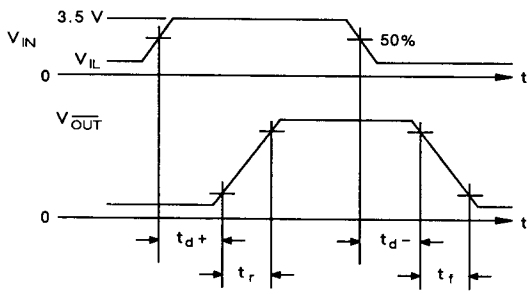
Test Conditions



Test Circuit



Waveforms A



Waveforms B

Parameter	Test 2	Tests 5 & 6		Tests 3 & 4		Units
		V+ = 15 V, V- = -15 V		V+ = 15 V, V- = 0 V		
		Capacitive Load		Capacitive Load		
	Resistive I_O = 25 mA	200 pF	1000 pF	200 pF	1000 pF	
Low-to-High						
Delay Time, t_{D+}	70	95	220	110	230	ns
Rise Time, t_{R+}	35	60	240	55	200	ns
High-to-Low						
Delay Time, t_{D-}	50	50	80	55	80	ns
Fall Time, t_{F-}	25	110	400	80	275	ns

Typical Switching Times

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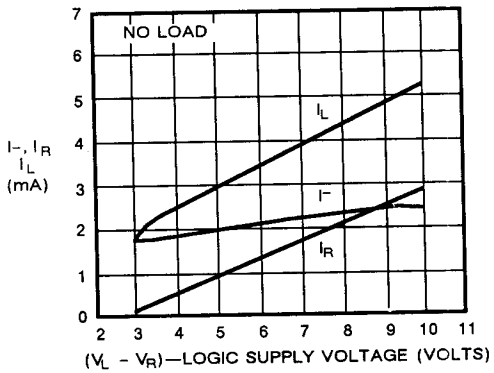
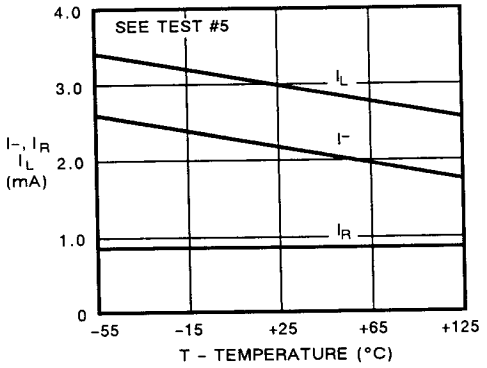
TYPICAL CHARACTERSITICS

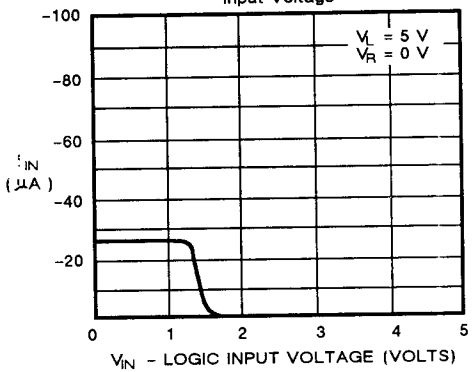
Supply Current Variation with Logic Supply



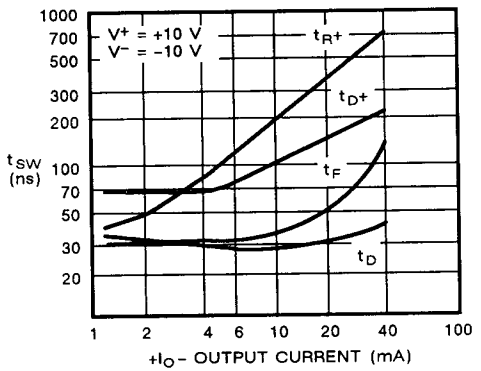
Effect of Temperature on Supply Currents



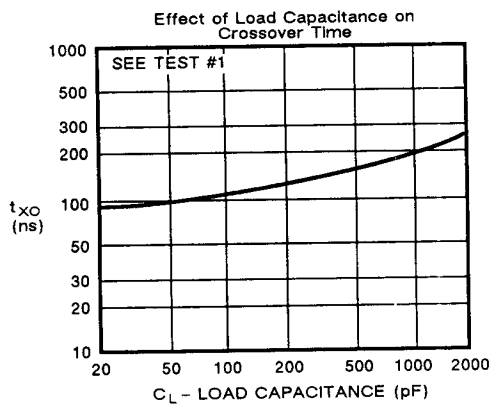
Logic Input Current vs. Logic Input Voltage



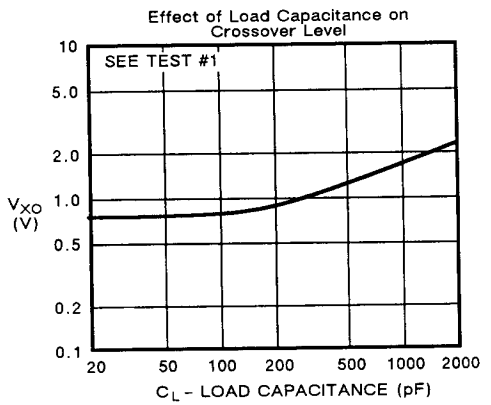
Switching Times with Resistive Load



Effect of Load Capacitance on Crossover Time

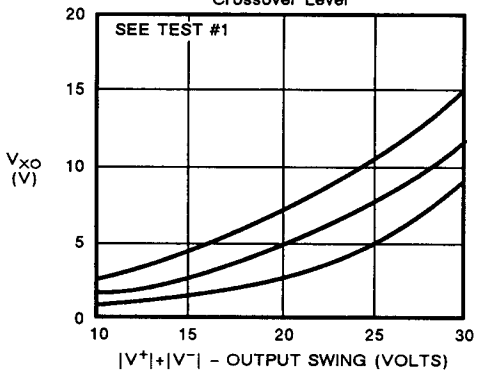


Effect of Load Capacitance on Crossover Level

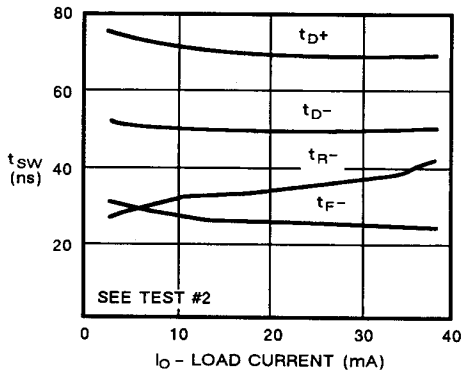


TYPICAL CHARACTERSITICS

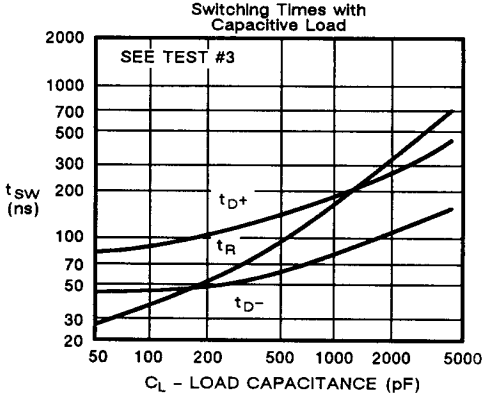
Effect of Voltage Output on Crossover Level



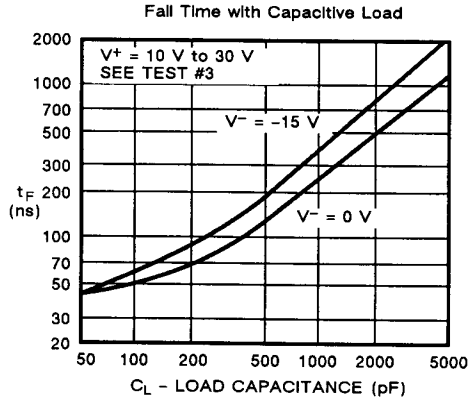
Resistive Load Switching



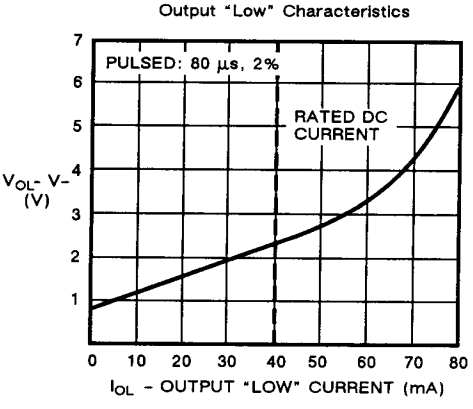
Switching Times with Capacitive Load



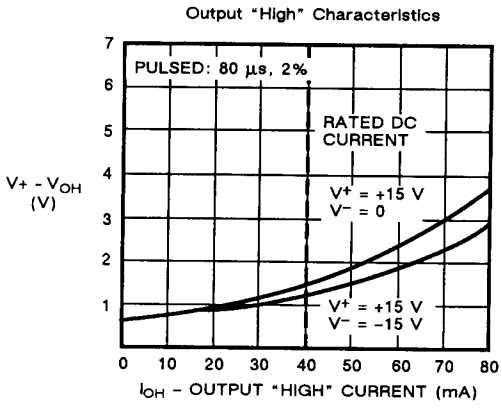
Fall Time with Capacitive Load



Output "Low" Characteristics



Output "High" Characteristics



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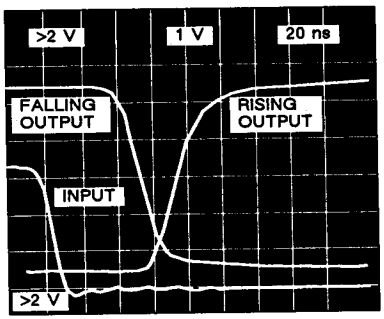
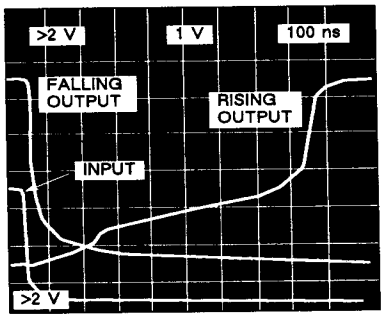
OPERATING GUIDELINES



40 mA LOAD, V+ = 20 V, V- = 0 V
Switching Waveform



+40 mA LOAD, V+ = 10 V, V- = -10 V
Switching Waveform

For proper performance of the D169 circuit, certain guidelines must be followed for the power supply and input terminals. These are listed below.

TERMINAL	ALLOWABLE CONDITIONS
V+ (Pin 6) V- (Pin 9)	Any positive voltage Any negative voltage or zero volts $10\ V \leq V+ - V- \leq 36\ V$
V_R (Pin 8)	$\geq V_{EE}+ 1$ V (Input Threshold = $V_R + 1.4$ V)
V_L (Pin 7)	$V_L - V_R \geq 4$ V
IN1L, IN2L (Pins 5, 10)	$\geq V_{EE} + 1$ V
IN1H, IN2H (Pins 5, 10)	$\geq V_{EE} + 3$ V

CIRCUIT OPERATION

The D169 circuit has three sections: (1) an input level detector, (2) a level shifter, and (3) a pair of complementary emitter-follower outputs. This arrangement provides a high input impedance, high output drive capability, and compatibility with a wide range of power supply levels. The input threshold level can be easily varied to accept various logic levels. Output swing is set by the V+ and V– power supply levels.

Level Detector

Transistors Q_1 and Q_2 form a differential input pair. Transistor Q_0, resistor R_1, and diodes D_1 and D_2 form a current source of about 1 mA which drives the common emitter connection. The voltage between supply levels V_L and V_R determines the trip point where the circuit changes state. With V_R grounded, the trip point is about 1.4 volts, depending somewhat on the voltage V_L. The input characteristics are shown in Figure 5.

Level Shifter

Schottky-clamped transistors Q_3 and Q_4 along with P-channel MOSFETs Q_5 and Q_6 form a complementary-coupled switching stage. This configuration draws no idle current and permits a change of state within 100 ns after the input signal passes the trip point. The circuit delays are such that the

CIRCUIT OPERATION (Cont'd)

that the switching action approaches a "break-before-make" sequence as shown in Figure 15. The response times are essentially independent of the input signal level and rise time.

The time measured from the input signal step to where the output waveforms from OUT and $\overline{OUT}$ cross is called cross-over time. The voltage level at that time with respect to V– is called crossover voltage. This point is of importance when driving certain loads where a break-before-make action is necessary to avoid high current surges. The crossover time is essentially independent of output voltage swing, but is affected by the load capacitance as shown in Figure 7. The delay time of the negative going waveform from OUT and $\overline{OUT}$ is not significantly affected by load capacitance; however the delay time of the positive going waveform experiences a delay which is fairly sensitive to load capacitance. This feature reduces the dependence of crossover voltage on the load capacitance as shown in Figure 8. However, the output voltage swing does exert considerable influence upon crossover level as indicated in Figure 9.

In order to provide adequate drive to Q_3 and Q_4, the voltage at the collector of the differential pair must be more positive than the V– level plus the base emitter drop of the schottky transistors. This dictates that the "low" level of V_{IN} should exceed V– by at least one volt.

APPLICATIONS

Totem-Pole Driver with Bootstrapping

When driving MOSPOWER in a totem-pole output configuration (see Figure 17), it is necessary to have the gate voltage 10 to 15 volts positive with respect to the source in order to handle load currents near the MOSPOWER maximum ratings. The D169 lends itself to bootstrapping because of its high voltage ratings.

In the circuit shown, the voltage on the 2000 pF bootstrap capacitors is applied via diode "OR" gates to the V+ terminal; therefore, regardless of which output is high, 30 V is present at V+. Maximum switching frequency is determined by the input capacitance of the MOSPOWER transistors used.

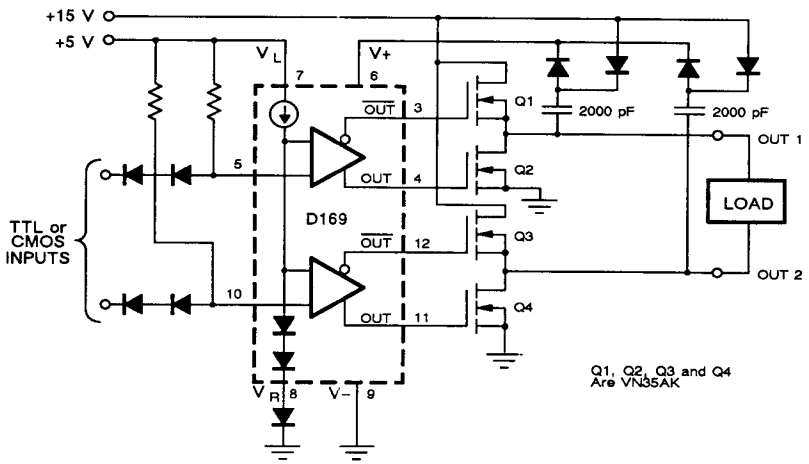


Figure 17. Totem-Pole Driver with Bootstrapping

APPLICATIONS (Cont'd)

Voltage-to-Frequency Converter

A simple, low-cost VFC can be designed using the D169 and a single op amp (see figure 18). The D169 serves as a level detector and provides complementary outputs. The op amp is used to integrate the input signal V_{IN} with a time constant of R_1C_1. The input, which must be negative, causes a positive ramp at the output of the integrator which is then summed with a negative zener voltage. When the ramp is positive enough to cause the D169 input (pin 10) to exceed the logic threshold of 1.4 V, then the D169 outputs change state and OUT 2 flips from negative to positive. This positive output of approximately 11 V puts transistor Q_1 into saturation which then resets the integrator to near zero. The integrator peak differential voltage ΔV will be approximately 9.2 V. The output frequency f_O, neglecting the short reset interval, will be

$$f_O = \frac{1}{R_1 C_1 \Delta V} V_{IN}, V_{IN} < 0$$

The pulse repetition rate, f_O, is directly proportional to the negative input voltage V_{IN}.

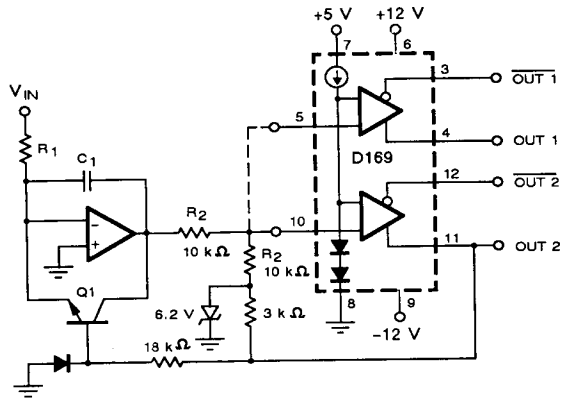


Figure 18. D169 Used as a Voltage-to-Frequency Converter

H-BRIDGE SWITCH APPLICATION

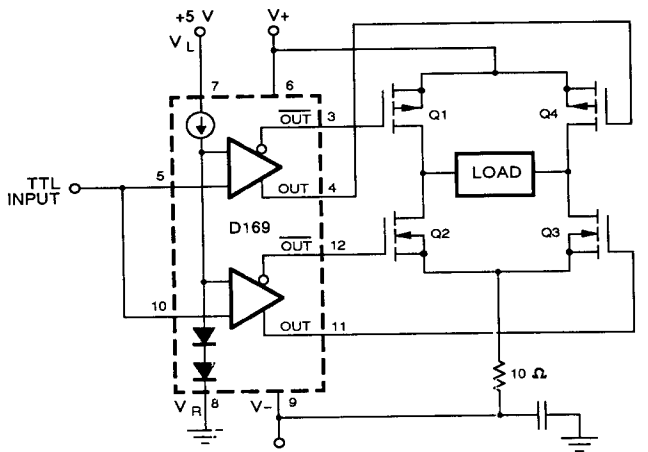


Figure 19. Driver for MOSPOWER H-Switch