Features

256Kx32 bit BiCMOS and CMOS Static Random Access Memory

- Access Times
  - BiCMOS: 10, 12 and 15ns
  - CMOS: 20ns
- Individual Byte Writes
- Output Enable Function
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Package

- 80 Pin SIMM, Gold Contacts No. 353
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

256Kx32 Static RAM CMOS, High Speed Module

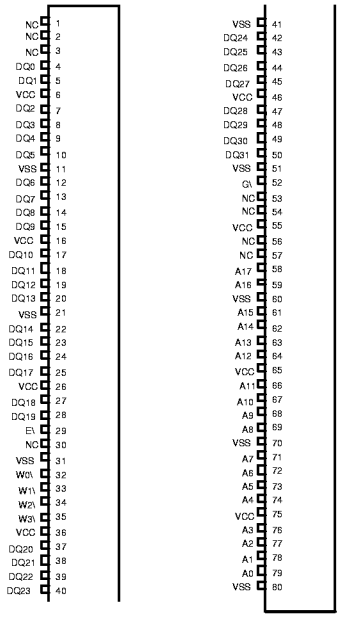
The EDI9F32255B\C is a high speed 8 megabit Static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Read operations are performed in x32 transfers. Writing can be executed on individual bytes or any combination of multiple bytes.

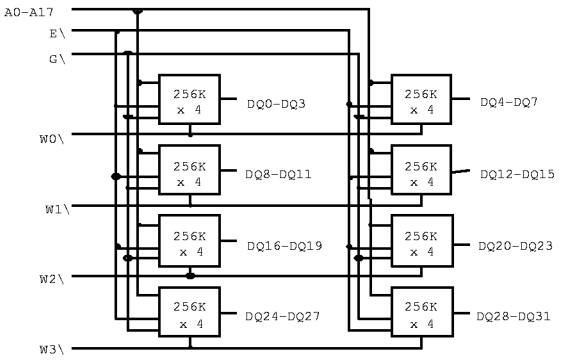
The EDI9F32255B/C is offered in a 80 pin SIMM package which enable 8 megabits of memory to be placed in less than 1.6 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Pin Configurations and Block Diagram



AØ-A17	Address Inputs
$\overline{EØ}$\	Chip Enable
$\overline{WØ}$\-$\overline{W3}$\	Write Enables
$\overline{GØ}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial.	0 ℃ to +70 ℃
Industrial	-40 ℃ to +85 ℃
Storage Temperature, Plastic	-55 ℃ to +125 ℃
Power Dissipation	8 Watt
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.3V	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	1.5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 50pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max 10ns	Max 12ns	Max 15/20ns	Units
Operating Power Supply Current	ICC1	W, $\overline{EO}$, $\overline{EI}$\ = VIL, II/O = 0mA		1,320	1,240	1,160	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{EO}$\or $\overline{EI}$\ • VIH, VIN - VIL or VIN • VIH		960	960	960	mA
Full Standby CMOS Power Supply Current	ICC3	$\overline{EO}$, $\overline{EI}$ • VCC-0.2V VIN • VCC-0.2V or VIN - 0.2V		160	160	160	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	±80	±80	±80	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	±20	±20	±20	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	0.4	0.4	0.4	V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	60	pF
Data Lines	CD/Q	20	pF
Chip Enable	CC	60	pF
Write Enable, Output Enable	CN	20	pF

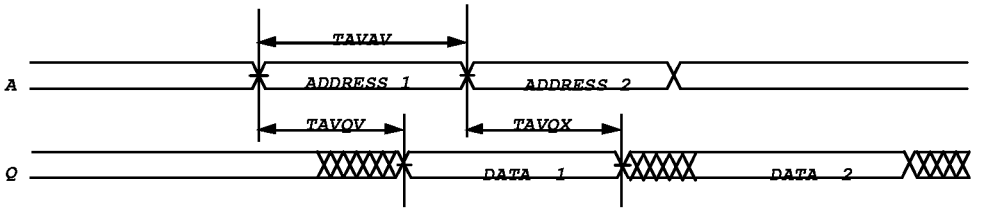
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

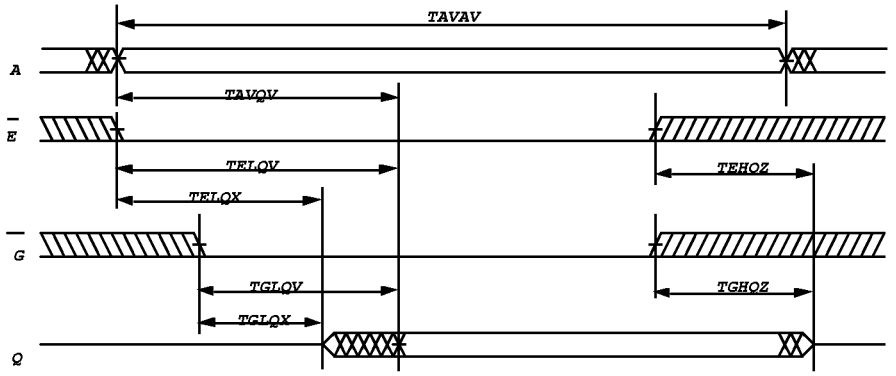
Parameter	Symbol JEDEC	Alt.	10ns* Min	10ns* Max	12ns* Min	12ns* Max	15ns* Min	15ns* Max	20ns Min	20ns Max	Units
Read Cycle Time	TAVAV	TRC	10		12		15		20		ns
Address Access Time	TAVQV	TAA		10		12		15		20	ns
Chip Enable Access	TELQV	TACS		10		12		15		20	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		5		6		8		10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		5		6		13	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		4		4		5		8	ns

Note 1: Guaranteed but not tested. *BICMOS

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{CØ}$ or $\overline{CE1}$ Low



Read Cycle 2 - $\overline{W}$ High

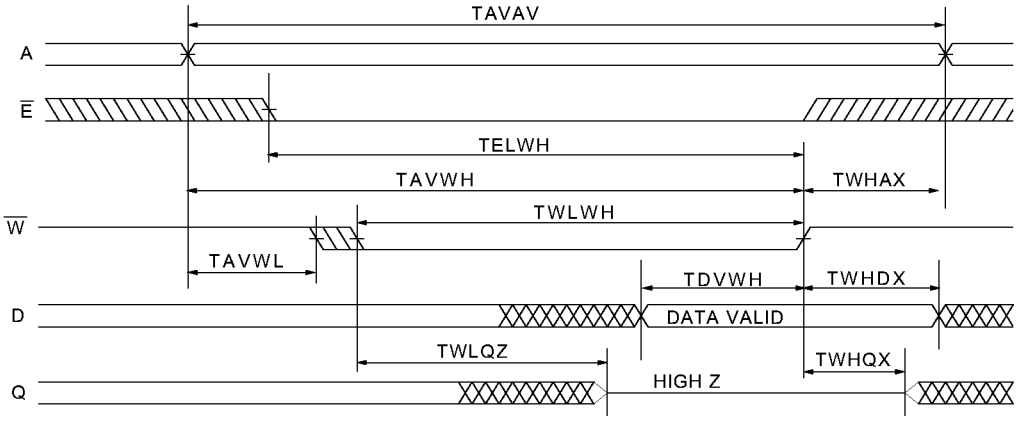


AC Characteristics Write Cycle

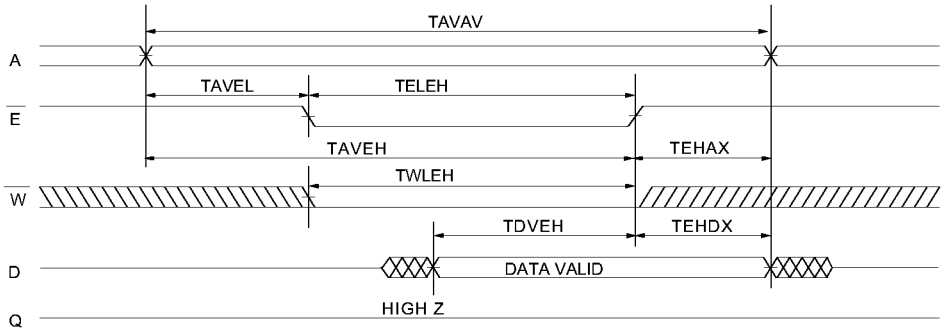
Parameter	Symbol JEDEC	Symbol Alt.	10ns* Min	10ns* Max	12ns* Min	12ns* Max	15ns* Min	15ns* Max	20ns Min	20ns Max	Units
Write Cycle Time	TAVAV	TWC	10		12		15		20		ns
Chip Enable to End of Write	TELWH	TCW	7		8		10		15		ns
	TWLEH	TCW	7		8		10		15		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	7		8		10		15		ns
	TAVEH	TAW	7		8		10		15		ns
Write Pulse Width	TWLWH	TWP	7		8		10		15		ns
	TELEH	TWP	7		8		10		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		3		ns
	TEHDX	TDH	3		3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	7	0	10	ns
Data to Write Time	TDVWH	TDW	5		6		7		12		ns
	TDVEH	TDW	5		6		7		12		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		3		ns

Note 1: Parameter guaranteed, but not tested. *BICMOS

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



Ordering Information

Part Number	Speed (ns)	Package No.
EDI9F32255B10MMC	10	353
EDI9F32255B12MMC	12	353
EDI9F32255B15MMC	15	353
EDI9F32255C20MMC	20	353

Note 1: Available with Gold Contacts Only.

Package Description

Package No. 353
80 lead SIM