Symbios® SYM53C710 SCSI I/O Processor

Technical Manual

March 2000

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This document describes the LSI Logic Corporation's Symbios® SYM53C710 SCSI I/O Processor and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This book is the primary reference and technical manual for the SYM53C710 SCSI I/O Processor. It contains a complete functional description for the product and includes complete physical and electrical specifications.

Audience

This manual assumes some prior knowledge of current and proposed SCSI and PCI standards.

Organization

This document has the following chapters and appendixes:

- Chapter 1, **General Description**, includes general information about the SYM53C710.
- Chapter 2, **Functional Description**, describes the main functional areas of the chip in more detail, including interfaces to the SCSI bus and external memory.
- Chapter 3, **Signal Descriptions**, contains pin diagrams and signal descriptions.
- Chapter 4, **Registers**, describes each bit in the operating registers, and is organized by register address.
- Chapter 5, **Instruction Set of the I/O Processor**, defines the SCSI SCRIPTS instructions supported by the SYM53C710.
- Chapter 6, **Electrical Specifications**, contains the electrical characteristics and AC timing diagrams.
- Appendix A, **Register Summary**, is a register summary.

- Appendix B, **Register and Bit Differences Between the SYM53C710 and SYM53C700**, explains the differences between the SYM53C710 and SYM53C700.
- Appendix C, **Mechanical Drawing**, is a mechanical drawing.
- Appendix D, **Setting Data Transfer Rates**, explains how to get the proper data transfer speed on the SCSI bus.

Related Publications

For background please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-1994 (SCSI-2)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2) or X3.253
(SCSI-3 Parallel Interface)

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Prentice Hall
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

SCSI Electronic Bulletin Board
(719) 533-7950

LSI Logic Internet Anonymous FTP Site
ftp.symbios.com (204.131.200.1)
Directory: /pub/symchips/scsi

LSI Logic World Wide Web Home Page
www.lsilogic.com

PCI Special Interest Group
2575 N.E. Katherine
Hillsboro, OR 97214
(800) 433-5177; (503) 693-6232 (International); FAX (503) 693-8344

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Revision Record

Revision	Date	Remarks
0.1	2/90	Draft.
0.2	4/90	Draft.
0.3	5/90	Draft.
0.99	8/90	Draft.
1.0	9/90	Preliminary Version.
2.0	9/91	Complete Rewrite.
2.1	6/92	Move Chapter 6, Electrical Specifications, to separate manual.
3.0	11/93	Chapter 6, Electrical Specifications, incorporated back into Data Manual; Misaligned Transfers section modified; updates to Chapter 4; Appendix D added with appropriate SENs.
3.1	3/00	Miscellaneous cosmetic/format changes from Symbios to LSI Logic.

Contents

Figures

Tables

Chapter 1
General Description

This chapter contains the following section:

- Section 1.1, “SYM53C710 Features Summary”

The SYM53C710 is the second member of the SYM53C700 family of intelligent, single chip, third generation SCSI host adapters. A high-performance SCSI core and an intelligent 32-bit bus master DMA core are integrated with a SCSI SCRIPTS™ processor to accommodate the flexibility requirements of SCSI-1, SCSI-2, and future SCSI standards. The SYM53C710 solves the protocol overhead problems that have plagued all previous intelligent and nonintelligent adapter designs.

The SYM53C710 is designed to completely implement a multithreaded I/O algorithm in either a workstation or file server environment, completely free of processor intervention except at the end of an I/O transfer. In addition, the SYM53C710 allows SCSI SCRIPTS instructions to be relocated if necessary, and requires no dynamic alteration of SCRIPTS instructions at the start of an I/O operation. All of the SCRIPTS code may be placed on a PROM. The SYM53C710 allows easy firmware upgrades and is SCRIPTS compatible with the SYM53C700.

The SYM53C710 supports two different host processor interfaces. Bus Mode 1 closely resembles the Motorola 68030 interface, and Bus Mode 2 closely resembles the 68040 interface. The modes are selected by using the bus mode select pin.

The SYM53C710 features Symbios® TolerANT® Active Negation Technology, which allows optional active negation of SCSI signals during information transfer phases. When enabled, TolerANT causes the SCSI REQ, ACK, Data and Parity signals to be actively pulled up to approximately three volts by transistors on each pin. The benefits of this technology include reduced noise when the signal is going high (deasserted), increased performance due to balanced duty cycles, and

improved fast SCSI transfer rates. Active Negation is enabled by setting the EAN bit in the Chip Test Zero (CTEST0) register. It can be used in both Single-Ended (SE) and differential mode. TolerANT is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

This manual provides descriptions and operational information for the SYM53C710 and SYM53C710-1. The SYM53C710 supports Bus Mode 1 (asynchronous) DMA timings up to 25 MHz, and Bus Mode 2 (synchronous) DMA timings up to 33 MHz. The SYM53C710-1 supports asynchronous timings up to 33 MHz and synchronous timings up to 40 MHz. Electrical characteristics and timings for the SYM53C710 and SYM53C710-1 are provided in Chapter 6, "Electrical Specifications".

1.1 SYM53C710 Features Summary

This section provides an overview of the SYM53C710 features and benefits. It contains information on Performance, Integration, Ease of Use, Flexibility, Reliability, and Testability.

1.1.1 Performance

- Supports variable block size and scatter/gather data transfers
- Supports 32-bit word data bursts with variable burst lengths
- High-speed SCSI bus transfers
  - Over 5 Mbytes/s asynchronous
  - 10 Mbytes/s synchronous
- 42.66 Mbytes/s sustained host bus bandwidth
- Enhanced SCRIPTS capabilities
  - Relative jump
  - Table indirect data mode
  - Read/write system memory
  - Read/write registers
  - Arithmetic operations
  - Memory-to-Memory DMA transfers

- Register parity during slave reads
- Glitchless SCSI on power-up/down
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts
- Unique interrupt status reporting reduces Interrupt Service Routine (ISR) overhead
- Cache line burst mode
- 64-byte DMA FIFO
- Active negation of SCSI Data, Parity REQ and ACK signals with Symbios TolerANT technology improves rise times and fast SCSI transfer rates in both SE and differential modes

1.1.2 Integration

- Full 32-bit DMA bus master
- High-performance SCSI core
- Integrated SCRIPTS processor
- Allows intelligent host adapter performance on a motherboard

1.1.3 Ease of Use

- Reduces SCSI development effort
- Emulates existing intelligent host adapters
- Support for big and little endian byte ordering
- Easily adapted to the SCSI Common Access Method (CAM) by “executing” data structures
- Fully compatible with existing SYM53C700 SCRIPTS
- Development tools and SCSI SCRIPTS provided
- All interrupts are maskable and pollable

1.1.4 Flexibility

- High level programmer’s interface (SCSI SCRIPTS)
- Allows tailored SCSI sequences to be executed from main memory or from a host adapter board

- Flexible sequences to tune I/O performance or to adapt to unique SCSI devices
- Accommodates changes in the logical I/O interface definition
- Low level programmability (register-oriented)
- Allows a target to disconnect and later reselect the SYM53C710 with no interrupt to the system processor
- Allows a multithreaded I/O algorithm to be executed in SCSI SCRIPTS with a fast I/O context switch
- Can autoswitch between initiator and target roles dynamically
- Allows indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM
- Separate SCSI and system clocks

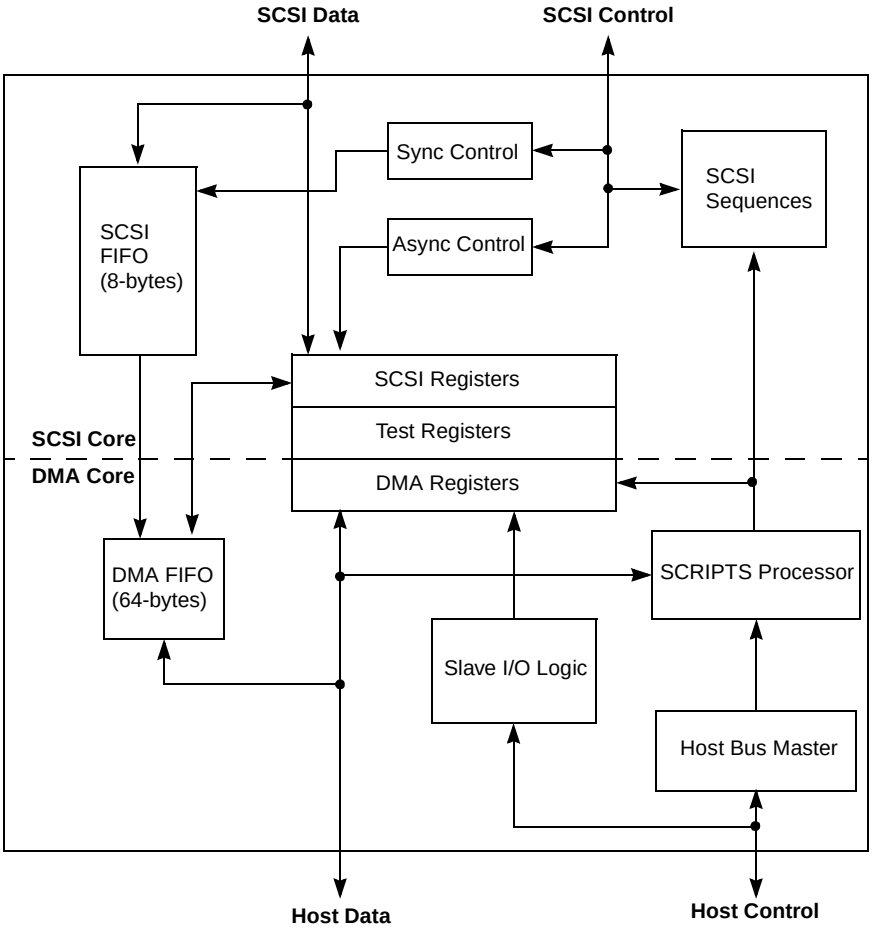
1.1.5 Reliability

- 2 kV minimum ESD protection
- Typical 350 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- 250 ms byte-to-byte SCSI activity timer
- Voltage feed-through protection (minimum leakage current through SCSI pads)
- 20% of signals are power and ground
- Ground isolation of I/O pads and chip logic

1.1.6 Testability

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- Self-selection capability
- SCSI bus signal continuity checking

Figure 1.1 SYM53C710 Block Diagram



Chapter 2
Functional Description

The SYM53C710 is composed of three tightly coupled functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor.

This chapter contains the following sections:

2.1 SCSI Core

The SCSI core supports synchronous transfer rates of up to 10 Mbytes/s, and asynchronous transfer rates greater than 5 Mbytes/s. The programmable SCSI interface makes it easy to fine tune the system for specific mass storage devices or SCSI-2 requirements.

The SCSI core offers low level register access or a high level control interface. Like first generation SCSI devices, the SYM53C710 SCSI core is accessible as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus is used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core performs a self-selection and operates as both an initiator and a target. The SYM53C710 tests the SCSI pins for physical connection to the board or the SCSI bus.

Unlike previous generation devices, the SCSI core can be controlled by the integrated DMA core through a high level logical interface. Commands controlling the SCSI core are fetched out of the main host memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus Phases and in general, implement all aspects of the SCSI protocol.

2.1.1 DMA Core

The DMA core is a bus master DMA device that directly attaches to 68030 and 68040 processors, and to other processors (80386, 80486, etc.) with minimum logic.

The SYM53C710 supports 32-bit memory and automatically supports misaligned DMA transfers. A 64-byte FIFO allows the SYM53C710 to support one, two, four, or eight longwords to be burst across the memory bus interface. This DMA interface does not support dynamic bus sizing.

The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor which supports uninterrupted scatter/gather memory operations.

2.2 SCRIPTS Processor

The SCRIPTS processor is a special high speed processor optimized for SCSI protocol. It allows both DMA and SCSI instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTS can control the actions of the SCSI and DMA cores and are executed from 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This compares with 2–8 ms required for traditional intelligent host adapters. The SCRIPTS processor offers performance and customized algorithms. Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (i.e. scanners, communication gateways, etc.) or to incorporate changes in the SCSI-2/SCSI-3 logical bus definitions without sacrificing I/O performance.

2.2.1 Loopback Mode

The SYM53C710 loopback mode allows testing of both initiator and target operations and, in effect, lets the chip talk to itself. When the Loopback Enable bit is set in the Chip Test Four (CTEST4) register, the SYM53C710 allows control of all SCSI signals, whether the SYM53C710 is operating in initiator or target mode.

2.2.2 Parity Options

The SYM53C710 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and can deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation.

Control

Assert ATN/ on Parity Errors (AAP) – Bit 1 in the SCSI Control Zero (SCNTL0) register. This bit causes the SYM53C710 to automatically assert SCSI ATN/ when it detects a parity error while operating as an initiator.

Enable Parity Generation (EPG) – Bit 2 in the SCSI Control Zero (SCNTL0) register. This bit determines whether the SYM53C710 generates parity sent to the SCSI bus or allows parity to “flow through” the chip to/from the SCSI bus and system bus.

Enable Parity Checking (EPC) – Bit 3 in the SCSI Control Zero (SCNTL0) register. This bit enables the SYM53C710 to check for parity errors. The SYM53C710 checks for odd parity.

Assert Even SCSI Parity (AESP) – Bit 2 in the SCSI Control One (SCNTL1) register. This bit determines the SCSI parity sense generated by the SYM53C710.

Disable Halt on ATN/ or a Parity Error (DHP: Target Mode Only) –

Bit 7 in the SCSI Transfer (SXFER) register. This bit causes the SYM53C710 to immediately halt operations when a parity error is detected in target mode.

Enable Parity Error Interrupt (PAR) – Bit 0 in the SCSI Interrupt Enable (SIEN) register. This bit determines whether the SYM53C710 generates an interrupt when it detects a parity error.

Observation

Parity Error – Bit 0 in the SCSI Status Zero (SSTAT0) register. This status bit is set whenever the SYM53C710 detects a parity error on either the SCSI bus or the system bus.

Status of SCSI Parity Signal – Bit 0 in the SCSI Status One (SSTAT1) register. This status bit represents the live SCSI Parity Signal (SDP/).

Latched SCSI Parity Signal – Bit 3 in the SCSI Status Two (SSTAT2) register. This status bit contains the SCSI parity of the byte latched in the SIDL.

DMA FIFO Parity – Bit 3 in the Chip Test Two (CTEST2) register. This status bit represents the parity bit in the DMA FIFO after data is read from the FIFO by reading the Chip Test Six (CTEST6) register.

DMA FIFO Parity – Bit 3 in the Chip Test Seven (CTEST7) register. This write only bit is written to the DMA FIFO after writing data to the DMA FIFO by writing the Chip Test Six (CTEST6) register.

SCSI FIFO Parity – Bit 4 in the Chip Test Two (CTEST2) register. This status bit represents the parity bit in the SCSI FIFO after data is read from the FIFO by reading the Chip Test Three (CTEST3) register.

Table 2.1 Parity Control

EVP[1]	EPG[2]	EPC[3]	AESP[4]	Description
0	0	0	0	**Does not check for parity errors.** Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data and host data.
0	0	0	1	**Does not check for parity errors.** Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data, odd parity when sending host data.
0	0	1	0	**Checks for odd parity on both SCSI data received and system data when sending.** Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data and host data.
0	0	1	1	**Checks for odd parity on both SCSI data received and system data when sending.** Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data, and odd parity when sending host data.
0	1	0	0	**Does not check for parity errors.** Parity on DP[2:0] is ignored and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip but is not asserted on DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	0	1	**Does not check for parity errors.** Parity on DP[2:0] is ignored, and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.
0	1	1	0	**Checks for odd parity on SCSI data received.** Parity on DP[2:0] is ignored, and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	1	1	**Checks for odd parity on SCSI data received.** Parity on DP[2:0] is ignored and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.

Table 2.1 Parity Control (Cont.)

EVP[1]	EPG[2]	EPC[3]	AESP[4]	Description
1	0	0	0	**Does not check for parity errors.** Parity flows from DP[2:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data, and even parity when sending host data.
1	0	0	1	**Does not check for parity errors.** Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data and host data.
1	0	1	0	**Checks for odd parity on SCSI data received and even parity on system data when sending.** Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data and even parity when sending host data.
1	0	1	1	**Checks for odd parity on SCSI data received and even parity on system data when sending.** Parity flows from DP[3:0] through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data and host data.
1	1	0	0	**Does not check for parity errors.** Parity on DP[2:0] is ignored, and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip but is not asserted on DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	0	1	**Does not check for parity errors.** Parity on DP[2:0] is ignored, and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.
1	1	1	0	**Checks for odd parity on SCSI data received.** Parity on DP[2:0] is ignored, and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	1	1	**Checks for odd parity on SCSI data received.** Parity on DP[2:0] is ignored, and DP3 becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP[3:0] when receiving SCSI data. Asserts even parity when sending SCSI data.

1. Even Parity.
2. Enable Parity Generation.
3. Enable Parity Checking.
4. Assert SCSI Even Parity.

2.3 DMA FIFO

The DMA FIFO is a 64 x 9 bit FIFO. It can be divided into four sections, each nine bits wide and 16 transfers deep as shown in Figure 2.1. Each of these four sections are called byte lanes. Each byte lane can be individually tested by writing known data into the FIFO and reading that same data back out of the FIFO.

Figure 2.1 DMA FIFO Sections

2.3.1 Interrupted Transfer Cleanup

The data path through the SYM53C710 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

Figure 2.2 shows how data is moved to or from the SCSI bus in each of the different modes.

The following steps determine if any bytes remain in the data path when the chip halts an operation:

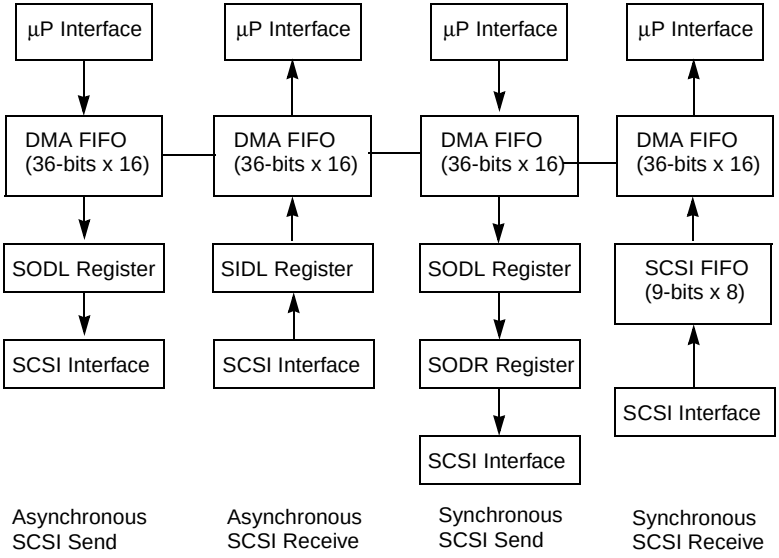
Asynchronous SCSI Send – Use the algorithm described in the DMA FIFO (DFIFO) register description (Chapter 4, “Registers”) to determine if any bytes are left in the DMA FIFO. Read the SCSI Status One (SSTAT1) register and examine bit 5 to determine if any bytes are left in the SCSI Output Data Latch (SODL) register. If bit 5 is set, then there is a byte in the SODL register.

Synchronous SCSI Send – Use the algorithm described in the DMA FIFO (DFIFO) register description to determine if any bytes are left in the DMA FIFO. Read the SCSI Status One (SSTAT1) register and examine bit 5 to determine if any bytes are left in the SCSI Output Data Latch (SODL) register. If bit 5 is set, then there is a byte in the SODL register. Read the SCSI Status One (SSTAT1) register and examine bit 6 to determine if any bytes are remaining in the SODR register. If bit 6 is set, then there is a byte in the SODR register.

Asynchronous SCSI Receive – Use the algorithm described in the DMA FIFO (DFIFO) register description to determine if any bytes are left in the DMA FIFO. Read the SCSI Status One (SSTAT1) register and examine bit 7 to determine if a byte is left in the SCSI Input Data Latch (SIDL) register. If bit 7 is set, then there is a byte in the SIDL register.

Synchronous SCSI Receive – Use the algorithm described in the DMA FIFO (DFIFO) register description to determine if any bytes are left in the DMA FIFO. Read the SCSI Status Two (SSTAT2) register and examine bits [7:4], the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

Figure 2.2 SYM53C710 Data Paths



2.4 Host Interface

2.4.1 Big/Little Endian Support

The big/little endian mode select pin gives the SYM53C710 the flexibility of operating with either byte orientation. Internally, in either mode, the byte lanes of the DMA FIFO and registers are not modified.

When a longword is accessed, no repositioning of the individual bytes is necessary, since longwords are addressed identically in either mode. Longwords are always used by SCRIPTS, compatibility is maintained.

Big/little endian mode selection has the most effect on individual byte access. Internally, the SYM53C710 adjusts the byte control logic of the DMA FIFO and register decodes to access the appropriate byte lane. The registers always appear on the same byte lane, but the address of the register is repositioned.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address ‘n’—there is no byte ordering in the chip. The first byte in from the SCSI bus goes

to address 0, the second to address 1, etc. Going out onto the SCSI bus, address 0 is the first byte out on the SCSI bus, address 1 is the second byte, etc.

Correct SCRIPTS is generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPTS patching in memory must patch the instructions in the order that the SCRIPTS processor expects it.

Software drivers for the SYM53C710 should access registers by their logical name (i.e., “SCNTL0”) rather than by their address. The logical name should be equated to the register’s big endian address in big endian mode (SCNTL0 = 0x03), and its little endian address in little endian mode (SCNTL0 = 0x00). This way, there is no change to the software when moving from one mode to the other; only the equate file needs to be changed. Addressing of registers from within a SCRIPTS is independent of bus mode. Internally, the SYM53C710 always operates in little endian mode.

2.4.2 Big Endian Mode

Big endian addressing is used primarily in designs based on Motorola processors. The SYM53C710 treats D[31:24] as the lowest physical memory address. The register map is left justified (Address 0x03 = SCNTL0) as detailed below.

2.4.3 Little Endian Mode

Little endian is used primarily in designs based on Intel processors. This mode treats D[7:0] as the lowest physical memory address. The register map is right justified (Address 0x00 = SCNTL0) as detailed below.

Table 2.2 Big and Little Endian Addressing

System Data Bus	[31:24]	[23:16]	[15:8]	[7:0]
SYM53C710 Pins	[31:24]	[23:16]	[15:8]	[7:0]
Register	SIEN	SDID	SCNTL1	SCNTL0
Little Endian Addr	0x03	0x02	0x01	0x00
Big Endian Addr	0x00	0x01	0x02	0x03

2.4.4 Misaligned Transfers

The SYM53C710 accommodates block data transfers beginning or ending on odd byte or odd word addresses in system memory. Such transfers are termed “misaligned.” An odd byte is defined as one in which the address contains A0 = 1. An odd word is defined as one in which the address contains A1 = 1. Misaligned transfers differ depending on the type of transfer (cache line or programming bursting) and whether they occur at the start or end of the transfer.

Note: The SYM53C710 does not perform 3-byte transfers.

2.4.5 Cache Line Bursting

If cache line bursting is supported by the external memory device, it can be used to reduce host bus ownership by the SYM53C710, thereby improving system performance. During cache line burst mode, the handshaking that occurs between the memory system and the SYM53C710 is minimized, reducing host bus activity and allowing more time for other bus masters to gain access to the host bus.

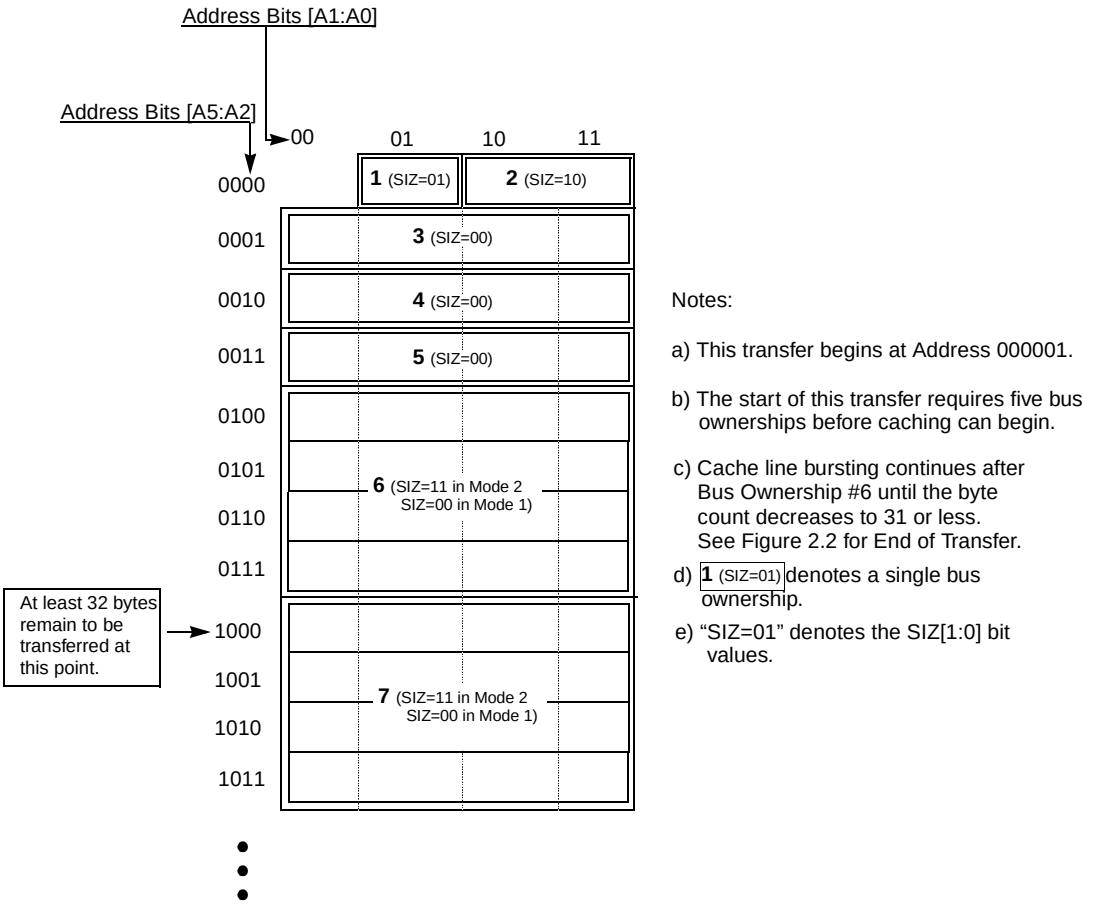
During caching mode, the SYM53C710 asserts one address and reads/writes four longwords of data with minimal handshaking (see Chapter 6, “Electrical Specifications” for cache line burst timings). Cache line burst mode is enabled in the SYM53C710 by clearing bit 7 in CTEST7. When using cache line burst mode, the burst length in DMODE must be set to 4.

Caution: The chip will not perform correctly if the burst length is set to 1, 2 or 8, while caching is enabled.

2.4.6 Cache Line Burst with Start of Transfer Misaligned

At the start of the transfer, if the address starts at an odd byte boundary (address bit A0 = 1), the SYM53C710 lines up to a word boundary by performing a single byte (8-bit) transfer in a single bus ownership. Then, if the address is at an odd word boundary (address bit A1 = 1), the SYM53C710 lines up to a longword boundary by performing a single word (2-byte) transfer in a single bus ownership. At this point, a longword (4-byte) transfer is performed, one per bus ownership, until the address bits line up to a cache line boundary (A[3:0] = 0). Once aligned, cache line bursts of four longwords per bus ownership are performed until the byte count decreases to 31 or less. The worst case example of five bus ownerships before cache line bursting can begin is depicted in little endian mode in Figure 2.3.

Figure 2.3 Cache Line Bursting, Start of Transfer (Little Endian Mode)

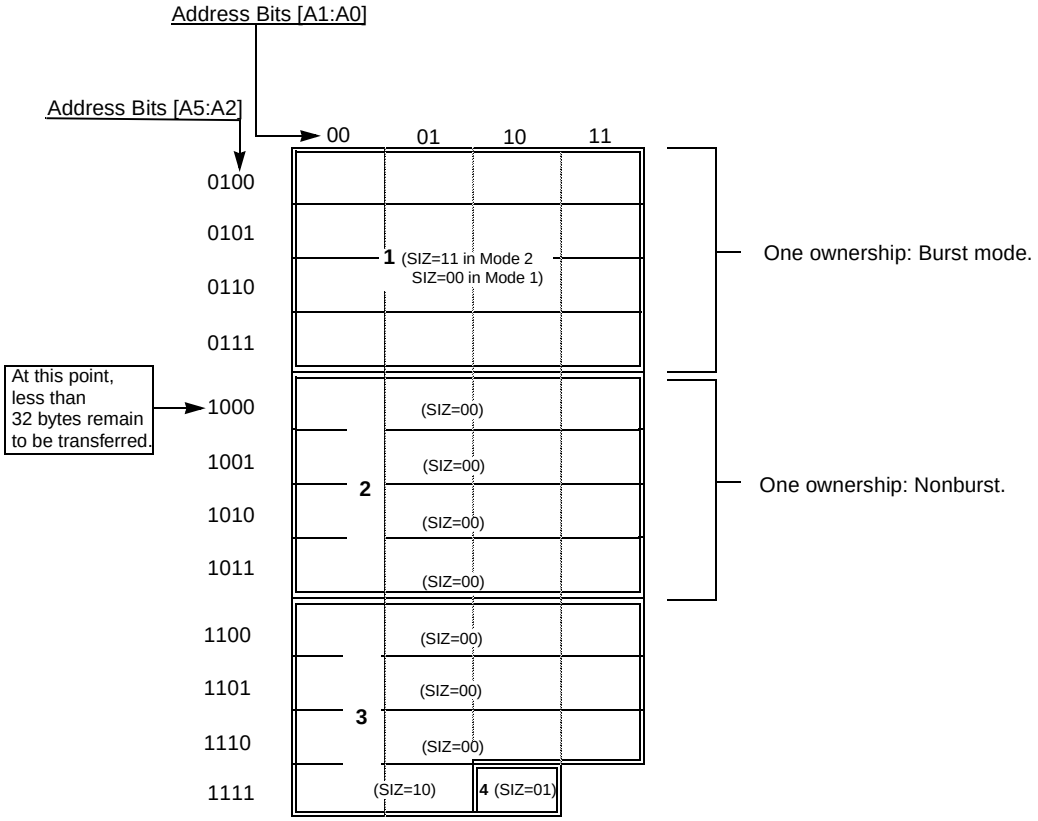


2.4.7 Cache Line Burst with End of Transfer Misaligned

When the byte count decreases to 31 or fewer bytes, the SYM53C710 drops out of cache burst mode and transfers the remaining longwords, words, and/or bytes in one or more bus ownerships until the transfer is complete. The SYM53C710 transfers longwords until the byte count decreases to 3 or less. If the byte count is 3 or 2, one word is transferred. If the byte count is 1, one byte is transferred. An example depicting the SYM53C710 dropping out of cache line burst mode with the byte count decreasing to 31 is shown in Figure 2.4.

Note: When doing cache line bursting during a Memory-to-Memory Move operation, the lower four address bits [A3:A0] of the source and destination must be equal. Cache line bursting will not start until [A3:A0] are zero.

Figure 2.4 Cache Line Bursting, End of Transfer (Little Endian Mode)



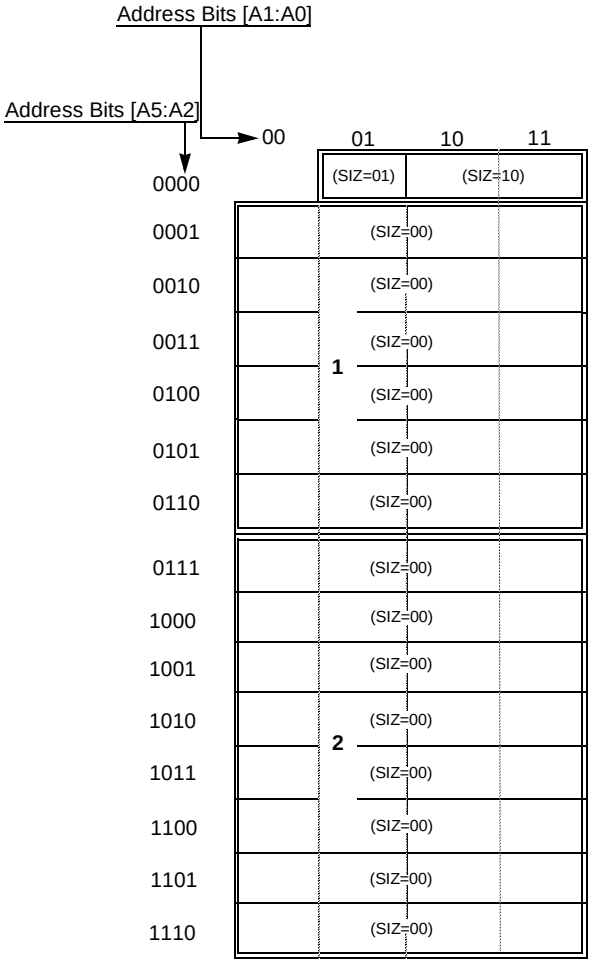
2.4.8 Programmable Bursting

The SYM53C710 performs programmable bursting when bit 7 in CTEST7 is set. In this mode, the SYM53C710 can perform 1, 2, 4 or 8 transfers per bus ownership, depending on the burst length value in the DMA Mode (DMODE) register. The transfers can be byte, word, or longword transfers, depending on the data alignment. During programmable burst mode, one TS/ is asserted per transfer, i.e., there is a complete handshake between the memory device and the SYM53C710 for each transfer.

2.4.9 Programmable Burst with Start of Transfer Misaligned

The SYM53C710 transfers the programmable burst length number of transfers during each bus ownership. If the address starts at an odd byte boundary (bit A0 = 1), the SYM53C710 lines up to a word boundary by performing a single byte transfer. If A1 = 1, the SYM53C710 performs a word transfer. At this point, the SYM53C710 transfers longwords until the byte count decreases to 3 or less. The chip transfers the programmable burst length number of transfers per bus ownership regardless of the width (byte, word or longword). An example of a transfer in which the programmable burst length is 8 is depicted in Figure 2.5.

Figure 2.5 Programming Bursting, Start of Transfer (Little Endian Mode)



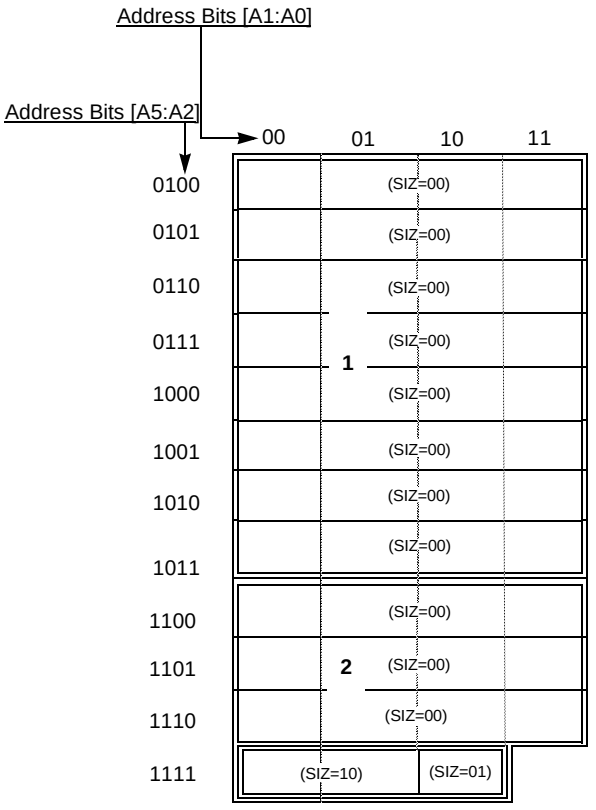
Note:
This transfer (programmable burst length = 8) involves two bus ownerships.

2.4.10 Programmable Burst with End of Transfer Misaligned

The SYM53C710 transfers longwords until the byte count decreases to 3 or less. If the byte count is 3 or 2, one word is transferred. If the byte count is 1, one byte is transferred. The SYM53C710 transfers the programmable burst length number of transfers per bus ownership. At the end of a block transfer, if the byte count is less than the programmable burst length, the remaining bytes are transferred during the bus ownership. It is possible to transfer less but not more than the programmable burst length number of transfers per bus ownership. An example of a transfer in which the programmable burst length is 8 is depicted in Figure 2.6.

Note: Each bus ownership requires the SYM53C710 to arbitrate for the host bus. There is a fairness delay of 5–8 clocks between each bus ownership.

Figure 2.6 Programming Bursting, Start of Transfer (Little Endian Mode)



Note:
This transfer (programmable burst length = 8) involves two bus ownerships.

2.4.11 Host Bus Retry

Host Bus Retry allows the SYM53C710 to retry the previous cycle using the same address, size, etc. The bus retry signals are asserted by an external device using the HALT/ (halt) and BERR/ (bus error) signals in Bus Mode 1, and TA/ (transfer acknowledge) and TEA/ (transfer error acknowledge) in Bus Mode 2. During a noncache line burst, a bus retry can be executed in any cycle. During a cache line burst, however, the bus retry should be executed during the ACK portion of the first transfer in the first cycle. In both bus modes, the SYM53C710 retries the bus cycle and asserts the CBREQ/ (Cache Burst Request) again. If a bus retry is attempted during one of the subsequent cycles, the SYM53C710 halts with a bus error status.

2.5 Bidirectional STERM/_TA/

The STERM/_TA/ signal terminates a read or write cycle. In a typical system, STERM/_TA/ is a wired-OR signal driven by slave devices and monitored by bus masters. When the system CPU is faster than the slave device being accessed, a cycle may be terminated as soon as the slave is ready. Slave devices which are faster than the CPU present a special problem in that they are required to insert wait states to allow the CPU to catch up. The SYM53C710 is able to accommodate both situations.

During slave accesses, the SLACK/ output provides an indication that the SYM53C710 is ready to terminate a read or write cycle. After asserting SLACK/, the SYM53C710 samples STERM/_TA/ on every subsequent rising BCLK edge until it is sampled active, at which time the read/write cycle is terminated. Any time between SLACK/ and STERM/_TA/ is treated as a wait state; a read/write cycle may be stretched indefinitely, but write data must be valid by the second clock cycle after Chip Select is sampled true.

Typically, SLACK/ is tied back to STERM/_TA/ as in Figure 2.7. If the system CPU is not capable of completing a slave cycle in the minimum time required by the SYM53C710, SLACK/ must be delayed before asserting STERM/_TA/. If the system CPU is capable of running slave read/write cycles with zero additional wait states, no delay is necessary.

In systems where the CPU is faster than the SYM53C710, SLACK/ may be connected to STERM/_TA/ with external logic, but the best solution is to set the Enable Acknowledge (EA) bit in the DMA Control (DCNTL) to internally connect SLACK/ to STERM_TA/. When the EA bit is set, the STERM/_TA/ pin changes from being an input in both master and slave modes, and becomes bidirectional: input in master mode, and output in slave mode. This way, no external logic is required and proper timing is guaranteed. Setting the EA bit must be the first slave I/O access to the SYM53C710. In addition, when the EA bit is set, a signal with the same timing characteristics as SLACK/ is driven onto the STERM/_TA/ pin, as illustrated in Figure 2.7. The external timing on this signal is the same as the signal generated if EA was not used, as illustrated in Figure 2.8. The additional control logic 3-states STERM/_TA/ for 5 ns after it is deasserted. The SLACK/ signal is always driven.

Figure 2.7 SLACK/ Tied Back to STERM/_TA/ (EA Bit Not Set)

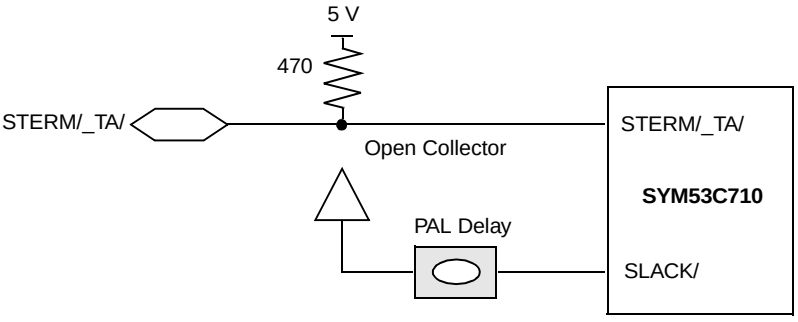
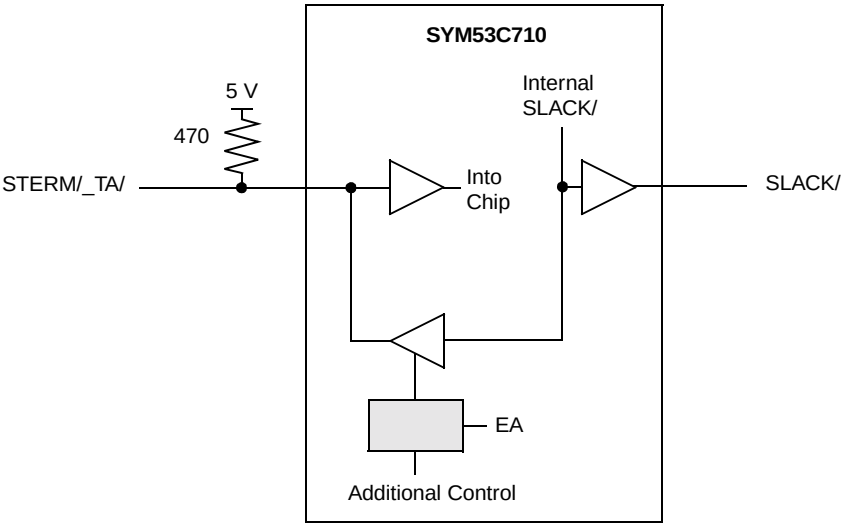


Figure 2.8 Bidirectional STERM/ (EA Bit Set)



2.6 Interrupts

2.6.1 Polling vs. Hardware Interrupts

The external microprocessor can be informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but it wastes CPU time that could be used by other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the SYM53C710 asserts the Interrupt Request (IRQ/) line that interrupts the microprocessor, causing the microprocessor to execute an Interrupt Service Routine (ISR). A hybrid approach would use hardware for long waits, and use polling for short waits.

2.6.2 Registers

The five registers in the SYM53C710 that are used for detecting or defining interrupts are Interrupt Status (ISTAT), SCSI Status Zero (SSTAT0), DMA Status (DSTAT), SCSI Interrupt Enable (SIEN) and DMA Interrupt Enable (DIEN).

ISTAT – The Interrupt Status (ISTAT) is the only register that can be accessed as a slave during SCRIPTS operation. Therefore, it is the register that is polled when polled interrupts are used. It is also the first register that should be read after the IRQ/ pin is asserted in association with a hardware interrupt.

If the SIP bit in the ISTAT register is set, then a SCSI-type interrupt occurs and the SCSI Status Zero (SSTAT0) register should be read.

If the DIP bit in the ISTAT register is set, then a DMA-type interrupt occurs and the DMA Status (DSTAT) register should be read. SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

SSTAT0 – The SCSI Status Zero (SSTAT0) register contains the SCSI-type interrupt bits. Reading this register determines which condition or conditions caused the SCSI-type interrupt, and clears that SCSI interrupt condition.

If the SYM53C710 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the chip attempts to send the contents of the DMA FIFO to memory before generating the interrupt.

If the SYM53C710 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. Because of this the DFE (DMA FIFO Empty) bit in DMA Status (DSTAT) should be checked. If this bit is cleared, set the CLF (Clear DMA and SCSI FIFOs) bit before continuing.

DSTAT – The DMA Status (DSTAT) register contains the DMA-type interrupt bits. Reading this register determines which condition or conditions caused the DMA-type interrupt, and clears that DMA interrupt condition. Bit 7 in DSTAT, DFE, is purely a status bit; it will not generate an interrupt under any circumstances and will not be cleared when read. DMA interrupts flush neither the DMA nor SCSI FIFOs before generating the interrupt, so the DFE bit in the DSTAT register should be checked after any DMA interrupt.

If the DFE bit is cleared, then the FIFOs must be cleared by setting the CLF (Clear DMA and SCSI FIFOs) bit (bit 2 in the Chip Test Eight (CTEST8)) register, or flushed by setting the FLF (Flush DMA FIFO) bit (bit 3 in the CTEST8 register).

SIEN – The SCSI Interrupt Enable (SIEN) register is the interrupt enable register for the SCSI interrupts in SCSI Status Zero (SSTAT0).

DIEN – The DMA Interrupt Enable (DIEN) register is the interrupt enable register for DMA interrupts in DMA Status (DSTAT).

2.6.3 Fatal vs. Nonfatal Interrupts

A fatal interrupt, as the name implies, always causes SCRIPTS to stop running. A nonfatal interrupt causes SCRIPTS to stop running only if it is not masked. Masking is discussed later in this technical manual. All DMA interrupts (indicated by the DIP bit in Interrupt Status (ISTAT) and one or more bits in DMA Status (DSTAT) being set) are fatal.

Some SCSI interrupts (indicated by the SIP bit in the Interrupt Status (ISTAT) and one or more bits in SCSI Status Zero (SSTAT0) being set) are nonfatal.

When the chip is operating in Initiator mode, only the Function Complete (CMP) and Selected or Reselected (SEL) interrupts are nonfatal.

When operating in Target mode CMP, SEL, and M/A (Target mode: ATN/ active) are nonfatal. Refer to the description for the Disable Halt on a Parity Error or ATN/ active (Target Mode Only) (DHP) bit in the SCSI Transfer (SXFER) register to configure the chip's behavior when the ATN/ interrupt is enabled during Target mode operation.

The reason for nonfatal interrupts is to prevent SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. This prevents an interrupt when arbitration is complete (CMP set), when the SYM53C710 is selected or reselected (SEL set), or when the initiator has asserted ATN (target mode: ATN/ active). These interrupts are not needed for events that occur during high level SCRIPTS operation.

2.6.4 Masking

Masking an interrupt means disabling or ignoring that interrupt. Interrupts can be masked by clearing bits in the SCSI Interrupt Enable (SIEN) (for SCSI interrupts) register or DMA Interrupt Enable (DIEN) (for DMA interrupts) register. How the chip responds to masked interrupts depends on whether polling or hardware interrupts are being used; whether the interrupt is fatal or nonfatal; and whether the chip is operating in Initiator or Target mode.

If a nonfatal interrupt is masked and that condition occurs, SCRIPTS does not stop, the appropriate bit in the SCSI Status Zero (SSTAT0) is set, the SIP bit in the Interrupt Status (ISTAT) is not set, and the IRQ/ pin is not asserted. See Section 2.6.3, "Fatal vs. Nonfatal Interrupts" for a list of the nonfatal interrupts.

If a fatal interrupt is masked and that condition occurs, then SCRIPTS still stops. The appropriate bit in the DMA Status (DSTAT) or SCSI Status Zero (SSTAT0) register is set, the SIP or DIP bits in the Interrupt Status (ISTAT) is set, and the IRQ/ pin is not asserted.

When the SYM53C710 is initialized, enable all fatal interrupts if hardware interrupts are being used. If a fatal interrupt is disabled and that interrupt condition occurs, SCRIPTS halts and the system never knows it unless it times out and checks the Interrupt Status (ISTAT) after a certain period of inactivity.

If ISTAT is being polled instead of using hardware interrupts, then masking a fatal interrupt makes no difference since the SIP and DIP bits in the Interrupt Status (ISTAT) inform the system of interrupts, not the IRQ/ pin.

Masking an interrupt after IRQ/ is asserted does not cause deassertion of IRQ/.

2.6.5 Stacked Interrupts

The SYM53C710 will stack interrupts, if they occur, one after the other. If the SIP or DIP bits in the Interrupt Status (ISTAT) register are set (first level), then there is already at least one pending interrupt, and any future interrupts are stacked in extra registers behind the SCSI Status Zero (SSTAT0) and DMA Status (DSTAT) registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts set additional bits in the extra registers behind SSTAT0 and DSTAT. When the first level of interrupts are cleared, all the interrupts that came in afterward move into the SSTAT0 and DSTAT. After the first interrupt is cleared by reading the appropriate register, the IRQ/ pin is deasserted for a set time as published in the product technical manual; the stacked interrupt(s) move into the SSTAT0 or DSTAT; and the IRQ/ pin is asserted once again.

Since a masked nonfatal interrupt does not set the SIP or DIP bits, interrupt stacking does not occur. A masked, nonfatal interrupt still posts the interrupt in SCSI Status Zero (SSTAT0) but does not assert the IRQ/ pin. Since no interrupt is generated, future interrupts move into the SCSI Status Zero (SSTAT0) instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked nonfatal interrupt is still set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which multiple interrupts can occur but are not stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or multiple SCSI and multiple DMA interrupts (both SIP and DIP set).

As previously mentioned, DMA interrupts do not attempt to flush the FIFOs before generating the interrupt. It is important to set either the Clear DMA and SCSI FIFOs (CLF) bit or the Flush DMA FIFO (FLF) bit

if a DMA interrupt occurs and the DMA FIFO Empty (DFE) bit is not set. This is because any future SCSI interrupts are not posted until the DMA FIFO is cleared of data. These 'locked out' SCSI interrupts are posted as soon as the DMA FIFO is empty.

2.6.6 Halting in an Orderly Fashion

When an interrupt occurs, the SYM53C710 attempts to halt in an orderly fashion.

- If the interrupt occurs in the middle of an instruction fetch, the fetch is completed, except in the case of a Bus Fault or Watchdog Time-out. Execution does not begin, but the DSP points to the next instruction since it is updated when the current SCRIPTS is fetched.
- If the DMA direction is a write to memory and a SCSI interrupt occurs, the SYM53C710 attempts to flush the DMA FIFO to memory before halting. Under any other circumstances only the current cycle is completed before halting, so the DFE bit in DMA Status (DSTAT) should be checked to see if any data remains in the DMA FIFO.
- SCSI REQ/ACK handshakes that have begun are completed before halting.
- The SYM53C710 attempts to clean up any outstanding synchronous offset before halting.
- In the case of Transfer Control Instructions, once instruction execution begins it continues to completion before halting.
- If the instruction is a JUMP/CALL WHEN <phase>, the DMA SCRIPTS Pointer (DSP) is updated to the transfer address before halting.
- All other instructions may halt before completion.

2.6.7 Sample Interrupt Service Routine

The following is a sample of an ISR for the SYM53C710. It can be repeated if polling is used, or should be called when the IRQ/ pin is asserted if hardware interrupts are used.

1. Read Interrupt Status (ISTAT).
2. If only the SIP bit is set, read SCSI Status Zero (SSTAT0) to clear the SCSI interrupt condition and get the SCSI interrupt status. The

bits in the SSTAT0 tell which SCSI interrupts occurred and determine what action is required to service the interrupts.

3. If only the DIP bit is set, read DMA Status (DSTAT) to clear the interrupt condition and get the DMA interrupt status. The bits in DSTAT tell which DMA interrupts occurred and determine what action is required to service the interrupts.
4. If both the SIP and DIP bits are set, read SCSI Status Zero (SSTAT0) and DMA Status (DSTAT) to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of SSTAT0 and DSTAT registers to clear interrupts, insert a 12 clock delay between the consecutive reads to ensure that the interrupts clear properly. Both the SCSI and DMA interrupt conditions should be handled before leaving the ISR. It is recommended that the DMA interrupt be serviced before the SCSI interrupt, because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.
5. When using polled interrupts go back to Step 1 before leaving the ISR in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin is asserted again if there are any stacked interrupts. This should cause the system to re-enter the ISR.

2.7 SCSI Bus Interface

The SYM53C710 can be used in both SE and differential applications.

In SE mode, all SCSI signals are active low. The SYM53C710 contains open drain output drivers that can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered down SYM53C710 has no effect on an active SCSI bus (CMOS “voltage feed-through” phenomenon). Additionally, signal filtering is present at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

In Differential Mode, the SDIR [7:0], SDIRP, IGS, TGS, RSTDIR, BSYDIR, and SELDIR signals control the direction of external differential pair transceivers. See Figure 2.9 for the suggested differential wiring diagram. Please refer to Appendix D for more information. The wiring diagram shows five 75ALS170 3-channel transceivers and one 75ALS171 3-channel transceiver, though other single and multichannel

devices may be used (DS36954 4-channel transceiver, for instance). The suggested value for the 15 pull-up resistors in the diagram is 680 Ω. If Active Negation is enabled and the chip is operating in differential mode, the value of the pull-up resistors should be 1.5 KΩ. Refer to Appendix D for other differential interface options.

2.7.1 Terminator Networks

The terminator networks provide the biasing needed to pull signals to an inactive voltage level, and are required for both SE and differential applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends. No system should ever have more or less than two sets of terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. There should be a means of disabling the termination.

SE cables can use a 220 Ω pull-up resistor to the termination power supply (Term Power) line and a 330 Ω pull-down resistor to ground. Differential cables use a 330 Ω pull-up resistor from "– SIG" to Term Power, a 330 Ω pull-down resistor from "+ SIG" to ground, and a 150 Ω resistor from "– SIG" to "+ SIG".

Because of the high-performance nature of the SYM53C710, Alternative Two SE termination is recommended. This method employs a 2.85 V regulator and 110 Ω pull-up resistors (no pull-down). Figure 2.10 and Figure 2.11 show two examples of schematics for Alternative Two termination. For more information on Alternative Two termination, refer to the SCSI-2 specification.

2.7.2 Select/Reselect During Selection/Reselection

In multithreaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select one target and is reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection.

The SYM53C710 can handle this condition in a manner identical to the SYM53C700, that is, autoswitching between initiator and target modes, but the recommended method is to disable the autoswitching utility.

When autoswitching is enabled, regardless of the current operating mode (initiator or target), if the SYM53C710 becomes reselected while executing a Select/Reselect instruction, then it autoswitches to initiator mode. Similarly, if the SYM53C710 becomes selected while executing a Select/Reselect instruction, it autoswitches to target mode.

After the automatic mode switch, the SYM53C710 fetches the next instruction from the alternate address, pointed to by the DMA Next Data Address (DNAD) register (the second 32-bit word of the Select/Reselect instruction).

The recommended method of handling Selection/Reselection during Selection/Reselection is to disable autoswitching and put a Set Target instruction at the start of the target SCRIPTS (before the Wait Select code).

2.7.3 Synchronous Operation

The SYM53C710 can transfer synchronous SCSI data in both initiator and target modes. The SCSI Transfer (SXFER) register controls both the synchronous offset and the transfer period. It may be loaded by the CPU before SCRIPTS execution begins, or from within SCRIPTS using a Table Indirect I/O instruction.

The SYM53C710 can receive data at a synchronous transfer period of 100/200 ns (SCSI-2/SCSI-1), regardless of the transfer period used to send data. Therefore, when negotiating for synchronous data transfers, the suggested transfer period is 100/200 ns. Depending on the SCLK frequency, the SYM53C710 can send synchronous data at intervals as short as 100/200 ns.

Figure 2.9 Differential Wiring Diagram

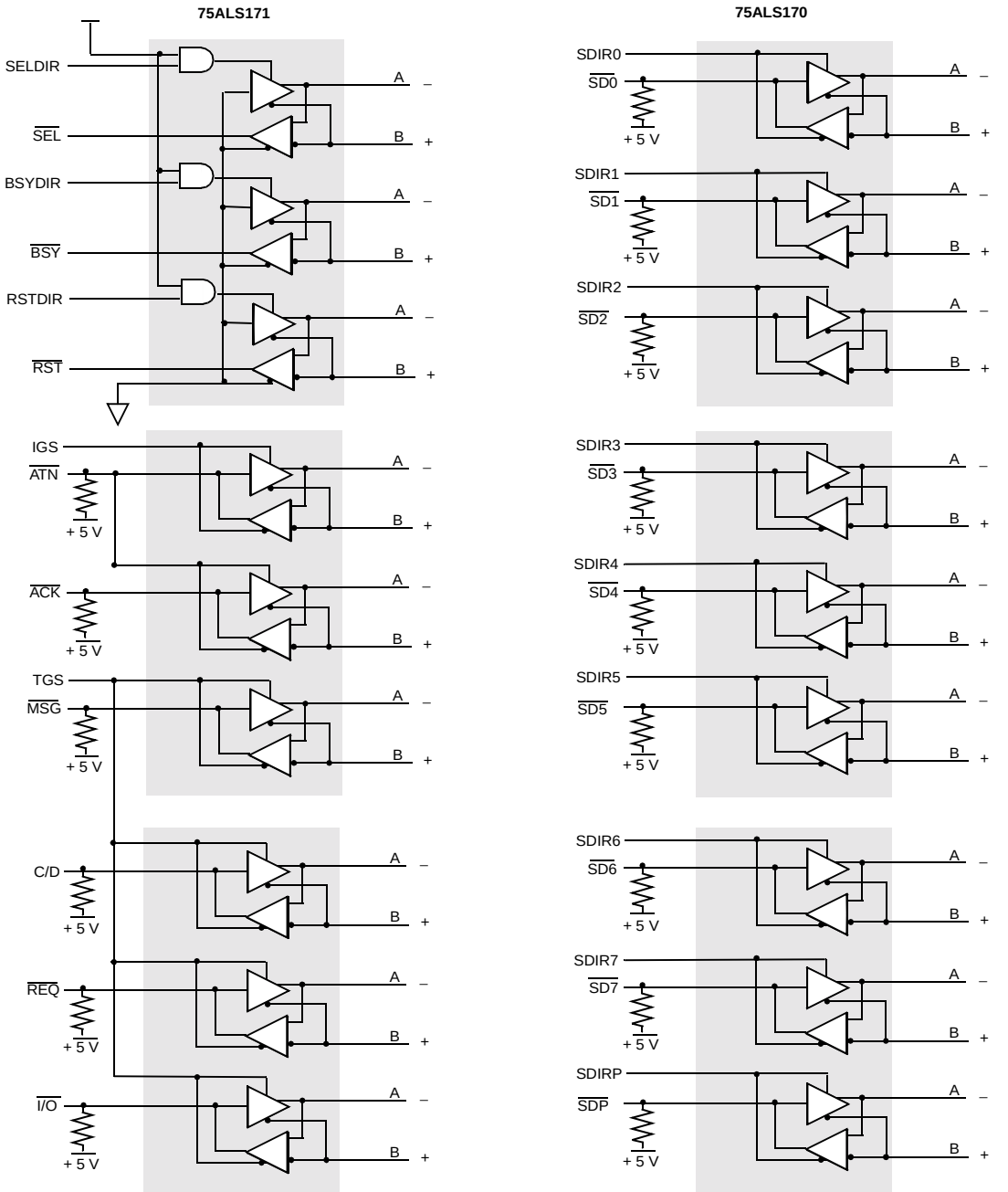
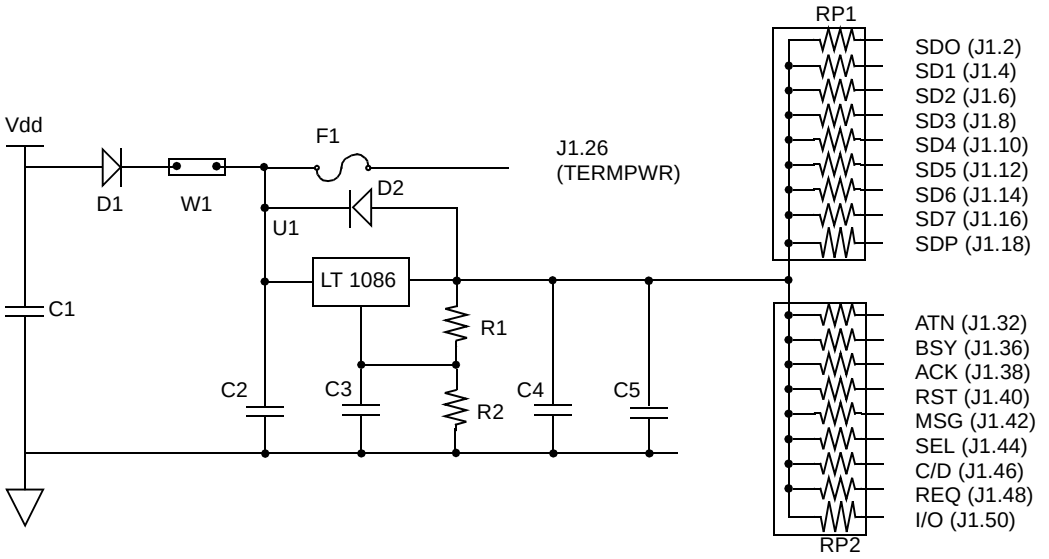


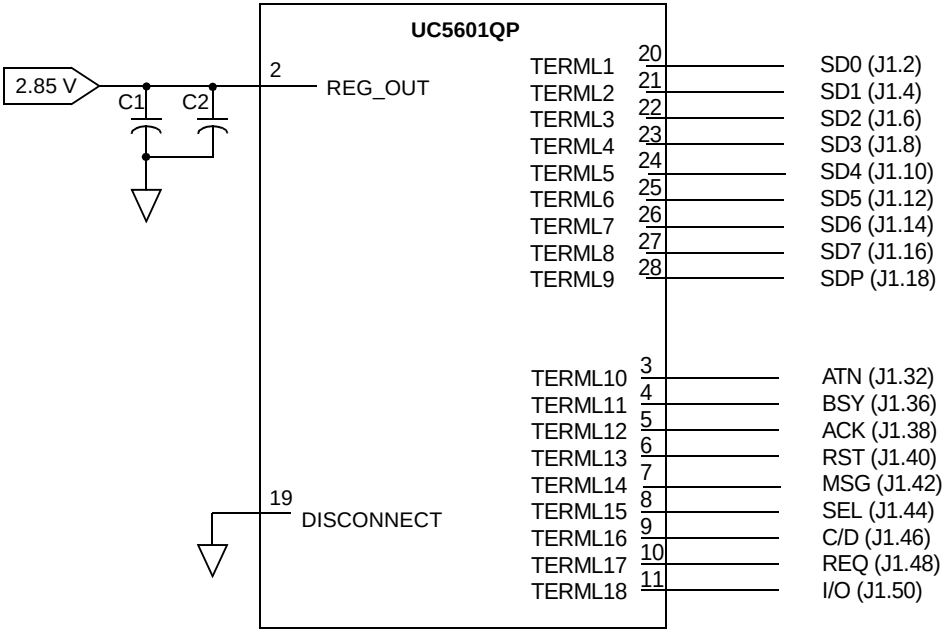
Figure 2.10 Alternative Two Termination (Example 1)



Note:

- C1 = 47 µF tantalum, SMT
- C2, C3 = 1.0 µF tantalum, SMT
- C4 = 2.2 µF tantalum, SMT
- C5 = 0.1 µF ceramic, SMT
- D1, D2 = Schottky diode, 1N5817
- F1 = 1.5 Amp fuse, socketed, 2AG
- J1 = 50-pin dual row header, male SCSI connector
- RP1, RP2 = 110 Ω x 9 pull-ups, 1% SIP-10
- U1 = Voltage Regulator LT 1086, TO-39
- W1 = 2 position jumper

Figure 2.11 Alternative Two Termination (Example 2)



Note:

- C1 = 10 µF tantalum, SMT
- C2 = 0.1 µF ceramic, SMT
- J1 = 50-pin dual row header, male SCSI connector

Chapter 3
Signal Descriptions

The SYM53C710 host bus can operate in one of two modes: Bus Mode 1 (asynchronous) and Bus Mode 2 (synchronous). The bus mode is selected with the Bus Select pin. The signal types are abbreviated as follows: “I” for input, “O” for output, and “Z” for high impedance. A slash (“/”) indicates an active low signal. Refer to the Section 6.1, “DC Characteristics” for specific pin type (3-state, open drain, etc.) and current drive capabilities.

Figure 3.1 SYM53C710 Pin Configuration

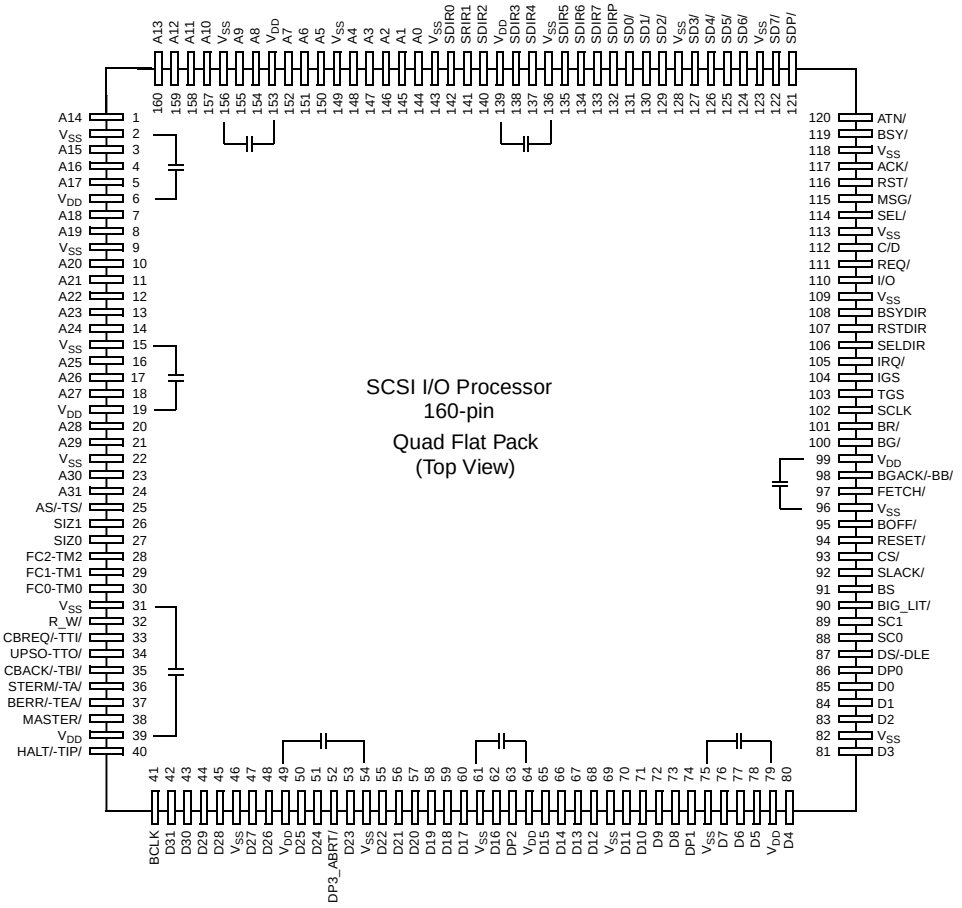


Table 3.1 Interface Signals

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description (Slave Type, Master Type)
D[31:0]	D[31:0]	I/O	I/O	**Host Data Bus**. Main 32-bit data path into host memory.
DP[3:0]	DP[3:0]	I/O	I/O	**Host Bus Data Parity**. DP0 provides parity for D[7:0], DP1 for D[15:8], etc. Parity is valid on all byte lanes, including unused lanes. When the parity through mode is disabled, DP3 becomes a hardware abort input (ABRT/).
DS/	DLE	Z I	O I	**Data Strobe, Data Latch Enable**. DS/: In Bus Mode 1, this signal indicates that a valid data has been or should be placed on the data lines. DLE: Latches read data into the SYM53C710 when operating in Bus Mode 2. Data latches are transparent when DLE is high. This signal is used to address host memory and internal registers. This signal should be pulled high if not used.
A[31:0]	A[31:0]	I	O	**Address Bus**. These signals provide an address bus to the host memory.
AS/	TS/	I	O	**Address Strobe, Transfer Start.** AS/: In Bus Mode 1, this signal indicates that a valid address is on A[31:0]. TS/: In Bus Mode 2, transfer start indicates that a bus cycle is starting and all of the status and address lines are valid.
R_W/	R_W/	I	O	**Read/Write**. Indicates the direction of the data transfer relative to the current master.
SIZ[1:0]	SIZ[1:0]	I	O	**Transfer Size**. Indicates the current transfer width. 00 - Longword (4 bytes) 01 - Byte (1 byte) 10 - Word 11 - Bus Mode 1: Illegal in slave mode, will not occur in master Bus Mode 2: Cache Line Burst

Table 3.1 Interface Signals (Cont.)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description (Slave Type, Master Type)
STERM/	TA/	I/O	I	**Synchronous Cycle Termination, Transfer Acknowledge**. STERM/: Acknowledges transfer to a 32-bit wide port. When the EA bit in the DMA Control (DCNTL) is set, this signal becomes bidirectional: input in master mode and output in slave mode. TA/: Acknowledges transfer to a 32-bit wide port. When the EA bit in the DMA Control (DCNTL) is set, this signal becomes bidirectional: input in master mode and output in slave mode.
BERR/	TEA/	O	I	**Bus Error Acknowledge, Transfer Error Acknowledge.** BERR/: Indicates that a bus fault has occurred. May be used with HALT/ to force a bus retry. TEA/: Indicates that a bus fault has occurred.
HALT/	TIP/	Z Z	I O	**Halt, Transfer in Progress.** HALT/: Input only, used with BERR/ to indicate a bus retry cycle. TIP/: Bidirectional, indicates that bus activity is in progress.
SLACK/	SLACK/	O	O	**Slave Acknowledge**. When asserted, indicates the internal end of a slave mode cycle. The external slave cycle ends when the SYM53C710 observes either STERM/_TA/ or BERR/-TEA/.
FC[2:0]	TM[2:0]	Z	O	**Function Codes, Transfer Modifiers.** Indicates the status of the current bus cycle. FC0, TM0 = 1: Indicates data space; it is the default for all transfers FC0, TM0 = 0: Indicates program space. It may be optionally selected when setting the PD bit in the DMA Mode (DMODE) register FC1, TM1: User definable from the DMODE register bits FC2, TM2: User definable from the DMODE register bits
SC[1:0]	SC[1:0]	Z(O)	O	**Snoop Control**. Indicates the bus snooping level. The bits are user programmable through bits in the Chip Test Seven (CTEST7) register. They are asserted when the SYM53C710 is the bus master. (SC[1:0] may optionally be used as pure outputs, active in both master and slave modes. See the Chip Test Eight (CTEST8) register description for use of SC[1:0] as pure outputs.)
MASTER/	MASTER/	O	O	**Master Status**. Driven low when the SYM53C710 becomes bus master.

Table 3.1 Interface Signals (Cont.)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description (Slave Type, Master Type)
FETCH/	FETCH/	O	O	**Fetching Opcode**. Indicates that the next bus request will be for an opcode fetch.
BR/	BR/	O	O	**Bus Request**. Indicates that there is a request to use the host bus.
BG/	BG/	I	I	**Bus Grant**. Indicates that the host bus has been granted to the SYM53C710.
BGACK/	BB/	Z	I/O	**Bus Grant Acknowledge, Bus Busy (can be wired-OR).** BGACK/: In Bus Mode 1, this signal indicates that the SYM53C710 or another device has taken control of the host bus signals. BB/: In Bus Mode 2, this signal indicates that the SYM53C710 or another device has taken control of the host bus signals.
BOFF/	BOFF/	I	I	**Back Off**. Forces the SYM53C710 to relinquish bus mastership at the end of the current cycle, if the proper setup timing requirements are met. When BOFF is deasserted, a new arbitration cycle will occur and bus cycles will resume.
BCLK	BCLK	I	I	**Bus Clock**. This clock controls all host related activity.
RESET/	RESET/	I	I	**Chip Reset**. Forces a full chip reset.
CS/	CS/	I	I	**Chip Select**. Selects the SYM53C710 as a slave I/O Device. When CS/ is detected: Bus Mode 1: CBACK/ is deasserted Bus Mode 2: TBI/ is asserted
IRQ/	IRQ/	O	O	**Interrupt.** Indicates that service is required from the host CPU.
UPSO	TT0/	Z	O	**User Programmable Status, Transfer Type Zero.** UPSO: General purpose line. The value in a DMA Mode (DMODE) register bit is asserted while the chip is a bus master. TT0: Indicates the current bus transfer type. This bit can be programmed from a register bit (default = 0). It is asserted only when the SYM53C710 is bus master.

Table 3.1 Interface Signals (Cont.)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description (Slave Type, Master Type)
CBREQ/	TT1/	Z	O	**Cache Burst Request, Transfer Type Bit 1**. CBREQ/: In Bus Mode 1, Cache Burst Request indicates an attempt to execute a line transfer of four longwords. TT1/: In Bus Mode 2, Transfer Type Bit 1, output line indicates the current bus transfer type. This bit can be programmed from a Chip Test Seven (CTEST7) register bit (default = 1). It is only asserted when the SYM53C710 is bus master.
CBACK/	TBI/	O	I	**Cache Burst Acknowledge, Transfer Burst Inhibit**. CBACK/: In Bus Mode 1, this signal indicates that the memory can handle a burst request. In slave mode this signal is deasserted in response to CS/. TBI/: In Bus Mode 2, Transfer Burst Inhibit indicates that the memory cannot currently handle a burst request. In slave mode this signal is asserted in response to CS/.
BS	BS	I	I	**Bus Mode Select**. Selects between asynchronous and synchronous host bus modes. BS = 0: Bus Mode 2 (68040-like) host bus mode BS = 1: Bus Mode 1 (68030-like) host bus mode
BIG_LIT/	BIG_LIT/	I	I	**Big/Little Endian Select**. Selects the byte order interpretation of data transferred between the HOST and SCSI bus. It also affects how the register set is addressed. BIG_LIT/ = 0: Little endian byte order BIG_LIT/ = 1: Big endian byte order
SCLK	SCLK	I	I	**SCSI Clock**. SCLK is used to derive all SCSI related timings. The speed of this clock will be determined by the application's requirements; in some applications SCLK and BCLK may be tied to the same source.
SD[7:0]	SDP/	I/O	I/O	**SCSI Data**. SD/[7:0]: 8-bit SCSI data bus SDP/: SCSI data parity bit

Table 3.1 Interface Signals (Cont.)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description (Slave Type, Master Type)
SCTRL/	SCTRL/	I/O	I/O	**SCSI Control**. CD/ SCSI phase line, command/data IO/ SCSI phase line, input/output MSG/ SCSI phase line, message REQ/ Data handshake signal from target device ACK/ Data handshake signal from initiator device ATN/ SCSI bus attention signal BSY/[1] SCSI bus arbitration signal, signal busy SEL/[1] SCSI bus arbitration signal, select device RST/[1] SCSI bus reset
SDIR[7:0]	SDIR[7:0]	O	O	**Differential Support Lines**. Driver direction control for SCSI data lines.
SDIRP	SDIRP	O	O	**Differential Support Line**. Driver direction control for SCSI parity signal.
BSYDIR	BSYDIR	O	O	**Differential Support Line**. Driver enable control for SCSI BSY/ signal.
SELDIR	SELDIR	O	O	**Differential Support Line**. Driver enable control for SCSI SEL/ signal.
RSTDIR	RSTDIR	O	O	**Differential Support Line**. Driver enable control for SCSI RST/ signal.
IGS	IGS	O	O	**Differential Support Line**. Direction control for initiator driver group.
TGS	TGS	O	O	**Differential Support Line**. Direction control for target driver group.

1. Input only in Differential Mode.

Chapter 4
Registers

Throughout this chapter, registers are referenced by their little endian addresses, with big endian addresses in parentheses. The term “set” is used to refer to bits that are programmed to a binary one. Similarly, the terms “clear” and “reset” are used to refer to bits that are programmed to a binary zero. Reserved bits are designated as “R” in each register diagram. These bits should always be written to zero; mask all information read from them. Unless otherwise indicated, all bits in registers are active high, the feature is enabled by setting the bit.

4.1 Register Descriptions

The bottom line of every register diagram shows the default register values after the chip is powered-up or reset. In the default lines below each diagram, a value of 1 indicates that the bit it set; a value of 0 indicates that the bit is clear; and a value of X indicates that the default is indeterminate or is a don’t care.

Warning: The only register that the host CPU can access while the SYM53C710 is executing SCRIPTS is the Interrupt Status (ISTAT) register; attempts to access other registers will interfere with the operation of the chip. All registers are accessible using SCRIPTS.

Table 4.1 Register Address Map

31	16	15	0	
SIEN	SDID	SCNTL1	SCNTL0	0x00
SOCL	SODL	SXFER	SCID	0x04
SBCL	SBDL	SIDL	SFBR	0x08
SSTAT2	SSTAT1	SSTAT0	DSTAT	0x0C
DSA				0x10
CTEST3	CTEST2	CTEST1	CTEST0	0x14
CTEST7	CTEST6	CTEST5	CTEST4	0x18
TEMP				0x1C
LCRC	CTEST8	ISTAT	DFIFO	0x20
DCMD	DBC			0x24
DNAD				0x28
DSP				0x2C
DSPS				0x30
SCRATCH				0x34
DCNTL	DWT	DIEN	DMODE	0x38
ADDER				0x3C

Register: 0x00 (0x03)
SCSI Control Zero (SCNTL0)
Read/Write

7	6	5	4	3	2	1	0
ARB[1:0]		START	WATN	EPC	EPG	AAP	TRG
1	1	0	0	0	0	0	0

ARB[1:0] Arbitration Mode Bits 1 and 0 [7:6]

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection/reselection

Simple Arbitration

1. The SYM53C710 waits for a bus free condition to occur.
2. It asserts BSY/ and its SCSI ID (contained in the SCSI Chip ID (SCID) register) onto the SCSI bus. If the SEL/ signal is asserted by another SCSI device, the SYM53C710 deasserts BSY/, deasserts its ID and sets the Lost Arbitration bit in the SCSI Status One (SSTAT1) register.
3. After an arbitration delay, the CPU reads the SCSI Bus Data Lines (SBDL) register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the SYM53C710 wins arbitration.
4. Once the SYM53C710 wins arbitration, SEL is asserted using the SCSI Output Control Latch (SOCL) for a bus clear plus a bus settle delay (1.2 µs) before a low level selection is performed.

Full Arbitration, Selection/Reselection

1. The SYM53C710 waits for a bus free condition to occur.
2. It asserts BSY/ and its SCSI ID (the highest priority ID stored in the SCSI Chip ID (SCID) register) onto the SCSI bus.
3. If the SEL/ signal is asserted by another SCSI device or if the SYM53C710 detects a higher priority ID, the SYM53C710 deasserts BSY/, deasserts its ID, and waits until the next bus free state to try arbitration again.
4. The SYM53C710 repeats arbitration until it wins control of the SCSI bus. When it wins, the Won Arbitration bit is set in the SCSI Status One (SSTAT1) register.
5. The SYM53C710 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SCSI Destination ID (SDID) register) and the SYM53C710's ID (the highest priority ID stored in the SCSI Chip ID (SCID) register).
6. After a selection is complete, the Function Complete bit is set in the SCSI Status Zero (SSTAT0) register.
7. If a selection time-out occurs, the Selection Time-out bit is set in the SCSI Status Zero (SSTAT0) register.

START **Start Sequence** **5**

When this bit is set, the SYM53C710 starts the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is accessed directly in low level mode; during SCSI SCRIPTS operations, this bit is controlled by the SCRIPTS processor. Do not start an arbitration sequence if the connected (CON) bit in the SCSI Control One (SCNTL1) register indicates the SYM53C710 is already connected to the SCSI bus. This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, check the connected bit in the SCSI Control One (SCNTL1) register to verify that the SYM53C710 is not connected to the SCSI bus.

WATN **Select with ATN/ on a Start Sequence** **4**

When this bit is set, the SCSI ATN/ signal is asserted during the selection phase (ATN/ is asserted at the same time BSY/ is deasserted while selecting a target). If a selection time-out occurs while attempting to select a target device, ATN/ is deasserted at the same time SEL/ is deasserted. When this bit is cleared, the ATN/ signal is not asserted during selection. When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but manual setting is possible in low level mode.

EPC **Enable Parity Checking** **3**

When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. The host data bus is checked for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SCSI Output Data Latch (SODL) register when sending SCSI data in either initiator or target mode. If a parity error is detected, bit 0 of the SCSI Status Zero (SSTAT0) register is set and an interrupt may be generated.

If the SYM53C710 is operating in initiator mode and a parity error is detected, assertion of ATN/ is optional, but the transfer continues until the target changes phase. When this bit is cleared, parity errors are not reported.

EPG **Enable Parity Generation/Parity Through** **2**

When this bit is set, the SCSI parity bit is generated by the SYM53C710. The host data bus parity lines DP[3:0] are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines flow through the SYM53C710 internal FIFOs and are driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus). This bit is set to enable the DP3_ABRT/ pin to function as an abort input (ABRT/).

AAP **Assert ATN/ on Parity Error** **1**

When this bit is set, the SYM53C710 automatically asserts the SCSI ATN/ signal upon detection of a parity error. ATN/ is only asserted in initiator mode. The ATN/

signal is asserted before deasserting ACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the SYM53C710 to assert ATN/ in this manner. The following parity errors can occur:

- A parity error detected on data received from the SCSI bus.
- A parity error detected on data transferred to the SYM53C710 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ is not automatically asserted on the SCSI bus when a parity error is received.

TRG **Target Mode** **0**

This bit determines the default operating mode of the SYM53C710, though there are instances when the chip may act in a role other than the default. For example, a mostly initiator device may be selected as a target. An automatic mode change does not affect the state of this bit. After completion of a mode change I/O operation, the SYM53C710 returns to the role defined by this bit. When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the SYM53C710 is an initiator device by default.

Register: 0x01 (0x02)

SCSI Control One (SCNTL1)

Read/Write

7	6	5	4	3	2	1	0
EXC	ADB	ESR	CON	RST	AESP	SND	RCV
0	0	0	0	0	0	0	0

EXC **Extra Clock Cycle of Data Setup** **7**

When this bit is set, an extra clock period of data setup is added to each SCSI data transfer. The extra data setup time can provide additional system design flexibility, though it affects the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

ADB **Assert SCSI Data Bus** **6**

When this bit is set, the SYM53C710 drives the contents of the SCSI Output Data Latch (SODL) register onto the SCSI data bus. When the SYM53C710 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. When the SYM53C710 is a target, the SCSI I/O signal must be active to assert the SODL contents onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the SYM53C710 is connected to the SCSI bus. Clear this bit when executing SCSI SCRIPTS. It is normally used only for diagnostic testing or operation in low level mode.

ESR **Enable Selection and Reselection** **5**

When this bit is set, the SYM53C710 responds to bus initiated selections and reselections. The SYM53C710 can respond to selections and reselections in both initiator and target roles. If SCSI Disconnect/Reconnect is to be supported, set this bit as part of the initialization routine. This bit is cleared after Disconnect/Reselection.

CON **Connected** **4**

This bit is automatically set any time the SYM53C710 is connected to the SCSI bus as an initiator or as a target. It is set after the SYM53C710 successfully completes arbitration or when it responds to a bus initiated selection or reselection. This bit is also set after the chip wins simple arbitration when operating in low level mode. When this bit is cleared, the SYM53C710 is not connected to the SCSI bus. This bit is automatically cleared when Bus Free phase is detected.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature is used primarily during loopback mode.

RST **Assert SCSI RST/ Signal** **3**

Setting this bit asserts the RST/ signal. The RST/ signal remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPTS delay routine. The RST/ signal asserts within 40 clocks and generates an interrupt if enabled in SCSI Interrupt Enable (SIEN).

AESP **Assert Even SCSI Parity (force bad parity)** **2**

When this bit is set and the Enable Parity Generation bit is set in the SCSI Control Zero (SCNTL0) register, the SYM53C710 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the chip. If parity checking is enabled, then the SYM53C710 checks data received for odd parity. This bit is used for diagnostic testing and is cleared during normal operation. It is useful to generate parity errors to test error handling functions.

SND **Start SCSI Send** **1**

Setting this bit to 1 initiates a SCSI send operation. Bytes in the DMA FIFO (DFIFO) are sent across the SCSI bus. It is automatically set to 1 by the SCRIPTS processor to start a SCSI send operation when executing SCSI SCRIPTS. Use it for register level programming to low level mode.

RCV **Start SCSI Receive** **0**

Setting this bit to 1 initiates a SCSI receive operation. Bytes are received from the SCSI bus into the DMA FIFO (DFIFO) (using the SCSI FIFO, if synchronous). It is automatically set to 1 by the SCRIPTS processor to start a SCSI receive operation when executing SCSI SCRIPTS. Use it for register level programming to low level mode.

Register: 0x02 (0x01)

SCSI Destination ID (SDID)

Read/Write

7							0
ID[7:0]							
0	0	0	0	0	0	0	0

ID[7:0] **SCSI Destination ID** **[7:0]**

This register sets the SCSI ID of the device to be selected when a select or reselect command is executed. Only one of these bits should be set for proper selection or reselection. When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS Select or Reselect instruction.

Note: When using Table Indirect I/O commands, the destination ID is loaded from the data structure.

Register: 0x03 (0x00)

SCSI Interrupt Enable (SIEN)

Read/Write

7	6	5	4	3	2	1	0
M/A	FCMP	STO	SEL	SGE	UDC	RST/	PAR
0	0	0	0	0	0	0	0

M/A **Initiator: Phase Mismatch, or Target: ATN/ Active** **7**

FCMP **Function Complete** **6**

STO **SCSI Bus Time-out** **5**

SEL **Selected or Reselected** **4**

SGE **SCSI Gross Error** **3**

UDC **Unexpected Disconnect** **2**

RST/ **SCSI RST/ Received** **1**

PAR **Parity Error** **0**

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SCSI Status Zero (SSTAT0) register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit is still set in the SCSI Status Zero (SSTAT0) register. Masking an interrupt does not prevent setting the ISTAT SIP bit, except in the case of nonfatal interrupts (SEL and FCMP). Setting a mask bit enables the assertion of IRQ/, for the corresponding interrupt. (A masked nonfatal interrupt does not prevent unmasked or fatal interrupts from getting through; interrupt stacking begins when either the ISTAT SIP or DIP bit is set.)

The SYM53C710 IRQ/ output is latched. Once asserted, it remains asserted until the interrupt is cleared by reading the appropriate status register. Masking an

interrupt after the IRQ/ output is asserted does not cause deassertion of IRQ/. In the case of nonfatal interrupts, masking an interrupt after it occurs causes the ISTAT SIP bit to clear and allows pending interrupts to fall through (interrupt stacking is disabled).

Note: See Chapter 2, "Functional Description" for a more detailed description of interrupts.

Register: 0x04 (0x07)

SCSI Chip ID (SCID)

Read/Write

7							0
ID[7:0]							
0	0	0	0	0	0	0	0

ID[7:0] **SCSI Chip ID** **[7:0]**

This register sets up the SYM53C710 SCSI ID. If more than one bit is set, the SYM53C710 responds to each corresponding SCSI ID. The SYM53C710 always uses the highest priority SCSI ID during arbitration. For example, if 0x84 is written to this register, the SYM53C710 responds when another device selects ID 7 or ID 2. When arbitrating for the SCSI bus, use ID 7 as the SYM53C710 SCSI ID.

Note: If no bits are set and simple arbitration is performed, the SYM53C710 arbitrates as described under the SCSI Control Zero (SCNTL0) section with no SCSI ID output onto the SCSI bus.

Register: 0x05 (0x06)

SCSI Transfer (SXFER)

Read/Write

7	6		4	3			0
DHP	TP[2:0]			MO[3:0]			
0	0	0	0	0	0	0	0

Note: When using Table Indirect I/O commands, this register is loaded from the I/O data structure.

DHP **Disable Halt on Parity Error or ATN/** **7**

When this bit is cleared, the SYM53C710 halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the SYM53C710 may transfer up to three additional bytes before halting to synchronize between internal core cells. During synchronous operation, the SYM53C710 transfers data until there are no outstanding synchronous offsets. If the SYM53C710 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. When data is sent in target mode with pass parity enabled, the byte with the parity error is not sent across the SCSI bus.

When this bit is set, the SYM53C710 does not halt the SCSI transfer when a parity error is received until the end of a Block Move operation. When this bit is set and the initiator asserts ATN/, the SYM53C710 completes the Block Move and then, depending on whether or not the ATN/ interrupt is enabled, either generate an interrupt or continue fetching instructions (the instruction following this is a JUMP address, IF ATN).

TP[2:0] **SCSI Synchronous Transfer Period** **[6:4]**

These bits determine the SCSI synchronous transfer period (XFERP) used by the SYM53C710 when sending synchronous SCSI data in either initiator or target mode. These bits control the possible combinations and their relationship to the synchronous data transfer period used by the SYM53C710.

TP2	TP1	TP0	XFERP
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The synchronous transfer period the SYM53C710 uses when transferring SCSI data is determined in the following equations. Table 4.2 and Table 4.3 show examples of possible bit combinations.

Formula:

The minimum synchronous transfer period when sending SCSI data:

Period = TCP * (4 + XFERP + 1)

If bit 7 in the SCSI Control One (SCNTL1) register is set (one extra clock cycle of data setup)

Period = TCP * (4 + XFERP)

If bit 7 in the SCSI Control One (SCNTL1) register is clear (no extra clock cycle of data setup)

The minimum synchronous transfer period when receiving SCSI data:

Period = TCP * (4 + XFERP)

Whether sending or receiving, TCP = 1 / SCSI core clock frequency. The SCSI core clock frequency is determined by the CF[1:0] bits in the DMA Control (DCNTL) register and SSCF[1:0] bits in SCSI Bus Control Lines (SBCL).

Table 4.2 Examples of Synchronous Transfer Periods and Rates for SCSI-1

CLK (MHz)	SCSI CLK/DCNTL bits [7:6]	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (Mbytes/s)
66.67	/3	0	180	5.55
66.67	/3	1	225	4.44
50	/2	0	160	6.25
50	/2	1	200	5
40	/2	0	200	5
37.50	/1.5	0	160	6.25
33.33	/1.5	0	180	5.55
25	/1	0	160	6.25
20	/1	0	200	5
16.67	/1	0	240	4.17

Table 4.3 Examples of Transfer Periods and Rates for Fast SCSI-2

CLK (MHz)	SCSI CLK/SBCL bits [1:0]	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (Mbytes/s)
66.67	/1.5	0	90	11.11[1]
66.67	/1.5	1	112.5	8.88
50	/1	0	80	12.5[1]
50	/1	1	100	10.0
40	/1	0	100	10.0
37.50	/1	0	106.67	9.375
33	/1	0	120	8.33
25	/1	0	160	6.25
20	/1	0	200	5
16.67	/1	0	240	4.17

1. Violates SCSI specifications.

MO[3:0] **Max SCSI Synchronous Offset** **[3:0]**

These bits describe the maximum SCSI synchronous offset used by the SYM53C710 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the SYM53C710. These bits determine the SYM53C710 method of transfer for Data-In and Data-Out phases only; all other information transfers will occur asynchronously.

Register: 0x06 (0x05)

SCSI Output Data Latch (SODL)

Read/Write

7							0
SDB[7:0]							
0	0	0	0	0	0	0	0

SDB[7:0] **SCSI Output Data Latch** **[7:0]**

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCSI Control One (SCNTL1) register. This register is used to send data using programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip.

Register: 0x07 (0x04)

SCSI Output Control Latch (SOCL)

Read/Write

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
0	0	0	0	0	0	0	0

REQ **Assert SCSI REQ/ Signal** **7**

ACK **Assert SCSI ACK/ Signal** **6**

BSY **Assert SCSI BSY/ Signal** **5**

SEL	**Assert SCSI SEL/ Signal**	**4**
ATN	**Assert SCSI ATN/ Signal**	**3**
MSG	**Assert SCSI MSG/ Signal**	**2**
C/D	**Assert SCSI C/D Signal**	**1**
I/O	**Assert SCSI I/O Signal**	**0**

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SCSI Output Control Latch (SOCL) should only be used when transferring data using programmed I/O. Some bits are set or reset when executing SCSI SCRIPTS. Do not write to the register once the SYM53C710 becomes connected and starts executing SCSI SCRIPTS.

The contents of this register are only output if the CON bit in the SCSI Control One (SCNTL1) register is set. The REQ, BSY, SEL, MSG, C/D and I/O signals are only driven while in Target role, and the ACK and ATN signals are only driven while in initiator role.

Register: 0x08 (0x0B)

SCSI First Byte Received (SFBR)

Read/Write

7							0
1B[7:0]							
0	0	0	0	0	0	0	0

1B[7:0]	**First Byte Received**	**[7:0]**

This register contains the first byte received in any asynchronous information transfer phase. For example, when the SYM53C710 is operating in initiator mode, this register contains the first byte received in Message-In, Status Phase, Reserved In and Data-In.

When a Block Move instruction is executed for a particular phase, the first byte received is stored in this register – even if the present phase is the same as the last phase. The first byte received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SCSI First Byte Received (SFBR) as the destination. This allows bit testing after an operation.

Additionally, the SCSI First Byte Received (SFBR) register may be used to contain the device ID after a selection or reselection, if the COM bit is cleared in the DMA Control (DCNTL) register. However, for maximum flexibility it is strongly recommended that the ID byte be directed only to the Longitudinal Parity (LCRC) register (COM bit set).

The SCSI First Byte Received (SFBR) is not writable using the CPU, and therefore not by a Memory Move. However, it can be loaded using Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate SYM53C710 register (such as the Scratch (SCRATCH) register), and then to the SFBR.

Register: 0x09 (0x0A)

SCSI Input Data Latch (SIDL)

Read Only

7							0
SDB[7:0]							
0	0	0	0	0	0	0	0

SDB[7:0] **SCSI Input Data Latch** **[7:0]**

This register is used primarily for diagnostic testing, programmed I/O operation, or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SCSI Output Data Latch (SODL) register and then read back into the SYM53C710 by reading this register to allow loopback testing. When receiving SCSI data, the data flows into this register and out to the host FIFO. This register differs from the SCSI Bus Data Lines (SBDL) register; this register contains latched data and the SCSI Bus Data Lines (SBDL) always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and causes a parity error interrupt if the data is not valid.

Register: 0x0A

SCSI Bus Data Lines (SBDL)
Read Only

7							0
SDB[7:0]							
x	x	x	x	x	x	x	x

SDB[7:0] **SCSI Bus Data** **[7:0]**

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data using programmed I/O. This register can also be used for diagnostic testing or in low level mode.

Register: 0x0B (0x08)

SCSI Bus Control Lines (SBCL)
Read/Write

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
x	x	x	x	x	x	x	x

REQ **REQ/ Status** **7**

ACK **ACK/ Status** **6**

BSY **BSY/ Status** **5**

SEL **SEL/ Status** **4**

ATN **ATN/ Status** **3**

MSG **MSG/ Status** **2**

C/D **C/D Status** **1**

I/O **I/O Status** **0**

This register returns the SCSI control line status. A bit is set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is

read. This register is used for diagnostic testing or operation in low level mode.

Writing to bits [7:2] has no effect.

Table 4.4 Synchronous SCSI Clock Control Bits

SSCF1	SSCF0	Synchronous CLK
0	0	Set by DCNTL
0	1	SCLK / 1.0
1	0	SCLK/ 1.5
1	1	SCLK / 2.0

These bits determine the clock prescale factor used by the synchronous portion of the SCSI core. The default is to use the same clock prescale factor as the asynchronous logic (set by CF[1:0] in DMA Control (DCNTL)). Setting one or both of these bits allows the synchronous logic to run at a different speed than the asynchronous logic. This is necessary for fast SCSI-2. Refer to Appendix D for more information.

Register: 0x0C (0x0F)

DMA Status (DSTAT)

Read Only

7	6	5	4	3	2	1	0
DFE	R	BF	ABRT	SSI	SIR	WTD	IID
1	0	0	0	0	0	0	0

Reading this register clears any bits that are set at the time the register is read, but does not necessarily clear the register because additional interrupts may be pending (the SYM53C710 stacks interrupts). It is possible to mask DMA interrupt conditions individually through the DMA Interrupt Enable (DIEN) register.

When performing consecutive 8-bit reads of the DMA Status (DSTAT) and SCSI Status Zero (SSTAT0) registers (in either order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading both registers when both the ISTAT SIP and DIP bits may not be set, the SCSI Status Zero (SSTAT0) register should be read before the DMA Status (DSTAT) register to avoid

missing a SCSI interrupt. Both concerns are avoided if the registers are read together as a 32-bit longword.

DFE **DMA FIFO Empty** **7**
This status bit is set when the DMA FIFO (DFIFO) is empty. It is possible to use it to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and does not cause an interrupt.

R **Reserved** **6**

BF **Bus Fault** **5**
This bit is set when a host bus fault condition is detected. A host bus fault can only occur when the SYM53C710 is bus master, and is defined as a memory cycle that ends by BERR/ (without HALT/) or TEA/ (without TA/) asserting. A bus fault occurs if Retry is attempted after the first transfer of a cache line burst.

ARBT **Aborted** **4**
This bit is set when an abort condition occurs. An abort condition occurs because of the following: the DP3_ABRT/ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting bit 7 of the Interrupt Status (ISTAT) register.

SSI **SCRIPTS Step Interrupt** **3**
If the Single Step Mode bit in the DMA Control (DCNTL) register is set, this bit is set and an interrupt is generated after successful execution of each SCRIPTS instruction.

SIR **SCRIPTS Interrupt Instruction Received** **2**
This status bit is set whenever an Interrupt instruction is evaluated as true.

WTD **Watchdog Time-out Detected** **1**
This status bit is set when the watchdog timer decrements to zero. The watchdog timer is only used for the host memory interface. When the timer decrements to zero, it indicates that the memory system did not assert the acknowledge signal within the specified time-out period.

IID **Illegal Instruction Detected** **0**

This status bit is set any time an illegal instruction is decoded, whether the SYM53C710 is operating in single step mode or automatically executing SCSI SCRIPTS.

This bit also sets if the SYM53C710 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

Note: See Chapter 2, “Functional Description” for a more detailed description of interrupts.

Register: 0x0D (0x0E)

SCSI Status Zero (SSTAT0)

Read Only

7	6	5	4	3	2	1	0
M/A	FCMP	STO	SEL	SGE	UDC	RST/	PAR
0	0	0	0	0	0	0	0

Reading this register clears any bits that are set at the time the register is read, but does not necessarily clear the register because additional interrupts may be pending (the SYM53C710 stacks interrupts). SCSI interrupt conditions are individually masked through the SCSI Interrupt Enable (SIEN) register.

When performing consecutive 8-bit reads of both the DMA Status (DSTAT) and SCSI Status Zero (SSTAT0) registers (in either order), insert a delay equivalent to 12 clock periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP and DIP bits are not set, read the SCSI Status Zero (SSTAT0) register before the DMA Status (DSTAT) register to avoid missing a SCSI interrupt. To clear the interrupts and avoid missing a SCSI interrupt, read both registers together as a 32-bit longword.

M/A **Initiator: Phase Mismatch or Target: ATN/ Active** **7**

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the SCSI phase defined in a Block Move instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator and the device is not in SELECT phase.

FCMP **Function Complete** **6**

This bit is set when an arbitration only or full arbitration sequence is completed.

STO **SCSI Bus Time-out** **5**

This bit is set if one of the following conditions occurs:

- There is a selection or reselection time-out. A selection/reselection time-out occurs if the device being selected or reselected does not respond within the 250 ms time-out period. CON is not set in the Interrupt Status (ISTAT) register.
- The Wait for Disconnect takes longer than 250 ms. The Wait for Disconnect instruction has a bus activity timer that is reset by the physical disconnect.
- No SCSI activity occurs for 250 ms while the SYM53C710 is connected to the bus. There is a timer on all bytes (in all phases) sent or received on the SCSI bus. The timer is a bus activity timer that is reset by a byte going over the SCSI bus. If 250 ms pass without a byte being moved, then a time-out will occur. This interrupt can be disabled by setting bit 6 (BTD) in the Chip Test Zero (CTEST0) register.

The user can disable STO by setting bit 4 (Notime) in the Chip Test Seven (CTEST7) register. This should be done when single stepping in the debugger.

SEL **Selected or Reselected** **4**

This bit is set when the SYM53C710 is selected or reselected by another SCSI device. The Enable Selection and Reselection bit must be set in the SCSI Control One (SCNTL1) register for the SYM53C710 to respond to selection and reselection interrupts.

SGE **SCSI Gross Error** **3**

This bit is set when the SYM53C710 encounters a SCSI Gross Error Condition. The following conditions can cause a SCSI Gross Error Condition:

- Data underflow – reading the SCSI FIFO when no data is present.
- Data overflow – writing too many bytes to the SCSI FIFO, or the synchronous offset causes overwriting the SCSI FIFO.

- Offset underflow – the SYM53C710 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.
- Offset overflow – the other SCSI device sends a REQ/ or ACK/ pulse with data which exceeds the maximum synchronous offset defined by the SCSI Transfer (SXFER) register.
- Residual data in the synchronous SCSI FIFO – a transfer other than synchronous data receive is started with data left in the synchronous data FIFO.
- A phase change occurred with an outstanding synchronous offset when the SYM53C710 is operating as an initiator.

UDC **Unexpected Disconnect** **2**

This bit is only valid when the SYM53C710 is in initiator mode. It is set when the SYM53C710 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. When the SYM53C710 is executing SCSI SCRIPTS, an unexpected disconnect is defined to be a disconnect that does not occur after receiving either a Disconnect Message (0x04) or a Command Complete Message (0x00). For example, if an ABORT message is sent, the Target will disconnect, resulting in a UDC. When the SYM53C710 operates in low level mode, any disconnect can cause an interrupt, even a valid SCSI disconnect.

RST/ **SCSI RST/ Received** **1**

This bit is set when the SYM53C710 detects an active RST/ signal, whether the reset is generated external to the chip or caused by the Assert RST/ bit in the SCSI Control One (SCNTL1) register. This SCSI reset detection logic is edge-sensitive, so that multiple interrupts are not generated for a single assertion of the SCSI RST/ signal.

PAR **Parity Error** **0**

This bit is set when the SYM53C710 detects a parity error while receiving or sending SCSI data. The Enable Parity Checking bit (bit 3 in the SCSI Control Zero (SCNTL0) register) must be set for this bit to become active. A parity error occurs when receiving data from the

SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SCSI Output Data Latch (SODL) register. A parity error occurs from the host bus only if pass through parity is enabled (bit 3 in the SCSI Control Zero (SCNTL0) register = 1, bit 2 in the SCSI Control Zero (SCNTL0) register = 0).

Note: See Chapter 2, "Functional Description" for a more detailed description of interrupts.

Register: 0x0E (0x0D)

SCSI Status One (SSTAT1)

Read Only

7	6	5	4	3	2	1	0
ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
0	0	0	0	0	0	0	0

ILF **SIDL Register Full** **7**

This bit is set when the SIDL contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch (SIDL) register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

ORF **SODR Register Full** **6**

This bit is set when the SCSI Output Data register (SODR, a hidden buffer register which is not directly accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not readable or writable by the user. It is possible to use this bit to determine how many bytes reside in the chip when an error occurs.

OLF **SODL Register Full** **5**

This bit is set when the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI Output Data register (SODR, a hidden buffer register which is not accessible) before being sent to the

SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. It is possible to use this bit to determine how many bytes reside in the chip when an error occurs.

AIP **Arbitration in Progress** **4**
Arbitration in Progress (AIP = 1) indicates that the SYM53C710 detects a bus free condition, asserts BSY, and asserts its SCSI ID onto the SCSI bus.

LOA **Lost Arbitration** **3**
When set, LOA indicates that the SYM53C710 detects a bus free condition, arbitrates for the SCSI bus, and loses arbitration due to another SCSI device asserting the SEL/ signal.

WOA **Won Arbitration** **2**
When set, WOA indicates that the SYM53C710 detects a bus free condition, arbitrates for the SCSI bus and wins arbitration. The arbitration mode selected in the SCSI Control Zero (SCNTL0) register must be full arbitration and selection to set this bit.

RST/ **SCSI RST/ Signal** **1**
This bit reports the current status of the SCSI RST/ signal. This bit is not latched and changes when read.

SDP/ **SCSI SDP/ Parity Signal** **0**
This bit represents the current status of the SCSI SDP/ parity signal. This signal is not latched and changes when read.

Register: 0x0F (0x0C)
SCSI Status Two (SSTAT2)
Read Only

7			4	3	2	1	0
FF[3:0]				SDP	MSG	C/D	I/O
0	0	0	0	0	0	0	0

FF[3:0] **FIFO Flags** **[7:4]**
These four bits define the number of bytes that currently reside in the SYM53C710 SCSI synchronous data FIFO. These bits are not latched and they change as data moves through the FIFO. Because the FIFO is only 8 bytes deep, values over 8 do not occur.

SDP **Latched SCSI Parity** **3**
This bit reflects the SCSI parity signal (SDP/), corresponding to the data latched in the SCSI Input Data Latch (SIDL) register. It changes when a new byte is latched into the SIDL register. This bit is active HIGH, in other words, it is set when the parity signal is active.

MSG **SCSI MSG/ Signal** **2**

C/D **SCSI C/D Signal** **1**

I/O **SCSI I/O Signal** **0**
These SCSI phase status bits are latched on the asserting edge of REQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

Registers: 0x10–0x13 (0x10–0x13)
Data Structure Address (DSA)
Read/Write

31																													0
DSA[31:0]																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSA **Data Structure Address** **[31:0]**

This register contains the base address used for all table indirect calculations. It is 32 bits wide and defaults to all zeros.

During any Memory Move operation, the contents of this register are overwritten. If the DSA value is needed for a subsequent SCSI SCRIPTS, save and later restore it.

Note: It is possible to perform a Memory-to-DSA Move, but not a DSA-to-Memory Move.

Register: 0x14 (0x17)
Chip Test Zero (CTEST0)
Read/Write

7	6	5	4	3	2	1	0
R	BTD	GRP	EAN	HSC	ERF	R	DDIR
0	0	0	0	0	0	0	0

R **Reserved** **7**
This bit must always be written to zero.

BTD **Byte-to-Byte Timer Disable** **6**
This bit, in conjunction with the Notime bit in CTEST7, provides the following selection/byte-to-byte timer options. At power-up or if both bits are not set, the selection and byte-to-byte timer are enabled. If Notime is set, both functions are disabled. If Notime is not set and the byte-to-byte disable is set, the selection timer will function but the byte-to-byte timer will be disabled.

GRP **Generate Receive Parity for Pass Through** **5**
When this bit is set, and the SYM53C710 is in parity pass through mode, the parity received on the SCSI bus will

not pass through to the DMA FIFO. Parity is generated as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through to the host bus. A SCSI parity error interrupt is generated, but a system parity problem is not created. After reset or when the bit is cleared, while pass through mode is enabled, parity received on the SCSI bus will pass through the SYM53C710 unmodified.

EAN **Enable Active Negation** **4**

Asserting this bit causes SCSI Request, Acknowledge, Data and Parity to be actively deasserted, instead of relying on external pull-ups, when the SYM53C710 is driving these signals. Active deassertion of these signals occurs only when the SYM53C710 is in an information transfer phase.

When operating in a differential environment or at fast SCSI timings, Active Negation should be enabled to improve setup and hold times. After reset or when the bit is cleared, Active Negation is disabled.

HSC **Halt SCSI Clock** **3**

Asserting this bit causes the internal divided SCSI clock to a stop in a glitchless manner. This bit is used for test purposes or to lower I_{DD} during a power-down mode.

Note: Reinitialize SCSI registers at power-up.

ERF **Extend REQ/ACK Filtering** **2**

The SCSI core contains a special digital filter on the REQ/ and ACK/ pins which causes glitches on deasserting edges to be disregarded. Asserting this bit extends the filter delay from 30 ns to 60 ns on the deasserting edge of the REQ/ and ACK/ signals. This 30 ns delay is used for fast SCSI.

Note: This bit must never be set during fast SCSI operations (> 5 M transfers per second), because a valid assertion is treated as a glitch. This bit does not affect transfer rates.

R **Reserved** **1**

DDIR **Data Transfer Direction** **0**

This status bit indicates which direction data is being transferred. When this bit is set, the data transfers from

the SCSI bus to the host bus. When this bit is clear, the data transfers from the host bus to the SCSI bus. This bit cannot be written.

Register: 0x15 (0x16)
Chip Test One (CTEST1)
Read Only

7			4	3			0
FMT[3:0]				FFL[3:0]			
1	1	1	1	0	0	0	0

FMT[3:0] **Byte Empty in DMA FIFO** **[7:4]**
These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty then FMT3 will be 1. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

FFL[3:0] **Byte Full in DMA FIFO** **[3:0]**
These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be 1. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register: 0x16 (0x15)
Chip Test Two (CTEST2)
Read Only

7	6	5	4	3	2	1	0
R	SIGP	SOFF	SFP	DFP	TEOP	DREQ	DACK
0	0	1	0	0	0	0	1

R **Reserved** **7**

SIGP **Signal Process** **6**
This bit is a copy of the SIGP bit in the Interrupt Status (ISTAT) register (bit 5). The SIGP bit is used to signal a running SCRIPTS instruction. The only SCRIPTS instruction directly affected by the SIGP bit is Wait for

Selection/Reselection. When this register is read, the SIGP bit in the Interrupt Status (ISTAT) register is cleared.

SOFF **SCSI Offset Compare** **5**

This bit operates differently, depending on whether the chip is an initiator or target. If the SYM53C710 is an initiator, this bit is set whenever the SCSI synchronous offset counter is equal to zero. If the SYM53C710 is a target, this bit is set whenever the SCSI synchronous offset counter is equal to the maximum synchronous offset defined in the SCSI Transfer (SXFER) register.

SFP **SCSI FIFO Parity** **4**

This bit represents the parity bit of the SCSI synchronous FIFO corresponding to data read out of the FIFO. Reading the Chip Test Three (CTEST3) register unloads a data byte from the bottom of the SCSI synchronous FIFO. When the Chip Test Three (CTEST3) register is read, the data parity bit is latched into this bit location.

DFP **DMA FIFO Parity** **3**

This bit represents the parity bit of the DMA FIFO when the Chip Test Six (CTEST6) register reads data out of the FIFO. Reading the Chip Test Six (CTEST6) register unloads one data byte from the bottom of the DMA FIFO. When the Chip Test Six (CTEST6) register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

TEOP **SCSI True End of Process** **2**

This bit indicates the status of the SYM53C710 internal TEOP signal. The TEOP signal acknowledges the completion of a block move through the SCSI portion of the SYM53C710. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

DREQ **Data Request Status** **1**

This bit indicates the status of the SYM53C710 internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

DACK **Data Acknowledge Status** **0**

This bit indicates the status of the SYM53C710 internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register: 0x17 (0x14)

Chip Test Three (CTEST3)

Read Only

7							0
SF[7:0]							
0	0	0	0	0	0	0	0

SF[7:0] **SCSI FIFO** **[7:0]**

Reading this register unloads the bottom byte of the 8-byte SCSI synchronous FIFO. Reading this register also latches the parity bit for the FIFO into the SCSI FIFO Parity bit in the Chip Test Two (CTEST2) register. The FIFO Full bits in the SCSI Status Two (SSTAT2) register can be read to determine how many bytes currently reside in the SCSI synchronous FIFO. Reading this register when the SCSI FIFO is empty causes a SCSI Gross Error (FIFO underflow).

Register: 0x18 (0x1B)

Chip Test Four (CTEST4)

Read/Write

7	6	5	4	3	2		0
MUX	ZMOD	SZM	SLBE	SFWR	FBL[2:0]		
0	0	0	0	0	0	0	0

MUX **Host Bus Multiplex Mode** **7**

When set, the MUX bit puts the SYM53C710 into host bus MUX mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is 3-stated), and then 3-states the address bus and drives the data bus (if a write). This allows the address and data buses to be tied together. It should be written prior to acquiring bus mastership. The MUX mode bit allows the SYM53C710 to operate without external

hardware on those host buses on which data and addresses share a common 32 bits.

ZMOD **High Impedance Mode** **6**

Setting this bit causes the SYM53C710 to place all output and bidirectional pins into a high impedance state. In order to read data out of the SYM53C710, this bit must be cleared.

This bit is intended for board level testing only. Setting this bit during system operation results in a system failure.

SZM **SCSI High Impedance Mode** **5**

Setting this bit causes the SYM53C710 to place certain SCSI outputs in a high impedance state. The following outputs are in a high impedance state: SD[7:0], SDP, BYS/, SEL/, RST/, REQ/, C/D, I/O, MSG/, ACK/, ATN/. The direction control lines (SDIR[7:0], SDIRP, BSYDIR, RSTDIR, and SELDIR) are driven LOW and are not in a high impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

SLBE **SCSI Loopback Enable** **4**

Setting this bit enables loopback mode. Loopback allows any SCSI signal to be asserted. SYM53C710 may be an initiator or a target. It also allows the SYM53C710 to transfer data from the SCSI Output Data Latch (SODL) register back into the SCSI Input Data Latch (SIDL) register.

SFWR **SCSI FIFO Write Enable** **3**

Setting this bit redirects data from the SODL to the SCSI FIFO. A write to the SCSI Output Data Latch (SODL) register loads a byte into the SCSI FIFO. The parity bit loaded into the FIFO is odd or even parity depending on the status of the Assert SCSI Even Parity bit in the SCSI Control One (SCNTL1) register. Clearing this bit will disable this feature.

FBL[2:0] **FIFO Byte Control** **[2:0]**

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	x	x	Disabled	N/A
1	0	0	0	D[7:0]
1	0	1	1	D[15:8]
1	1	0	2	D[23:16]
1	1	1	3	D[31:24]

These bits send the contents of the Chip Test Six (CTEST6) register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. If the FLB2 bit is cleared, internal logic determines which byte lane of the DMA FIFOs is to be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set to this value before executing SCSI SCRIPTS).

Register: 0x19 (0x1A)

Chip Test Five (CTEST5)

Read/Write

7	6	5	4	3	2	1	0
ADCK	BBCK	ROFF	MASR	DDIR	EOP	DREQ	DACK
0	0	0	0	0	0	0	0

ADCK **Clock Address Incrementor** **7**

Setting this bit increments the address pointer contained in the DMA Next Data Address (DNAD) register. The DMA Next Data Address (DNAD) register is incremented by 1, 2 or 4, based on the current DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DMA Next Data Address (DNAD) register.

BBCK **Clock Byte Counter** **6**

Setting this bit decrements the byte count contained in the DMA Byte Counter (DBC) register. It is decremented

by 1, 2 or 4 based on the current DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DMA Byte Counter (DBC) register.

ROFF **Reset SCSI Offset** **5**

Setting this bit clears any outstanding synchronous SCSI REQ/ACK offset. This bit is set when a SCSI Gross Error condition occurs. The offset is reset when a synchronous transfer does not complete successfully. This bit automatically resets itself after clearing the synchronous offset.

MASR **Master Control for Set or Reset Pulses** **4**

This bit controls the operation of bits [3:0]. When this bit is set, bits [3:0] assert the corresponding signals. When this bit is reset, bits [3:0] deassert the corresponding signals. This bit and bits [3:0] should not be changed in the same write cycle.

DDIR **DMA Direction** **3**

Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data is transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

EOP **End of Process** **2**

Setting this bit either asserts or deasserts the internal EOP control signal depending on the current status of the MASR bit in this register. The internal EOP signal is an output from the DMA portion of the SYM53C710 to the SCSI portion of the SYM53C710. Asserting the EOP signal indicates that the last data byte has been transferred between the two portions of the chip. Deasserting the EOP signal indicates that the last data byte has not been transferred between the two portions of the chip. If the MASR bit is configured to assert this signal, this bit automatically clears itself after pulsing the EOP signal.

DREQ **Data Request** **1**

Setting this bit either asserts or deasserts the internal DREQ (data request signal) depending on the current status of the MASR bit in this register. Asserting the

DREQ signal indicates that the SCSI portion of the SYM53C710 requests a data transfer with the DMA portion of the chip. Deasserting the DREQ signal indicates that data should not be transferred between the SCSI portion of the SYM53C710 and the DMA portion. If the MASR bit is configured to assert this signal, this bit automatically clears after asserting the DREQ signal.

DACK **Data Acknowledge** **0**

Setting this bit either asserts or deasserts the internal DACK/ data request signal dependent on the current status of the MASR bit in this register. Asserting the DACK/ signal indicates that the DMA portion of the SYM53C710 acknowledges a data transfer with the SCSI portion of the chip. Deasserting the DACK/ signal indicates that data should not be transferred between the DMA portion of the SYM53C710 and the SCSI portion. If the MASR bit is configured to assert this signal, this bit automatically clears itself after asserting the DACK/ signal.

Register: 0x1A (0x19)

Chip Test Six (CTEST6)

Read/Write

7							0
DF[7:0]							
x	x	x	x	x	x	x	x

DF[7:0] **DMA FIFO** **[7:0]**

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the Chip Test Four (CTEST4) register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the Chip Test Four (CTEST4) register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the Chip Test Two (CTEST2) register.

To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS.

Note: Writing to this register loads the DMA FIFO, regardless of the FBL bits in the Chip Test Four (CTEST4) register. Use the FLF bit in the Chip Test Eight (CTEST8) register to flush the DMA FIFO.

Register: 0x1B (0x18)

Chip Test Seven (CTEST7)

Read/Write

7	6	5	4	3	2	1	0
CDIS	SC[1:0]		Notime	DFP	EVP	TT1	DIFF
0	0	0	0	0	0	0	0

CDIS **Cache Burst Disable** **7**

When this bit is set, the SYM53C710 does not request a cache line burst. When this bit is clear, the chip attempts cache line bursts when two conditions are met. The first condition is that the address must be lined up to a cache line boundary (A3–A0 must be zero). The second condition is that the transfer counter must be at least 32. Cache line burst mode eliminates the need for a full handshake between the bus master and the memory device when transferring data. Burst length in DMODE must be 4 if caching is enabled.

SC[1:0] **Snoop Control** **[6:5]**

The SC0 and SC1 bits control the two Snoop Control pins. The SC1 bit controls the Snoop Control 1 pin all of the time. The SC0 bit controls the Snoop Control 0 pin only when the snoop mode bit is not set. Monitoring the SC0 bit gives advance notice of a pending SYM53C710 bus request. Bus snooping allows for transmission of additional information to other devices on the host bus about the current type of transfer. In Bus Mode 2, the host processor can snoop an alternate master Read/Write transfer, ensuring access to valid data. In other operating modes, these bits and pins provide additional user defined functionality.

Notime **Selection Time-out Disable** **4**

Setting this bit disables the 250 ms timer for all modes, including byte-to-byte. If STO is disabled, the user cannot abort a Select/Reselect SCRIPTS instruction using the ABORT bit.

DFP **DMA FIFO Parity** **3**

This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO using programmed I/O. In order to transfer data to or from the DMA FIFO, perform a read or a write to the Chip Test Six (CTEST6) register. When loading data into the FIFO using programmed I/O, write this bit to the FIFO as the parity bit for each byte loaded. When writing data to the DMA FIFO, set this bit with the status of the parity bit to be written to the FIFO before writing the byte to the FIFO.

EVP **Even Parity** **2**

Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense.

Setting this bit causes the SYM53C710 to generate even parity when driving data on the host data bus. The SYM53C710 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the SYM53C710 checks parity and sends the data to the SCSI bus. Clearing this bit causes the SYM53C710 to maintain odd parity throughout the chip.

TT1 **Transfer Type Bit** **1**

The inverted value of this bit is asserted on the TT1 pin during bus mastership in Bus Mode 2 only. This bit is not used in Bus Mode 1.

DIFF **Differential Mode** **0**

Setting this bit enables the SYM53C710 to interface with external differential pair transceivers. The SCSI BSY/, SEL/, and RST/ are input only in differential mode. For more information on differences between the two modes, refer to the pin descriptions for these signals. Resetting this bit enables SE mode. This bit should be set in the initialization routine if the differential pair interface is to be used.

Register: 0x1C (0x1C–0x1F)
Temporary Stack (TEMP)
Read/Write

31																												0
TEMP[31:0]																												
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TEMP **Temporary Stack** **[31:0]**

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction. The address pointer stored in this register is loaded into the DMA SCRIPTS Pointer (DSP) register. This address points to the next instruction to be executed. Do not write to TEMP while the SYM53C710 is executing SCSI SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are destroyed. If the TEMP value is needed for a subsequent SCSI SCRIPTS, save and then later restore it.

Register: 0x20 (0x23)
DMA FIFO (DFIFO)
Read/Write

7	6						0
R	BO[6:0]						
0	0	0	0	0	0	0	1

R **Reserved** **7**

BO[6:0] **Byte Offset Counter** **[6:0]**
These six bits indicate the amount of data transferred between the SCSI core and the DMA core. They are used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores. Once the chip has stopped transferring data, these bits are stable.

The following steps determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer.

1. Subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register.
2. AND the result with 0x7F for a byte count between zero and 64.

Register: 0x21 (0x22)

Interrupt Status (ISTAT)
Read/Write

7	6	5	4	3	2	1	0
ABRT	RST	SIGP	R	CON	R	SIP	DIP
0	0	0	0	0	0	0	0

This is the only register that is accessible by the host CPU while the SYM53C710 is executing SCRIPTS (without interfering in the operation of the SYM53C710). It is used to poll for interrupts if interrupts are masked. When either the SIP or DIP bit is set, the DSTAT and SSTAT0 latches close and subsequent interrupts are stacked (held in a pending register “behind” the status register). When the current interrupt is cleared by reading the appropriate status register, the stacked interrupts are transferred to the status register and cause another interrupt.

When an interrupt event occurs, the SYM53C710 halts in an orderly fashion before asserting IRQ. If in the middle of an instruction fetch, the fetch is completed (except in the case of a Bus Fault or Watchdog Time-out), though execution does not begin. If possible, DMA write operations empty the FIFO before halting. All other DMA operations finish only the current cycle (or burst if a cache line) before halting. SCSI handshakes that have begun are completed before halting. The SYM53C710 attempts to clean up any outstanding synchronous offset. In the case of Transfer Control Instructions, once execution begins it continues to completion before halting. If the instruction is JUMP/CALL WHEN, the wait aborts and the DSP is updated to the transfer address before halting. All other instructions halt before completing execution.

Note: The ISTAT is a shadowed register, therefore it cannot be accessed using the Read/Write Instruction. To move the Interrupt Status (ISTAT) register to the SFBR, use a Memory Move to transfer the ISTAT to SCRATCH1, then perform a SCRATCH1-to-SFBR Move.

ABRT **Abort Operation** **7**

Setting this bit aborts the current operation under execution by the SYM53C710. If this bit is set and an interrupt is received, reset this bit before reading the DMA Status (DSTAT) register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1. Set this bit.
2. Wait for an interrupt.
3. Read the Interrupt Status (ISTAT) register.
4. If the SCSI Interrupt Pending bit is set, read the SCSI Status Zero (SSTAT0) register to determine the cause of the SCSI Interrupt and go back to Step 2.
5. If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, write 0x00 value to this register to clear the ABORT.
6. Read the DMA Status (DSTAT) register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

The ABORT operation aborts a sequence of instructions. It does not abort a current opcode execution. ABORT looks for an appropriate time to interrupt. During a Selection/Reselection, ABORT interrupts at STO. During a Move, ABORT waits for the transfer to complete, or for the Target to change phase or disconnect.

RST **Software Reset** **6**

Setting this bit resets the SYM53C710. All registers except the DCNTL EA bit are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not assert the SCSI RST/ signal. This bit is not self-clearing; it must be cleared to remove the reset condition (a hardware reset also clears this bit). This reset does not clear the Enable Acknowledge (EA) bit, the Function Control One (FC1) bit, or the COM bit in the DMA Control (DCNTL) register.

SIGP **Signal Process** **5**

SIGP is a Read/Write bit that is writable at any time, and polled and reset using Chip Test Two (CTEST2). The

SIGP bit is used in various ways to pass a flag to or from a running SCRIPTS.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait for Selection/Reselection. Setting this bit causes that opcode to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit is usable at any time and is not restricted to the Wait for Selection/Reselection condition.

Note: If the SIGP bit is active when a selection/reselection occurs, the autoswitching from/to target mode is disabled and must be manually set by either the host or a SCRIPTS.

R **Reserved** **4**

CON **Connected** **3**
This bit is automatically set any time the SYM53C710 is connected to the SCSI bus as an initiator or as a target. It is set after successfully completing arbitration or when the SYM53C710 responds to a bus initiated selection or reselection. It is also set after the SYM53C710 wins arbitration when operating in low level mode. When this bit is clear, the SYM53C710 is not connected to the SCSI bus. This bit is unlatched and may be changing as it is read.

R **Reserved** **2**

SIP **SCSI Interrupt Pending** **1**
This status bit is set when an interrupt condition is detected in the SCSI portion of the SYM53C710. The following conditions cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)
- An arbitration sequence completes
- A selection or reselection time-out occurs
- The SYM53C710 is selected or reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs

- A parity error is detected

To determine exactly which condition(s) caused the interrupt, read the SCSI Status Zero (SSTAT0) register.

This bit is synchronous to BCLK, but may change during read cycles.

DIP **DMA Interrupt Pending** **0**

This status bit is set when an interrupt condition is detected in the DMA portion of the SYM53C710. The following conditions cause a DMA interrupt to occur:

- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single step mode
- A SCRIPTS interrupt instruction is executed
- The Watchdog Timer decrements to zero
- An illegal instruction is detected

To determine exactly which condition(s) caused the interrupt, read the DMA Status (DSTAT) register.

The bit is synchronous to BCLK, but may change during read cycles.

Note: See Chapter 2, “Functional Description” for a more detailed description of interrupts.

Register: 0x22 (0x21)
Chip Test Eight (CTEST8)
Read/Write

7			4	3	2	1	0
V[3:0]				FLF	CLF	FM	SM
V	V	V	V	0	0	0	0

V[3:0] **Chip Revision Level** **[7:4]**

These bits identify the chip revision level for software purposes. This technical manual applies to devices with revision level 2 (0010).

FLF **Flush DMA FIFO** **3**

When this bit is set, data residing in the DMA FIFO is transferred to memory, starting at the address in the DMA Next Data Address (DNAD) register. The internal DMAWR signal, controlled by the Chip Test Five (CTEST5) register, determines the direction of the transfer. This bit is not self-clearing; clear it once the data is successfully transferred by the SYM53C710. Setting this bit does not flush the SCSI FIFO or SIDL.

Note: All chip registers may be read during flush operations.

CLF **Clear DMA and SCSI FIFOs** **2**

When this bit is set, all data pointers for the SCSI and DMA FIFOs are cleared. In addition to the SCSI and DMA FIFO pointers, the SIDL, SODL, and SODR full bits in the SCSI Status One (SSTAT1) register are cleared. Data in either of the FIFOs is lost. This bit automatically resets after the SYM53C710 successfully clears the appropriate FIFO pointers and registers.

FM **Fetch Pin Mode** **1**

When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ is only active during the opcode portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM, reducing the long delay associated with arbitrating for the host bus in order to fetch SCRIPTS instructions from system memory.

If this bit is not set, FETCH/ is asserted for all bus cycles during instruction fetches.

SM **Snoop Pins Mode** **0**

When set, the two snoop pins change functions and become pure outputs that are always driven, except when in ZMODE.

Pin	Function
SC0	Becomes a copy of the internal bus request signal. Signal asserts prior to BR/ and is negated during the AS/ (Asynchronous, or TS/, Synchronous) of the last bus cycle. Note: If cache line bursting is enabled, the signal is negated prior to the release of the last TA.
SC1	Drives the value in the SC1 register bit.

When clear, the snoop pins are driven during host bus ownership with the values of the CTEST7 SC[1:0] bits.

Register: 0x23 (0x20)

Longitudinal Parity (LCRC)

Read/Write

7							0
LCRC[7:0]							
0	0	0	0	0	0	0	0

LCRC **Longitudinal Parity** **[7:0]**

This register contains the longitudinal parity for all data crossing the DMA FIFO to or from the SCSI core. The parity consists of an exclusive OR of all data bytes.

Writing to this register clears its contents to 0x00 regardless of the value written.

Like the SCSI First Byte Received (SFBR) register in the SYM53C700, this register is used by the SCSI core to hold the SCSI ID value during selection and reselection. The Longitudinal Parity (LCRC) register is used instead of the SFBR because the SFBR is used as an accumulator during many SCRIPTS operations, and may be overwritten at any time by a selection or reselection.

Register: 0x24–0x26 (0x25–0x27)
DMA Byte Counter (DBC)
Read/Write

23																					0
DBC[23:0]																					
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DBC **DMA Byte Counter** **[23:0]**

This 24-bit register determines the number of bytes transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the SYM53C710. The DBC counter is decremented each time the AS/ signal is pulsed by the SYM53C710. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DMA Byte Counter (DBC) register is 0xFFFFFF. If the instruction is a Block Move and a value of 0x000000 is loaded into the DBC register, an illegal instruction interrupt occurs if the chip is not operating in a target mode command phase.

The DMA Byte Counter (DBC) register is also used during table indirect I/O SCRIPTS to hold the offset value.

Register: 0x27 (0x24)
DMA Command (DCMD)
Read/Write

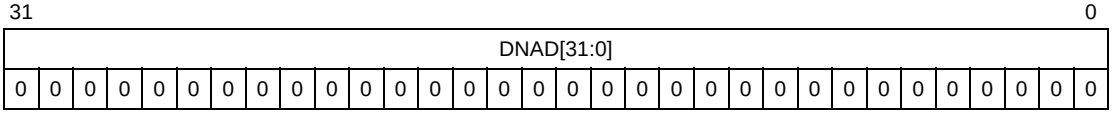
7							0
DCMD[7:0]							
0	0	0	0	0	0	0	0

DCMD **DMA Command** **[7:0]**

This 8-bit register determines the instruction for the SYM53C710 to execute. This register has a different

format for each instruction. For a complete description, refer to the SYM53C710 instruction set.

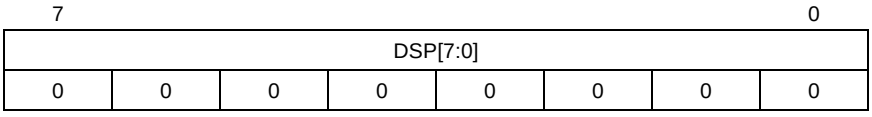
Register: 0x28–0x2B (0x28–0x2B)
DMA Next Data Address (DNAD)
Read/Write



DNAD **DMA Next Data Address** **[31:0]**
This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DMA SCRIPTS Pointer Save (DSPS) register. Its value may not be valid except in certain abort conditions.

To maintain software compatibility with the SYM53C700, interrupt vectors are read from the DMA SCRIPTS Pointer Save (DSPS) register.

Register: 0x2C–0x2F (0x2C–0x2F)
DMA SCRIPTS Pointer (DSP)
Read/Write



DSP **DMA SCRIPTS Pointer** **[7:0]**
To execute SCSI SCRIPTS, the address of the first SCSI SCRIPTS must be written to this register. In normal SCRIPTS operation, once the starting address of the SCSI SCRIPTS is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single step mode, there is a SCRIPTS step interrupt after each instruction is executed. The DMA SCRIPTS Pointer (DSP) register does not need to be written with the next address, but the Start DMA bit (bit 2), DMA Control (DCNTL) must be set each time the step interrupt

occurs to fetch and execute the next SCSI SCRIPTS. When writing this register eight bits at a time, writing the upper eight bits, 2F (2C), begins execution of SCSI SCRIPTS.

Register: 0x30–0x33 (0x30–0x33)

DMA SCRIPTS Pointer Save (DSPS)

Read/Write

7							0
DSPS[7:0]							
0	0	0	0	0	0	0	0

DSPS **DMA SCRIPTS Pointer Save** **[7:0]**

This register contains the second longword of Read/Write or Transfer Control SCRIPTS instructions. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS interrupt instruction is fetched, this register holds the interrupt vector.

Register: 0x34–0x37 (0x34–0x37)

Scratch (SCRATCH)

Read/Write

7							0
SCRATCH[7:0]							
0	0	0	0	0	0	0	0

SCRATCH **Scratch (SCRATCH)** **[7:0]**

This is a general purpose, user-definable scratch pad register. Apart from CPU access, only register read/write and memory moves into the Scratch (SCRATCH) register alter its contents.

The Scratch (SCRATCH) register combined with Register-to-Register Move, AND, OR, and ADD operations provides the capability to write a complete SCSI interface program in SCRIPTS.

Register: 0x38 (0x3B)
DMA Mode (DMODE)
Read/Write

7	6	5	4	3	2	1	0
BL[1:0]		FC[1:0]		PD	FAM	U0	MAN
0	0	0	0	0	0	0	0

BL[1:0] **Burst Length** **[7:6]**

BL1	BL0	Burst Length
0	0	1 - Transfer Burst
0	1	2 - Transfer Burst
1	0	4 - Transfer Burst
1	1	8 - Transfer Burst

These bits control the number of cycles performed per bus ownership. The SYM53C710 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed.

To perform cache line burst, these bits must be set to 4 transfers and cache bursting must be enabled (CTEST7).

The SYM53C710 inserts a “fairness delay” of approximately 5 to 8 BCLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

FC[1:0] **Function Code** **[5:4]**
These bits are user defined. Their values are asserted onto the corresponding device pins during bus mastership. These bits/pins are active in both bus modes.

PD **Program/Data** **3**
This bit affects the function of the FC0/ pin. Setting this bit causes the SYM53C710 to drive the FC0/ signal low when fetching instructions from memory. Clearing this bit causes the SYM53C710 to drive the FC0/ signal high when fetching instructions from memory.

The FC0/ signal is always driven high when moving data to or from memory and can only be driven low during instruction fetch cycles. This feature can be used to allow SCRIPTS and data to be stored in separate memory banks.

FAM **Fixed Address Mode** **2**

When the fixed address mode bit is set, the address pointer in the DMA Next Data Address (DNAD) register is disabled and will not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. The fixed address mode feature is used to transfer data to or from a fixed port address. This port width must be 32 bits and longword aligned. Setting this bit does not affect SCRIPTS fetching instructions; only data transfer instructions are affected.

U0 **User Programmable Transfer Type** **1**

In both bus modes, UPSO-TT0/ is a general purpose output pin. The value of this bit is asserted onto the UPSO-TT0/ pin while the SYM53C710 is a bus master, to indicate the type of access for the current bus transfer.

MAN **Manual Start Mode** **0**

Clearing this bit causes the SYM53C710 to automatically fetch and execute SCSI SCRIPTS after the DMA SCRIPTS Pointer (DSP) register is written. Setting this bit disables the SYM53C710 from automatically fetching and executing SCSI SCRIPTS after the DMA SCRIPTS Pointer (DSP) register is written. When the Start DMA bit in the DMA Control (DCNTL) register is cleared, it controls the start time of the operation. Once the Start DMA bit in the DMA Control (DCNTL) is set, the SYM53C710 automatically fetches and executes each instruction.

Register: 0x39 (0x3A)
DMA Interrupt Enable (DIEN)
Read/Write

7	6	5	4	3	2	1	0
R		BF	ABRT	SSI	SIR	WTD	IID
0	0	0	0	0	0	0	0

R **Reserved** **[7:6]**

BF **Bus Fault** **5**

ABRT **Abort Operation** **4**

SSI **SCSI Set Interrupt** **3**

SIR **SCRIPTS Interrupt Instruction Received** **2**

WTD **Watchdog Time-out Detected** **1**

IID **Illegal Instruction Detected** **0**

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DMA Status (DSTAT) register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit is still set in the DMA Status (DSTAT) register. Masking an interrupt does not prevent setting the ISTAT DIP from being set; all DMA interrupts are considered fatal. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

A masked nonfatal interrupt does not prevent unmasked or fatal interrupts from getting through. Interrupt stacking does not begin until either the ISTAT SIP or DIP bit is set.

The SYM53C710 IRQ/ output is latched; once asserted, it remains asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted does not cause IRQ/ to be deasserted.

Note: See Chapter 2, “Functional Description” for a more detailed description of interrupts.

Register: 0x3A (0x39)

DMA Watchdog Timer (DWT)
Read/Write

7							0
DWT[7:0]							
0	0	0	0	0	0	0	0

DWT **DMA Watchdog Timer** **[7:0]**

The DMA watchdog timer register provides a time-out mechanism during data transfers between the SYM53C710 and memory. This register determines the amount of time that the SYM53C710 waits for the assertion of the transfer acknowledge (TA/) signal after starting a bus cycle. Write the time-out value to this register during initialization. Every time that the SYM53C710 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the time-out feature by writing 0x00 to this register.

The unit time base for this register is 16 * BCLK input period. For example, at 50 MHz the time base for this register is 16 x 20 ns = 320 ns. If a time-out of 50 µs is desired, then this register should be loaded with a value of 0x9D.

The minimum time-out value that should be loaded into this register is 0x02; the value 0x01 does not provide a reliable time-out period.

Register: 0x3B (0x38)
DMA Control (DCNTL)
Read/Write

7	6	5	4	3	2	1	0
CF[1:0]		EA	SSM	LLM	STD	FA	COM
0	0	0	0	0	0	0	0

CF[1:0] **Clock Frequency** **[7:6]**

CF1	CF0	SCSI Core Clock	SCLK Frequency
1	1	SCLK/3	50.01 – 66.67 MHz
0	0	SCLK	237.51 – 50.00 MHz
0	1	SCLK	1.525.01 – 37.50 MHz
1	0	SCLK	116.67 – 25.00 MHz

These two bits determine the SCLK prescale factor used by the SYM53C710 SCSI core; the internal SCSI clock is derived from the externally applied SCLK. The above table describes how to program these two bits.

Note: It is important that these bits be set to the proper values to guarantee that the SYM53C710 meets the SCSI timings as defined by the ANSI specification. These bits affect both asynchronous and synchronous timings (unless the synchronous clock is decoupled using the SCSI Bus Control Lines (SBCL) register).

EA **Enable ACK** **5**
Setting this bit causes the STERM/_TA/ pin to become bidirectional. As a result, the SYM53C710 generates STERM/_TA/ during slave accesses. When this bit is clear, the SYM53C710 will monitor STERM/_TA/ to determine the end of a cycle. This bit takes effect during the cycle in which it is set; setting this bit must be the first I/O performed to the SYM53C710 if this feature is desired. See Chapter 2, “Functional Description” for information on bidirectional STERM/_TA/.

SSM **Single Step Mode** **4**
Setting this bit causes the SYM53C710 to stop after executing each SCRIPTS instruction, and generate a

SCRIPTS step interrupt. When this bit is cleared, the SYM53C710 does not stop after each instruction. It continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, keep this bit cleared. To restart the SYM53C710 after it generates a SCRIPTS Step interrupt, the Interrupt Status (ISTAT) and DMA Status (DSTAT) registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

LLM **Enable SCSI Low Level Mode** **3**

Setting this bit places the SYM53C710 in low level mode. In this mode, no DMA operations can occur, and no SCRIPTS instructions can be executed. Arbitration and selection are performed by setting the Start Sequence bit as described in the SCSI Control Zero (SCNTL0) register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

STD **Start DMA Operation** **2**

The SYM53C710 fetches a SCSI SCRIPTS instruction from the address contained in the DMA SCRIPTS Pointer (DSP) register when this bit is set. This bit is required if the SYM53C710 is in one of the following modes:

- Manual start mode – Bit 0 in the DMA Mode (DMODE) register is set
- Single step mode – Bit 4 in the DMA Control (DCNTL) is set

When the SYM53C710 is executing SCRIPTS in manual start mode, the Start DMA bit must be set to start instruction fetches, but need not be set again until an interrupt occurs. When the SYM53C710 is in single step mode, set the Start DMA bit to restart execution of SCRIPTS after a single step interrupt.

FA **Fast Arbitration** **1**

When this bit is set, the SYM53C710 immediately becomes bus master after receiving a bus grant, saving one clock cycle of arbitration time. When this bit is clear, the SYM53C710 follows the normal arbitration sequence.

COM **SYM53C700 Compatibility** **0**

When this bit is clear, the SYM53C710 behaves in a manner compatible with the SYM53C700; selection/reselection IDs are stored in both the Longitudinal Parity (LCRC) and SCSI First Byte Received (SFBR) registers, and autoswitching is enabled. The default condition of this bit (clear) causes the SYM53C710 to act the same as the SYM53C700.

When this bit is set, the ID is stored only in the Longitudinal Parity (LCRC) register, protecting the SFBR from being overwritten if a selection/reselection occurs during DMA register-to-register operation. When this bit is set, autoswitching is disabled.

Register: 0x3C–0x3F (0x3C–0x3F)

Adder Sum Output (ADDER)

Read Only

31																													0
ADDER[31:0]																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADDER **Adder Sum Output** **[31:0]**

This 32-bit register contains the output of the internal adder, and is used primarily for test purposes.

Chapter 5
Instruction Set of the I/O Processor

This chapter contains the following sections:

After power-up and initialization of the SYM53C710, the chip may be operated in one of two modes:

1. Low level register interface
2. SCSI SCRIPTS mode

In the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip may be operated much like a SYM53C80. An external processor has access to the SCSI bus signals and the low level DMA signals, to allow creation of complicated board level test algorithms. The low level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip’s pins.

To operate in the SCSI SCRIPTS mode, the SYM53C710 requires only a SCRIPTS start address. All commands are fetched from external memory. The SYM53C710 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as

detection of a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the SYM53C710 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer (DSP) register to restart the automatic fetch and execution of instructions.

The SCSI SCRIPTS mode of execution allows the SYM53C710 to make decisions based on the status of the SCSI bus. This reduces the need for interrupt service by the microprocessor.

Given the rich set of SCSI-oriented features included in the command set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Switching to low level mode for error recovery should never be required.

Five types of instructions are implemented in the SYM53C710:

- Block Move
- I/O
- Read/Write
- Transfer Control
- Memory Move

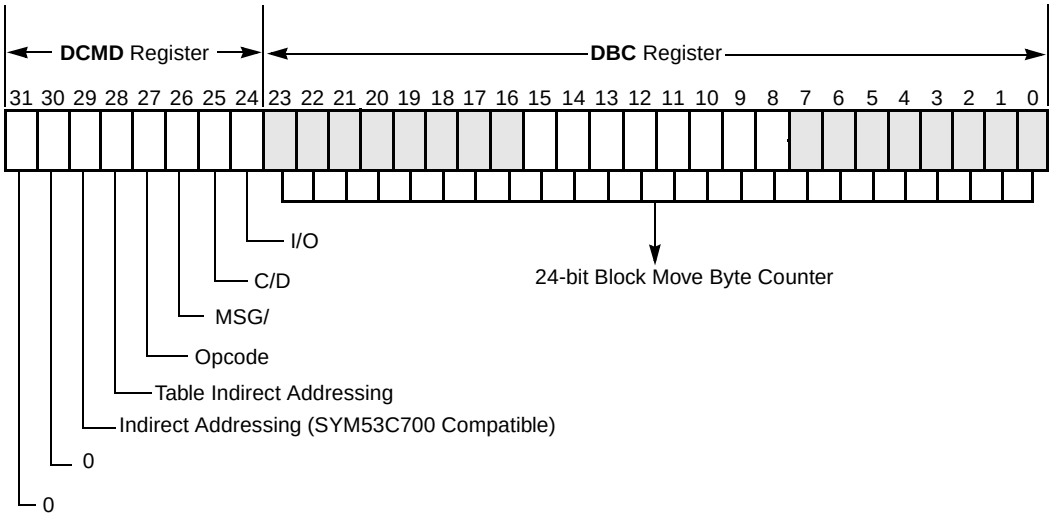
Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DMA Command (DCMD) and DMA Byte Counter (DBC) registers, the second into the DMA SCRIPTS Pointer Save (DSPS) register. The third word, used only by Memory Move instructions, is loaded into the Temporary Stack (TEMP) register.

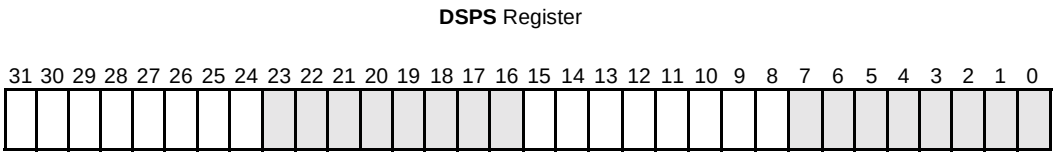
5.1 Getting Started

Before fetching and executing SCRIPTS, initialize the SYM53C710 registers. If using the bidirectional STERM/_TA/ feature, initialize the EA bit in the DMA Control (DCNTL) before any other registers. Also, at a minimum, the DMA registers (DMA Mode (DMODE), DMA Control (DCNTL), and DMA Interrupt Enable (DIEN) and SCSI registers SCSI Control Zero (SCNTL0), SCSI Control One (SCNTL1), SCSI Transfer (SXFER), SCSI Interrupt Enable (SIEN), and SCSI Bus Control Lines (SBCL) should be initialized to their desired values, if the default values are not correct. After these registers are initialized, the starting address of SCRIPTS instructions is loaded into the DSP. When the high byte of DSP is written, the SCRIPTS begin executing.

Figure 5.1 describes the Block Move Instruction register.

Figure 5.1 Block Move Instruction Register





Instruction Type Block Move **[31:30]**

Indirect Addressing **29**

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred.

When set, the 32-bit data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DMA Next Data Address (DNAD) register using a third longword fetch (4-byte transfer across the host computer bus).

Direct Addressing

The byte count and absolute address are:

Command	Byte Count
Address of Data	

Indirect Addressing

Use the byte count and fetch the data address from the address in the command. The byte count is contained in the DMA Byte Counter (DBC) register and the data address is fetched from the DMA SCRIPTS Pointer Save (DSPS) register.

Command	Byte Count
Address of Pointer to Data	

Once the data buffer is loaded, it is executed as if the chip were operating in the direct mode.

Table Indirect **28**

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the Data Structure Address (DSA) register. Both the transfer count and the source/destination address are fetched from this address.

Use the signed integer offset in bits [23:0] of the second 4 bytes of the instruction to fetch first the byte count and

then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign extended values of all ones for negative values are allowed, but ignored.

Command	Not Used
xx	Table Offset

Prior to the start of an I/O, the Data Structure Address (DSA) register must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from this address brings the data values into the chip.

For a MOVE command, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the SYM53C710. Execution begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory. The eight bytes of data in the MOVE command must be contiguous, as shown below. Indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

00	Byte Count
Physical Data Address	

Opcode **27**

This 1-bit Opcode field defines the instruction to be executed. The Opcode Field bit has different meaning depending on whether the SYM53C710 is operating in initiator or target mode. Entering a reserved value for the

current operating mode causes an illegal instruction interrupt.

Target Mode

In Target mode, the Opcode bit defines the following operations:

OPC	Instruction Defined
0	MOVE
1	Reserved

These instructions perform the following steps:

1. The SYM53C710 verifies that it is connected to the SCSI bus as a target before executing this instruction.
2. The SYM53C710 asserts the SCSI phase signals (MSG/, C/D, and I/O) as defined by the Phase Field bits in the instruction.
3. If the instruction is for the Command phase, the SYM53C710 receives the first command byte and decodes its SCSI Group Code.
   a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the SYM53C710 overwrites the DMA Byte Counter (DBC) register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.
   b) If any other Group Code is received, the DMA Byte Counter (DBC) register is not modified and the SYM53C710 requests the number of bytes specified in the DMA Byte Counter (DBC) register. If the DMA Byte Counter (DBC) register contains 0x000000, an illegal instruction interrupt is generated.
4. The SYM53C710 transfers the number of bytes specified in the DMA Byte Counter (DBC) register starting at the address specified in the DMA Next Data Address (DNAD) register.
5. If the SCSI ATN/ signal is asserted by the initiator or if a parity error occurs during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error ATN bit in the SCSI Transfer

(SXFER) register controls whether an interrupt is generated.

Initiator Mode

In Target mode, the Opcode bit defines the following operations:

OPC	Instruction Defined
0	CHMOV
1	MOVE

These instructions perform the following steps:

1. The SYM53C710 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.
2. The SYM53C710 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the SYM53C710 has not yet transferred data by responding with an ACK/.
3. The SYM53C710 compares the SCSI phase bits in the DMA Command (DCMD) register with the latched SCSI phase lines stored in the SCSI Status Two (SSTAT2) register. These phase lines are latched when REQ/ is asserted.
4. If the SCSI phase bits match the value stored in the SCSI Status Two (SSTAT2) register, the SYM53C710 transfers the number of bytes specified in the DMA Byte Counter (DBC) register starting at the address pointed to by the DMA Next Data Address (DNAD) register.
5. If the SCSI phase bits do not match the value stored in the SCSI Status Two (SSTAT2) register, the SYM53C710 generates a phase mismatch interrupt and the command is not executed.

SCSI Phase **[26:24]**

This 3-bit field defines the desired SCSI information transfer phase. When the SYM53C710 operates in initiator mode, these bits are compared with the latched SCSI phase bits in the SCSI Status Two (SSTAT2) register. When the SYM53C710 operates in target mode, the SYM53710 asserts the phase defined in this field.

The following table describes the possible combinations and the corresponding SCSI phase.

Table 5.1 SCSI Information Transfer Phase

MSG	C_D	I_O	SCSI Phase
0	0	0	Data-Out
0	0	1	Data-In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved-Out
1	0	1	Reserved-In
1	1	0	Message-Out
1	1	1	Message-In

Transfer Counter [23:0]

This 24-bit field specifies the number of data bytes to be moved between the SYM53C710 and system memory. The field is stored in the DMA Byte Counter (DBC) register. When the SYM53C710 transfers data to or from memory, the DMA Byte Counter (DBC) register is decremented by the number of bytes transferred. In addition, the DMA Next Data Address (DNAD) register is incremented by the number of bytes transferred. This process is repeated until the DMA Byte Counter (DBC) register has been decremented to zero. At that time, the SYM53C710 fetches the next instruction.

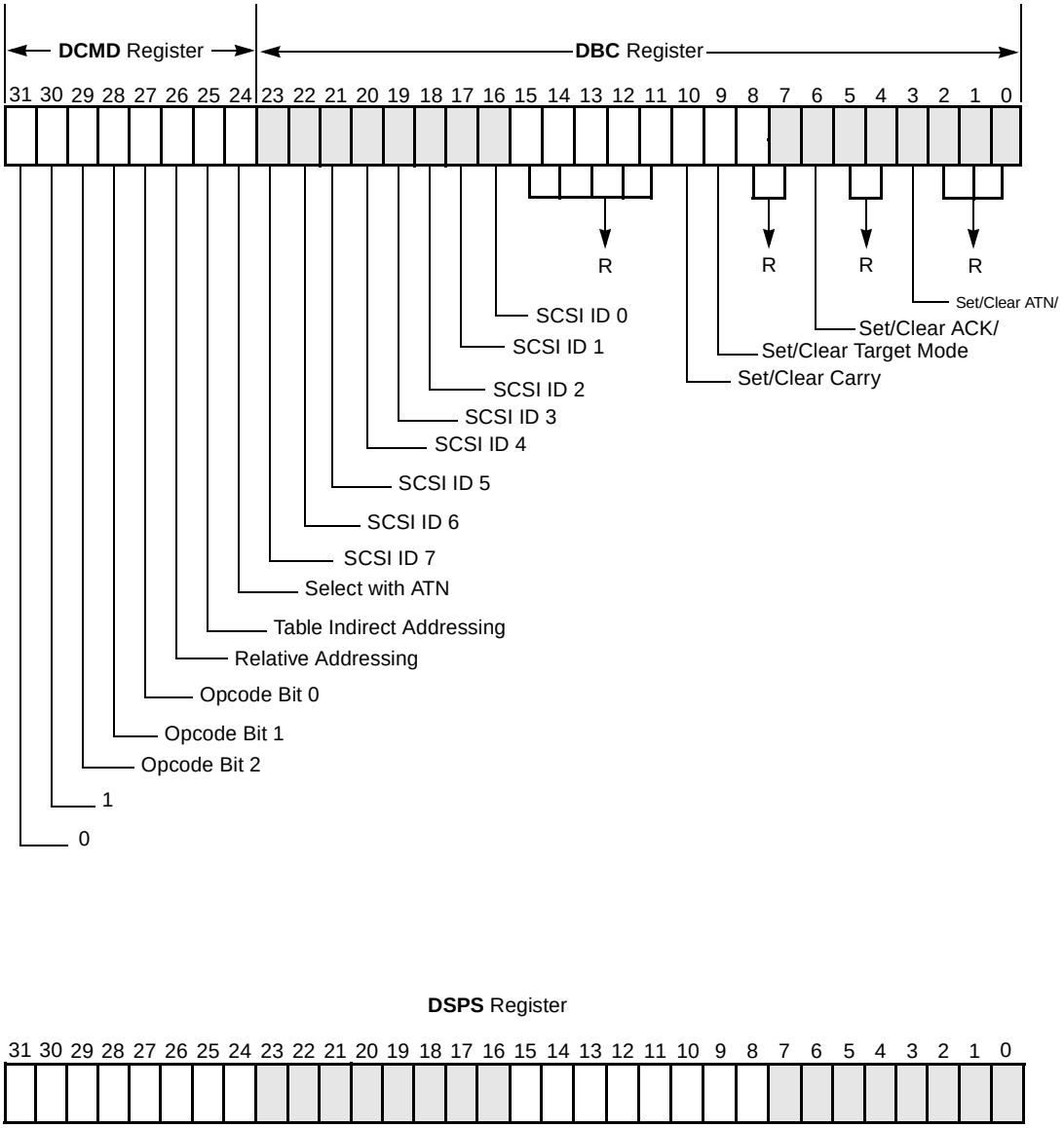
Start Address [31:0]

This 32-bit field specifies the starting address of the data to be moved to or from memory. This field is copied to the DMA Next Data Address (DNAD) register. When the SYM53C710 transfers data to or from memory, the DMA Next Data Address (DNAD) register is incremented by the number of bytes transferred.

5.2 I/O Instructions

Figure 5.2 describes the I/O Instruction register.

Figure 5.2 I/O Instruction Register



Instruction Type - I/O Instruction **[31:30]**

Opcode **[29:27]**

The Opcode bits have different meanings, depending on whether the SYM53C710 is operating in initiator or target mode. Opcode values 101 through 111 are not reserved, but are considered Read/Write instructions rather than I/O, and are discussed in the Read/Write Instructions section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1. The SYM53C710 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCSI Chip ID (SCID) register. If the SYM53C710 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the SYM53C710 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the SYM53C710 has won arbitration, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.
3. If the SYM53C710 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. The SYM53C710 automatically configures itself to be in the initiator mode if it is reselected, or the target mode if it is selected, provided the SYM53C700 compatibility bit (bit 0 in the DMA Control (DCNTL) is set. For more information, please refer to the Section 2.7.2, “Select/Reselect During

Selection/Reselection” of Chapter 2, “Functional Description”.

Disconnect Instruction

The SYM53C710 disconnects from the SCSI bus by deasserting all SCSI signal outputs. The SCSI direction control signals are deasserted, which disables the differential pair output drivers.

Wait Select Instruction

1. If the SYM53C710 is selected, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.
2. If reselected, the SYM53C710 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. The SYM53C710 automatically configures into initiator mode when reselected, provided the SYM53C700 compatibility bit (bit 0 in the DMA Control (DCNTL) register) is set. For more information, please refer to the Section 2.7.2, “Select/Reselect During Selection/Reselection” of Chapter 2, “Functional Description”.
3. If the CPU sets the SIGP bit in the Interrupt Status (ISTAT) register, the SYM53C710 will abort the WAIT SELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SCSI Output Control Latch (SOCL) register are set. ACK/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCSI Control Zero (SCNTL0) register is also set. When the carry bit is set, the corresponding bit in the ALU is set.

Note: None of the signals are affected on the SCSI bus in target mode.

Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SCSI Output Control Latch (SOCL) register. ATN/ should not be cleared except for testing purposes. When the target bit is cleared, the corresponding bit in the SCSI Control Zero (SCNTL0) register is also cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Note: None of the signals are affected on the SCSI bus in target mode.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1. The SYM53C710 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCSI Chip ID (SCID) register. If the SYM53C710 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the SYM53C710 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. It then fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.
3. If the SYM53C710 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. The SYM53C710 automatically configures itself to initiator mode if it is reselected, or to target mode if it is selected, provided the SYM53C700 compatibility bit (bit 0 in the DMA Control (DCNTL)) is set. For more information,

please refer to the Section 2.7.2, “Select/Reselect During Selection/Reselection” of Chapter 2, “Functional Description”.

4. If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

Wait Reselect Instruction

The SYM53C710 waits for the target to perform a “legal” disconnect from the SCSI bus. A “legal” disconnect occurs when BSY/ and SEL/ are inactive for a minimum of one Bus Free Delay (400 ns), after the SYM53C710 has received a Disconnect Message or a Command Complete Message.

Wait Reselect Instruction

1. If the SYM53C710 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register. The SYM53C710 automatically configures itself to be in target mode when selected, provided the SYM53C700 compatibility bit (bit 0 in the DMA Control (DCNTL)) is set. For more information, please refer to the Section 2.7.2, “Select/Reselect During Selection/Reselection” of Chapter 2, “Functional Description”.

2. If the SYM53C710 is reselected, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.

3. If the CPU sets the SIGP bit in the Interrupt Status (ISTAT) register, the SYM53C710 aborts the Wait Reselect instruction and fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Data Address (DNAD) register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SCSI Output Control Latch (SOCL) register are set. ACK/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCSI Control Zero (SCNTL0) register is also set. When

the carry bit is set, the corresponding bit in the ALU is set.

Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SCSI Output Control Latch (SOCL) register. ATN/ should not be cleared except for testing purposes. When the target bit is cleared, the corresponding bit in the SCSI Control Zero (SCNTL0) register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Relative Addressing Mode **26**

When this bit is set, the 24-bit signed value in the DMA Next Data Address (DNAD) register is used as a relative displacement from the current DSP address.

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Table Indirect Mode **25**

When this bit is set, the 24-bit signed value in the DMA Byte Counter (DBC) register is used as an offset relative to the value in the Data Structure Address (DSA) register. The SCSI ID, synchronous offset and synchronous period are loaded from this address.

Prior to the start of an I/O, the DSA must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data. Both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory.

- The I/O data structure must lie within the 8 Mbyte above or below the base address.
- An I/O command structure must have all four bytes contiguous in system memory, as shown below. The DHP/period/offset bits are ordered as in the SCSI Transfer (SXFER) register.

00	ID	DH/period/offset	00

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 or 26 may be set individually or in combination.

Bit 25	Bit 26	Addressing Mode
0	0	Direct
0	1	Table Indirect
1	0	Relative
1	1	Table Relative

Direct

Uses the device ID and physical address in the command.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect

Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative

Uses the device ID in the command, but treats the alternate address as a relative jump.

Command	ID	Not Used	Not Used
xx	Alternate Jump Offset		

Table Relative

Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits [23:0] of the first four bytes of the SCRIPTS to the data structure base address to form the fetch address.

Command	Table Offset
xx	Alternate Jump Offset

Select with ATN/ **24**
This bit specifies whether ATN/ will be asserted during the selection phase when the SYM53C710 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

SCSI Destination ID **[23:16]**
This 8-bit field specifies the destination SCSI ID for an I/O instruction. Only one bit may be set in this field.

Set/Clear Carry **10**
This bit is used in conjunction with a Set or Clear command to set or clear the Carry bit. Setting this bit with a Set command asserts the Carry bit in the ALU. Clearing this bit with a set command deasserts the Carry bit in the ALU.

Set/Clear Target Mode **9**
This bit is used in conjunction with a Set or Clear command to set or clear target mode. Setting this bit with a Set command configures the SYM53C710 as a target device (this sets bit 0 of the SCSI Control Zero (SCNTL0) register). Setting this bit with a Clear command configures the SYM53C710 as an initiator device (this clears bit 0 of the SCSI Control Zero (SCNTL0) register).

Set/Clear ACK/ **6**

Set/Clear ATN/ **3**

These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal, bit 3 controls the SCSI ATN/ signal.

Setting either of these bits sets or resets the corresponding bit in the SCSI Output Control Latch (SOCL) register, depending on the command used. The Set command is used to assert ACK/ and/or ATN/ on the SCSI bus. The Clear command is used to deassert ACK/ and/or ATN/ on the SCSI bus.

Since ACK/ and ATN/ are initiator signals, they are not asserted on the SCSI bus unless the SYM53C710 is operating as an initiator or the SCSI Loopback Enable bit is set in the Chip Test Four (CTEST4) register.

The Set/Clear SCSI ACK/ATN instruction is used after message phase Block Move operations, to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction.

Reserved **[2:0]**

Jump Address **[31:0]**

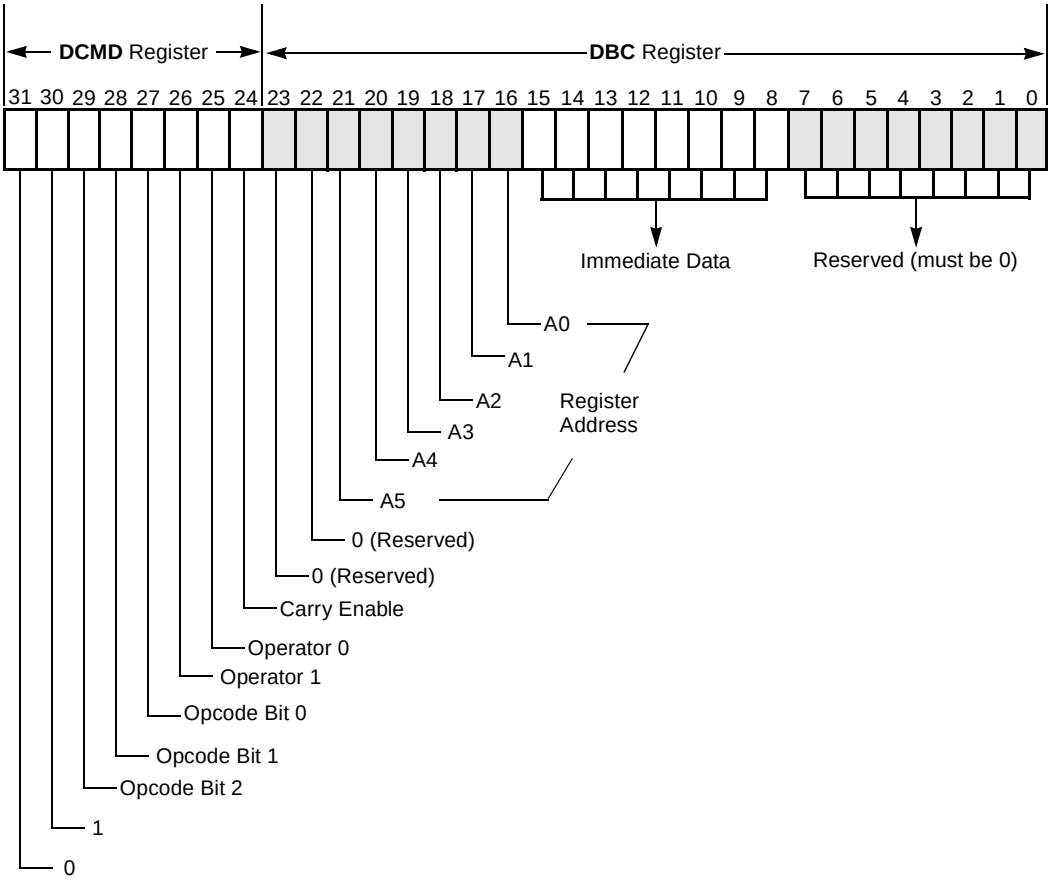
This 32-bit field specifies the address of the instruction to fetch when the SYM53C710 encounters a jump condition. The SYM53C710 fetches instructions from the address pointed to by this field whenever the SYM53C710 encounters a SCSI condition that is different from the condition specified in the instruction.

For example, during the execution of a Select instruction in initiator mode, if the SYM53C710 is reselected, then the next instruction is fetched from the address pointed to by the jump address field. For a complete description of the different jump conditions, refer to the description of each instruction.

5.3 Read/Write Instructions

Figure 5.3 describes the Read/Write Instruction register.

Figure 5.3 Read/Write Instruction Register



DSPS Register

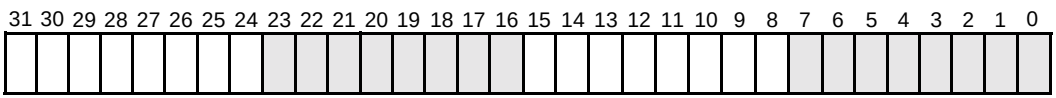


Table 5.2 Read/Write Instructions

Operator Bits [26:25]	Opcode 111 Read-Modify-Write	Opcode 110 Move to SFBR	Opcode 101 Move from SFBR
00	Immediate data to destination register	Immediate data to SCSI First Byte Received (SFBR)	Immediate data to destination register
01	Immediate data OR'ed with destination register	Immediate data OR register to SCSI First Byte Received (SFBR)	Immediate data OR'ed with SCSI First Byte Received (SFBR) to destination register
10	Immediate data AND'ed with destination register	Immediate data AND register to SCSI First Byte Received (SFBR)	Immediate data AND'ed with SCSI First Byte Received (SFBR) to destination register
11	Immediate data added to destination register	Immediate data added with register to SCSI First Byte Received (SFBR)	Immediate data added with SCSI First Byte Received (SFBR) to destination register

Instruction Type - Read/Write Instruction [31:30]

Opcode [29:27]
The combinations of these bits determine if the instruction is a Read/Write or I/O instruction. Opcodes 000 through 100 are considered I/O instructions.

Operator [26:25]

Carry Enable 24
When this bit is set, it allows the previous carry value to be used by the present Add instruction. The carry value remains intact unless it is modified by an Add, Set Carry or Clear Carry instruction. All other instructions do not affect Carry. If Carry Enable is not set, no carry is used during the present Add instruction.

Register Address - A[5:0] [21:16]
Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A[5:0] select an 8-bit source/destination register within the SYM53C710. Register addresses are always written using little endian byte orientation.

5.3.1 Read-Modify-Write Cycles

In this cycle, the register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

5.3.2 Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SCSI First Byte Received (SFBR). The possible functions of this command are:

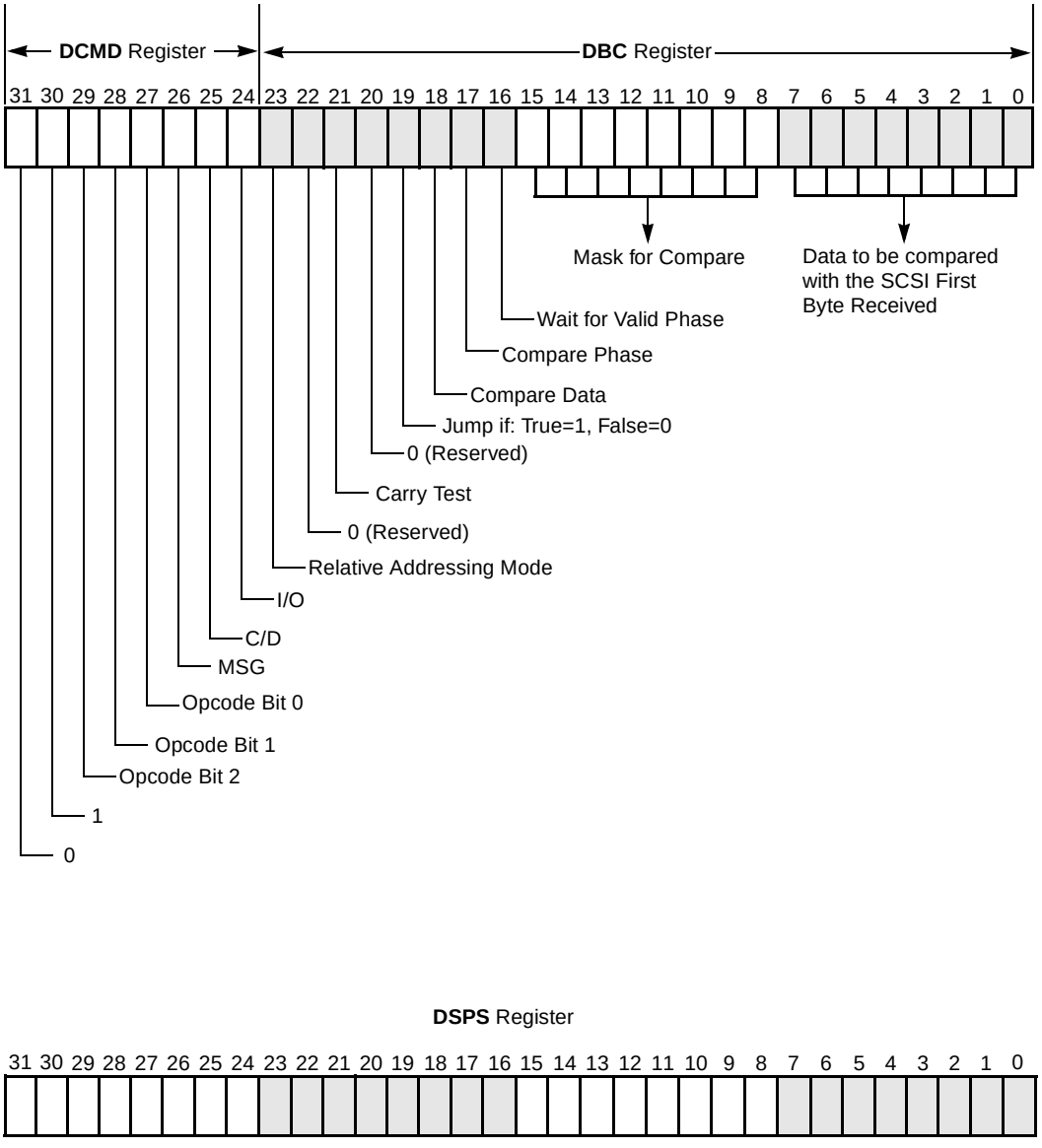
- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SCSI First Byte Received (SFBR) from/to any other register.
- Alter the value of a register with AND/OR/ADD operators.
- After moving values to the SFBR, the compare and jump, call, or similar commands may be used to check the value.
- A Move to SFBR followed by a Move from SFBR can be used to perform a register to register move.

  Note: Because the Interrupt Status (ISTAT) register is a shadowed register, it cannot be accessed using the Read/Write instruction. To move the Interrupt Status (ISTAT) register to the SFBR, use a Memory Move to transfer the ISTAT to SCRATCH1, then perform a SCRATCH to SFBR Move.

5.4 Transfer Control Instructions

Figure 5.4 describes the Transfer Control Instruction register.

Figure 5.4 Transfer Control Instruction Register



DSPS Register

Instruction Type - Transfer Control Instruction **[31:30]**

Opcode **[29:27]**

This 3-bit field specifies the type of transfer control instructions to be executed. All transfer control instructions can be dependent on a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

Table 5.3 Transfer Control Instructions

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	x	x	Reserved

Jump Instruction

The SYM53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the SYM53C710 loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register. The DMA SCRIPTS Pointer (DSP) register now contains the address of the next instruction.

If the comparisons are false, the SYM53C710 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register, leaving the instruction pointer unchanged.

Call Instruction

The SYM53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the SYM53C710 loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register and that address value becomes the address of the next instruction.

When the SYM53C710 executes a Call instruction, the instruction pointer contained in the DMA SCRIPTS Pointer (DSP) register is stored in the Temporary Stack (TEMP) register.

When a Return instruction is executed, the value stored in the Temporary Stack (TEMP) register is returned to the DMA SCRIPTS Pointer (DSP) register.

If the comparisons are false, the SYM53C710 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register and the instruction pointer is not modified.

Note: The Memory Move instruction destroys the return address stored in the Temporary Stack (TEMP) register.

Return Instruction

The SYM53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the SYM53C710 loads the DMA SCRIPTS Pointer (DSP) register with the contents of the Temporary Stack (TEMP) register. That address value becomes the address of the next instruction.

When the SYM53C710 executes a Call instruction, the current instruction pointer contained in the DMA SCRIPTS Pointer (DSP) register is stored in the Temporary Stack (TEMP) register.

When a Return instruction is executed, the value stored in the Temporary Stack (TEMP) register is returned to the DMA SCRIPTS Pointer (DSP) register.

The SYM53C710 does not check to see whether the Call instruction has already been executed. It does not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

If the comparisons are false, then the SYM53C710 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register and the instruction pointer is not modified.

Note: The Memory Move instruction destroys the return address stored in the Temporary Stack (TEMP) register.

Interrupt Instruction

The SYM53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the SYM53C710 generates an interrupt by asserting the IRQ/ signal.

The 32-bit address field stored in the DMA SCRIPTS Pointer Save (DSPS) register can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.

The SYM53C710 halts and the DMA SCRIPTS Pointer (DSP) register must be written to start any further operation.

SCSI Phase **[26:24]**

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the SYM53C710 is operating in initiator mode. When the SYM53C710 is operating in the target mode, these bits should be cleared.

Table 5.4 SCSI Phase Comparisons

MSG	C/D	I/O	SCSI Phase
0	0	0	Data-Out
0	0	1	Data-In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved-Out
1	0	1	Reserved-In
1	1	0	Message-Out
1	1	1	Message-In

Relative Addressing Mode **23**

When this bit is set, the 24-bit signed value in the DMA SCRIPTS Pointer Save (DSPS) register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address

Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address

Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
xx	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPTS routine currently being executed by the SYM53C710. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (2's complement), the jump can be forward or backward.

A relative transfer can be made to any address within a 16 Mbyte segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPTS is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

Reserved **22**

Carry Test **21**
When this bit is set, decisions based on the ALU Carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Reserved **20**

Jump If True/False **19**
This bit determines whether the SYM53C710 should branch when a comparison is true or when a comparison is false. This bit applies to both Phase Compares and Data Compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Result of Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Compare Data **18**
When this bit is set, then the first byte received from the SCSI data bus (contained in SCSI First Byte Received (SFBR) register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Compare Phase **17**
When the SYM53C710 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ/) are compared to the Phase Field in the Transfer Control instruction. If they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur.

When the SYM53C710 is operating in target mode this bit, when set, tests for an active SCSI ATN/ signal.

Wait for Valid Phase **16**
If the Wait for Valid Phase bit is set, then the SYM53C710 waits for a previously unserviced phase before comparing the SCSI phase and data.

If the Wait for Valid Phase bit is clear, then the SYM53C710 compares the SCSI phase and data immediately.

Data Compare Mask **[15:8]**
The Data Compare Mask allows a SCRIPTS to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored.

For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is on while ignoring the remaining bits.

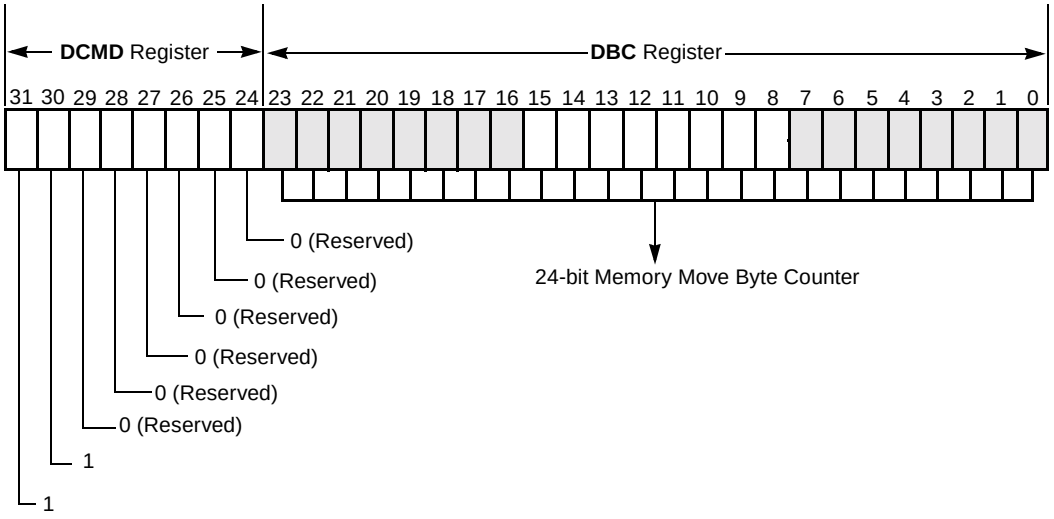
Data Compare Value **[7:0]**
This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

Jump Address **[31:0]**
This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the SYM53C710 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by four, loaded into the DMA SCRIPTS Pointer (DSP) register and becomes the current instruction pointer.

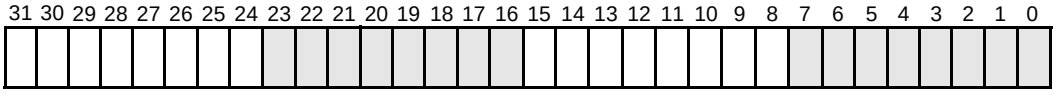
5.5 Memory Move Instructions

Figure 5.5 describes the Memory Move Instruction register.

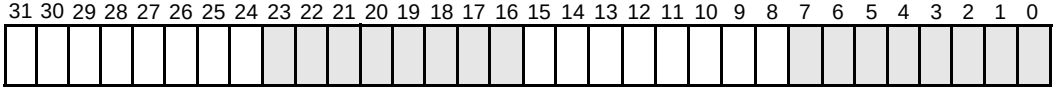
Figure 5.5 Memory Move Instruction Register



DSPS Register



TEMP Register



The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the SYM53C710 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than current DMA controllers. Up to 16 Mbytes may be transferred with one instruction. There are three restrictions:

- Both the source and destination addresses must start with the same address alignment (A[1:0] must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur. If cache line bursting is enabled, address lines A[3:0] must be the same.
- During execution of this opcode, TEMP and DSA are destroyed. Therefore, if the contents of either register are required for additional SCRIPTS, save them before any Memory Move is executed. Before resuming a SCSI SCRIPTS, restore the contents of the appropriate register.
- Indirect addresses are not allowed.

The Memory-to-Memory Move instruction passes the source and destination addresses and the byte count to the SYM53C710. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPTS is fetched from system memory.

The DMA SCRIPTS Pointer Save (DSPS) and Data Structure Address (DSA) registers are additional holding registers used during the Memory Move.

Instruction Type - Memory Move Instruction [31:30]

Reserved [29:24]
These bits are reserved and must be zero. If any of these bits are set, an illegal instruction interrupt will occur.

Transfer Count [23:0]
The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

5.5.1 Read/Write System Memory from SCRIPTS

By using the Memory Move instruction, single or multiple register values may be transferred to or from system memory.

Because the Chip Select (CS/) input is derived from an address decode, it could activate during a Memory Move operation if the source/destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower 6 bits of the memory address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable using the CPU, and therefore not by a Memory Move. However, it can be loaded using SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate SYM53C710 register (for example, the Scratch (SCRATCH)), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

Note: DSA can be the destination register of a memory-to-memory transfer, but not the source.

Chapter 6
Electrical Specifications

This chapter contains the following sections:

6.1 DC Characteristics

This section of the manual describes the SYM53C710 DC Characteristics. Table 6.1 through Table 6.10 give current and voltage specifications.

Table 6.1 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Units
T_{STG}	Storage temperature	–55	150	°C
V_{DD}	Supply voltage	–0.5	7.0	V
V_{IN}	Input voltage	V_{SS} –0.5	V_{DD} +0.5	V
I_{LU}	Latch-up current	–2 V < V_{PIN} < +8 V	±150	mA
ESD[2]	Electrostatic discharge	–	2 K	V

1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or at any other conditions beyond those indicated in the Operating Conditions section of this specification is not implied.
2. Measured according to MIL-STD-883C, Method 3015.7.

Table 6.2 Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply voltage	4.75	5.25	V
I_{DD}	Supply current (static)	–	1	mA
I_{DD}	Supply current (dynamic) - SYM53C710	–	50	mA
I_{DD}	Supply current (dynamic) - SYM53C710-1	–	60	mA
T_A	Operating temperature (free air)	0	70	°C
Θ_{JA}	Thermal resistance[1] (junction to ambient air)	–	46	°C/W
P_{DD}	Power dissipation	–	0.26	W

1. 160-pin, QFP only.

Table 6.3 SCSI Signals (Open Drain)—SD[7:0], SDP/, REQ/, MSG/, I_O/, C_D/, ATN/, ACK/, BSY/, SEL/, RST/

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
V_{HYS}	Hysteresis	300	–	mV	–
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
I_{IN}	Input leakage current	–10	10	µA	–
I_{NR}	Input leakage (SCSI RST)	–200	50	µA	–
I_{OZ}	3-state leakage current	–10	10	µA	–

Table 6.4 Input Signals—BG/, BOFF/, RESET/, CS/, BS, BIG-LIT/, BCLK, SCLK

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
I_{IN}	Input leakage current	–1.0	1.0	µA	–

Table 6.5 Output Signals (Totem Pole)—SDIR[7:0], SDIRP, BSYDIR, SELDIR, RSTDIR, TGS, IGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –4 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 4 mA
I_{OH}	Output high current	–2.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	4.0	–	mA	V_{OL} = 0.4 V

Table 6.6 Output Signals (Totem Pole)—FETCH/, IRQ/

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 8mA
I_{OH}	Output high current	–4.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	8.0	–	mA	V_{OL} = 0.4 V

Table 6.7 Output Signals (Totem Pole)—SLACK/, MASTER

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 16 mA
I_{OH}	Output high current	–8.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	16.0	–	mA	V_{OL} = 0.4 V

Table 6.8 3-State Output Signals—A[31:6], FC[2:0], SC[1:0], UPSO-TT0/, CBREQ/-TT1/, BR/

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 16 mA
I_{OH}	Output high current	–8.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	16.0	–	mA	V_{OL} = 0.4 V
I_{OZ}	3-state leakage current	–10	10	µA	–

Table 6.9 Bidirectional Signals (Totem Pole Outputs)—A[5:0], D[31:0], DP[3:0], DS/-DLE, AS/-TS/, RW/, SIZ[1:0], BERR/-TEA/, HALT/-TIP/, BGACK-BB/, CBACK/-TBI/, STERM/-TA/

Symbol	Parameter	Min	Max	Units	Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	I_{OH} = –16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	I_{OL} = 16 mA
I_{OH}	Output high current	–8.0	–	mA	$V_{OH} = V_{DD}$ –0.5 V
I_{OL}	Output low current	16.0	–	mA	V_{OL} = 0.4 V
I_{IN}	Input leakage current	–10	10	µA	–
I_{OZ}	3-state leakage current	–10	10	µA	–

Table 6.10 Capacitance

Symbol	Parameter	Min	Max	Units	Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

6.2 Symbios TolerANT Specifications

Table 6.11 TolerANT Active Negation Technology Electrical Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}[2]	Output high voltage	2.5	3.1	3.5	V	I_{OH} = 2.5 mA
V_{OL}	Output low voltage	0.1	0.2	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	–	7.0	V	–
V_{IL}	Input low voltage	–0.5	–	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.74	–0.77	V	V_{DD} = min; I_I = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.1	1.2	1.3	V	–
V_{TL}	Threshold, LOW to HIGH	1.5	1.6	1.7	V	–
V_{TH}-V_{TL}	Hysteresis	300	350	400	mV	–
I_{OH}[2]	Output high current	2.5	15	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	150	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	–	625	mA	Output driving low, pin shorted to V_{DD} supply[3]
I_{OSL}	Short-circuit output low current	–	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	0.05	10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–	–0.05	–10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 0.5 V
R_I	Input resistance	–	20	–	MΩ	SCSI pins[4]
C_P	Capacitance per pin	6	8	10	pF	QFPP
t_R[2]	Rise time, 10% to 90%	9.7	15.0	18.5	ns	Figure 6.1
t_F	Fall time, 90% to 10%	5.2	8.1	14.7	ns	Figure 6.1
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.23	0.49	V/ns	Figure 6.1
dV_L/dt	Slew rate, HIGH to LOW	0.19	0.37	0.67	V/ns	Figure 6.1
	Electrostatic discharge	2	–	–	KV	MIL-STD-883C; 3015.7
	Latch-up	100	–	–	mA	–
	Filter delay	20	25	30	ns	Figure 6.2
	Extended filter delay	40	50	60	ns	Figure 6.2

1. These values are guaranteed by period characterization.
2. Active Negation outputs only: Data, Parity, REQ, ACK.
3. Single pin only. Irreversible damage may occur if sustained for one second.
4. SCSI RESET pin has 10 KΩ pull-up resistor.

Figure 6.1 Rise and Fall Time Test Conditions

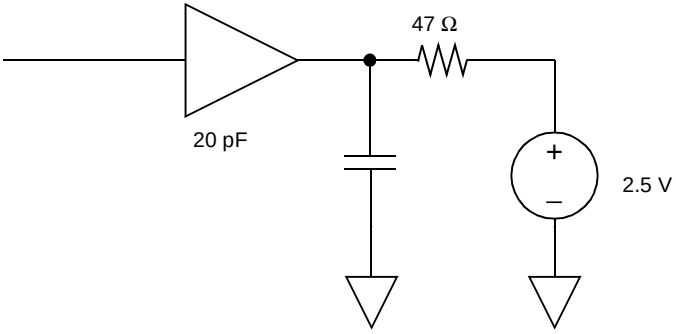
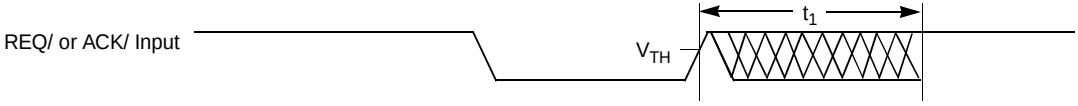


Figure 6.2 SCSI Input Filtering



Note: t_1 is the input filtering period, register programmable to either 30 or 60 ns.

Figure 6.3 Hysteresis of SCSI Receiver

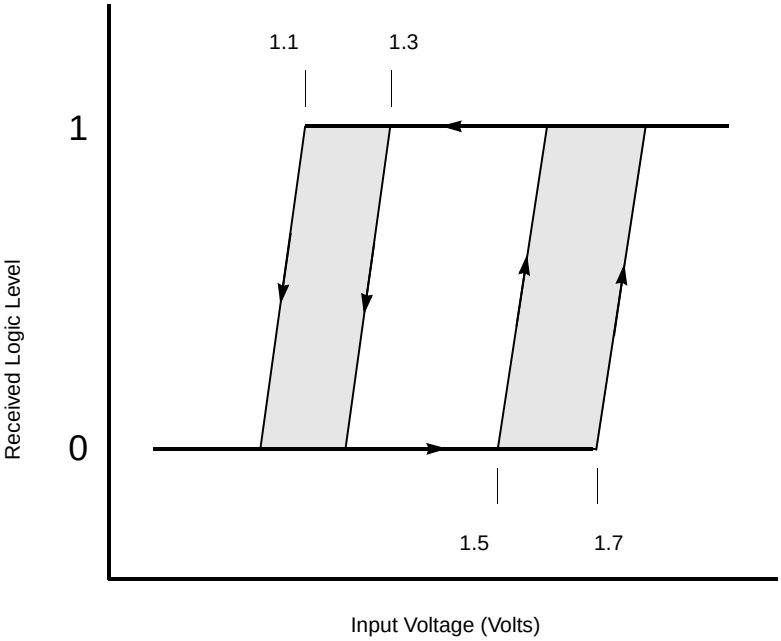


Figure 6.4 Input Current as a Function of Input Voltage

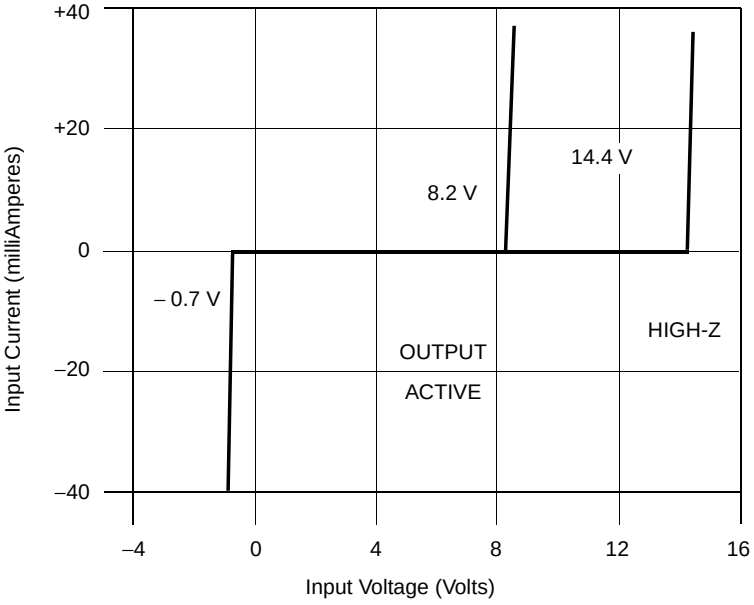
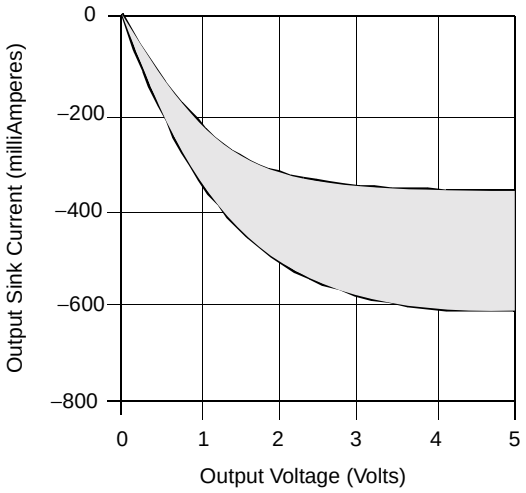
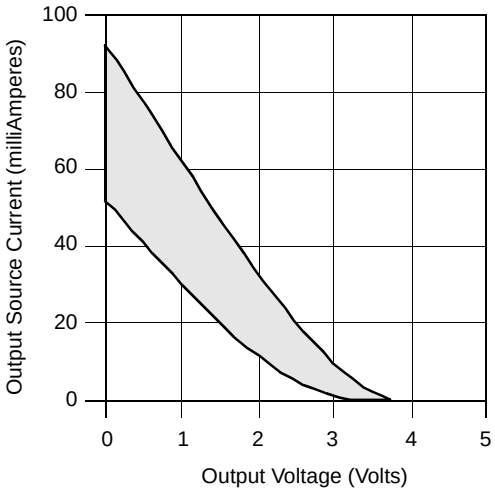


Figure 6.5 Output Current as a Function of Output Voltage





6.3 AC Specifications

The AC characteristics described in this section apply over the operating voltage and temperature range, 4.75 > VDD > 5.25 V and 0 °C > TA < 70 °C. Output timings are based on worst case conditions (4.75 V, 70 °C) and worst case processing using the following termination. The simulation load of the I/O pads is 120 pF, all timings in the specification are taken from the 10% and 90% points with respect to the specified VOL and VOH of the waveforms.

Figure 6.6 Clock Timing

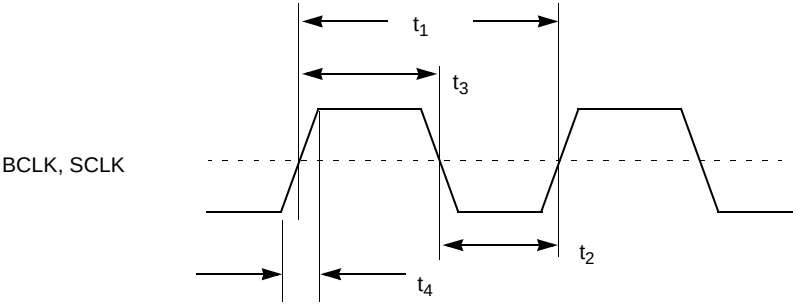


Table 6.12 SYM53C710 Bus Mode 1 Clock Timings

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time (t_{BCLK})	40	DC	ns
	SCSI clock cycle time (t_{SCLK})[1]	15	60	ns
t_2	BCLK LOW time[2]	17	–	ns
	SCLK LOW time[2]	7	–	ns
t_3	BCLK HIGH time[2]	17	–	ns
	SCLK HIGH time[2]	7	–	ns
t_4	BCLK slew rate	1	–	V/ns
	SCLK slew rate	1	–	V/ns

1. This parameter must be met to ensure SCSI timings are within specification.
2. Duty cycle not to exceed 60/40.

Table 6.13 SYM53C710 Bus Mode 2 Clock Timings

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time (t_{BCLK})	30	DC	ns
	SCSI clock cycle time (t_{SCLK})[1]	15	60	ns
t_2	BCLK LOW time[2]	14	–	ns
	SCLK LOW time[2]	7	–	ns
t_3	BCLK HIGH time[2]	14	–	ns
	SCLK HIGH time[2]	7	–	ns
t_4	BCLK slew rate	1	–	V/ns
	SCLK slew rate	1	–	V/ns

1. This parameter must be met to ensure SCSI timings are within specification.
2. Duty cycle not to exceed 60/40.

Table 6.14 SYM53C710-1 Bus Mode 1 Clock Timings

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time (t_{BCLK})	30	DC	ns
	SCSI clock cycle time (t_{SCLK})[1]	15	60	ns
t_2	BCLK LOW time[2]	13	–	ns
	SCLK LOW time[2]	7	–	ns
t_3	BCLK HIGH time[2]	13	–	ns
	SCLK HIGH time[2]	7	–	ns
t_4	BCLK slew rate	1	–	V/ns
	SCLK slew rate	1	–	V/ns

1. This parameter must be met to ensure SCSI timings are within specification.
2. Duty cycle not to exceed 60/40.

Table 6.15 SYM53C710-1 Bus Mode 2 Clock Timings

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time (t_{BCLK})	25	DC	ns
	SCSI clock cycle time (t_{SCLK})[1]	15	60	ns
t_2	BCLK LOW time[2]	11	–	ns
	SCLK LOW time[2]	7	–	ns
t_3	BCLK HIGH time[2]	11	–	ns
	SCLK HIGH time[2]	7	–	ns
t_4	BCLK slew rate	1	–	V/ns
	SCLK slew rate	1	–	V/ns

1. This parameter must be met to ensure SCSI timings are within specification.
2. Duty cycle not to exceed 60/40.

Figure 6.7 Chip Reset Timing Waveforms

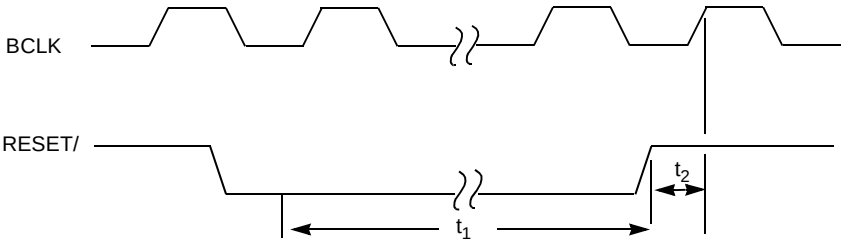


Table 6.16 Chip Reset Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	Reset pulse width	10	–	BCLK
t_2	Reset deasserted setup to BCLK HIGH	10	–	ns

1. This timing is only required to ensure clock-for-clock repeatability after RESET/ is deasserted.

Figure 6.8 IRQ Timing Waveforms

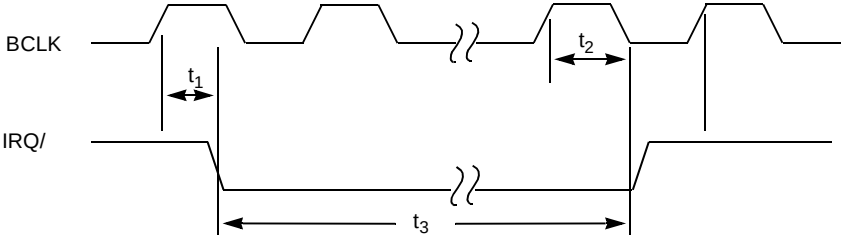


Table 6.17 IRQ Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to IRQ/ asserted	–	20	ns
t_2	BCLK HIGH to IRQ/ deasserted	–	58	ns
t_3	IRQ/ assertion time	3	–	BCLK

6.4 Bus Mode 1 Slave Cycle

6.4.1 Bus Mode 1 Slave Read Sequence

1. The Read/Write, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the SYM53C710 on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the SYM53C710.
5. Two clock cycles of wait state are inserted and the Data lines are asserted by the SYM53C710.
6. Slave Acknowledge is asserted by the SYM53C710 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. Synchronous cycle termination is asserted by memory.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the SYM53C710, and the Data lines are 3-stated by the SYM53C710.

Table 6.18 SYM53C710 Bus Mode 1 Slave Read Timings

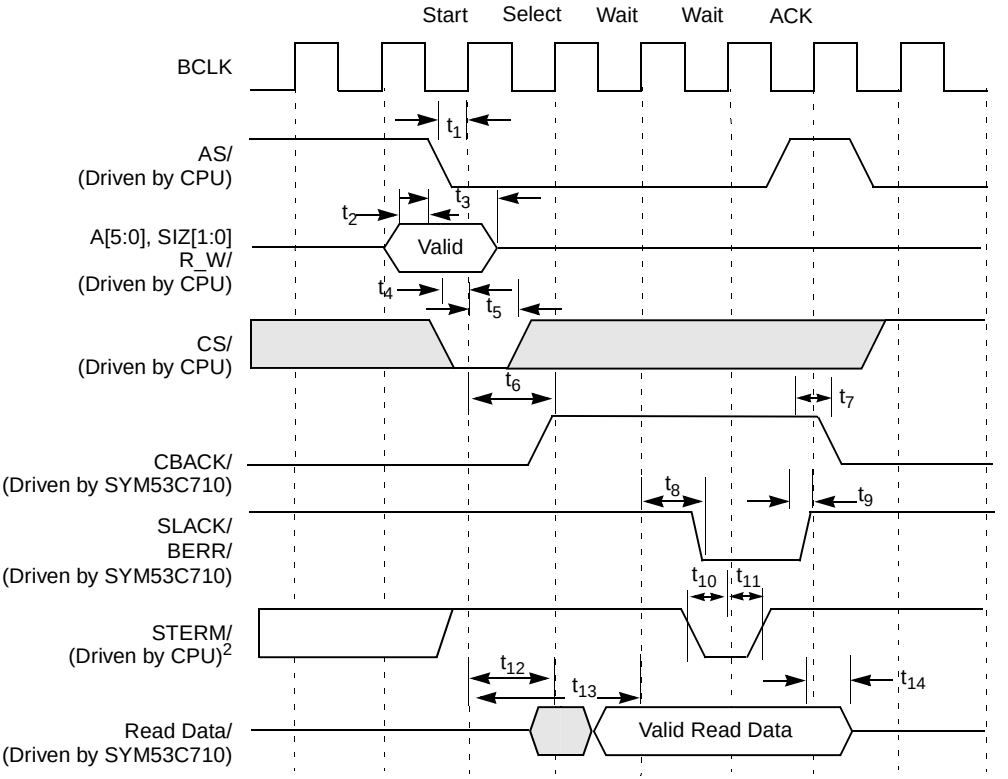
Symbol	Parameter	Min	Max	Units
t_1	AS/ setup to CS/ clocked active	5	–	ns
t_2	A[5:0], SIZ[1:0], R_W/ setup to AS/	4	–	ns
t_3	A[5:0], SIZ[1:0], R_W/ hold from AS/	8	–	ns
t_4	CS/ setup to BCLK HIGH after AS/	5	–	ns
t_5	CS/ hold from BCLK HIGH after AS/	5	–	ns
t_6	BCLK HIGH to CBACK/ HIGH	5	26	ns
t_7	AS/ HIGH to CBACK/ LOW	3	17	ns
t_8	BCLK HIGH to SLACK/, BERR/ LOW	–	22	ns
t_9	AS/ HIGH to SLACK/, BERR/ HIGH	–	22	ns
t_{10}	STERM/ (input) setup to BCLK HIGH	3	–	ns
t_{11}	STERM/ (input) hold from BCLK HIGH	7	–	ns
t_{12}	BCLK HIGH to data bus driven	8	28	ns
t_{13}	BCLK HIGH to read data valid	–	75	ns
t_{14}	AS/ HIGH to data bus HIGH-Z	7	28	ns

Table 6.19 SYM53C710-1 Bus Mode 1 Slave Read Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	AS/ setup to CS/ clocked active	5	–	ns
t_2	A[5:0], SIZ[1:0], R_W/ setup to AS/	4	–	ns
t_3	A[5:0], SIZ[1:0], R_W/ hold from AS/	8	–	ns
t_4	CS/ setup to BCLK HIGH after AS/	5	–	ns
t_5	CS/ hold from BCLK HIGH after AS/	5	–	ns
t_6	BCLK HIGH to CBACK/ HIGH	5	20	ns
t_7	AS/ HIGH to CBACK/ LOW	3	15	ns
t_8	BCLK HIGH to SLACK/, BERR/ LOW	–	20	ns
t_9	AS/ HIGH to SLACK/, BERR/ HIGH	–	20	ns
t_{10}	STERM/ (input) setup to BCLK HIGH	2	–	ns
t_{11}	STERM/ (input) hold from BCLK HIGH	7	–	ns
t_{12}	BCLK HIGH to data bus driven	8	28	ns
t_{13}	BCLK HIGH to read data valid	–	60	ns
t_{14}	AS/ HIGH to data bus HIGH-Z	7	28	ns

1. The SYM53C710 must see address strobes paired up with synchronous cycle terminations, even though the slave cycle may not be intended for the SYM53C710.

Figure 6.9 Bus Mode 1 Slave Read Cycle[1]



1. Shaded area indicates that the signal is a don't care.
2. This signal may be driven by the SYM53C710 if the ENABLE ACK (EA) bit is set (DCNTL, bit 5). See explanation in Chapter 2 for use of this signal as an output.

6.4.2 Bus Mode 1 Slave Write Sequence

1. The Read/Write, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the SYM53C710 on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the SYM53C710.
5. The Data lines are asserted by the CPU.
6. Slave Acknowledge is asserted by the SYM53C710 if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. STERM/ is sampled.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the SYM53C710.

Table 6.20 SYM53C710 Bus Mode 1 Slave Write Timings

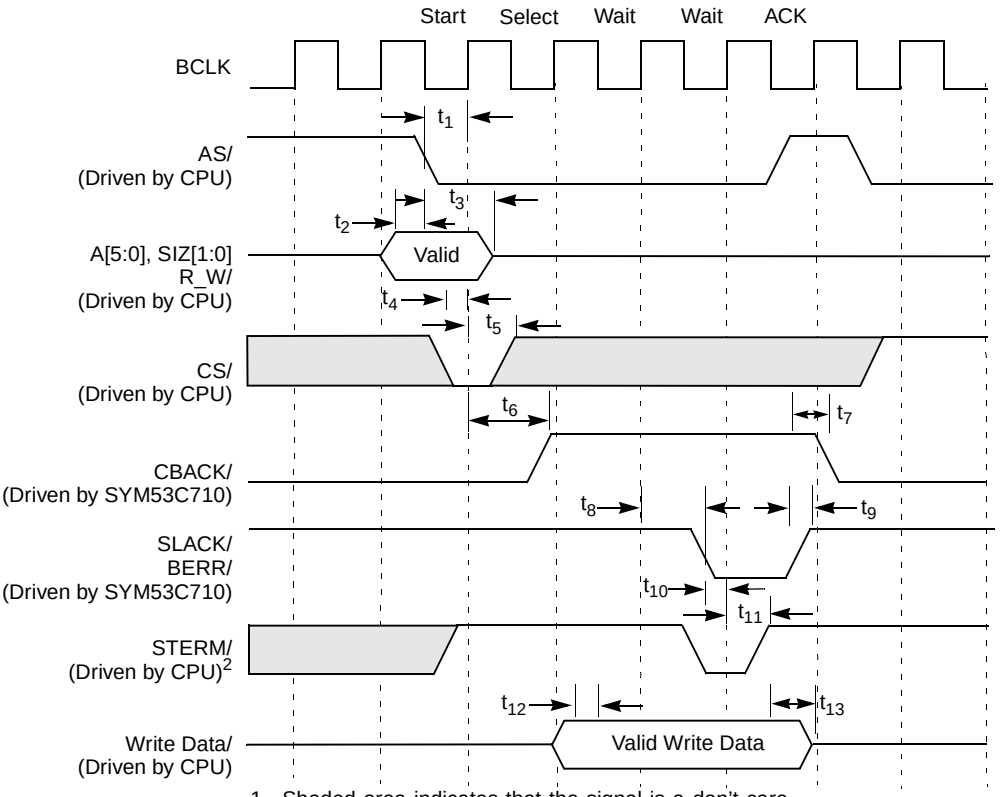
Symbol	Parameter	Min	Max	Units
t_1	AS/ setup to CS/ clocked active	5	–	ns
t_2	A[5:0], SIZ[1:0], R_W/ setup to AS/	4	–	ns
t_3	A[5:0], SIZ[1:0], R_W/ hold from AS/	8	–	ns
t_4	CS/ setup to BCLK HIGH after AS/	5	–	ns
t_5	CS/ hold from BCLK HIGH after AS/	5	–	ns
t_6	BCLK HIGH to CBACK/ HIGH	5	26	ns
t_7	AS/ HIGH to CBACK/ LOW	3	17	ns
t_8	BCLK HIGH to SLACK/, BERR/ LOW	–	22	ns
t_9	AS/ HIGH to SLACK/, BERR/ HIGH	–	22	ns
t_{10}	STERM/ (input) setup to BCLK HIGH	3	–	ns
t_{11}	STERM/ (input) hold from BCLK HIGH	7	–	ns
t_{12}	Write data setup to BCLK LOW	4	–	ns
t_{13}	Write data hold from BCLK LOW	6	–	ns

Table 6.21 SYM53C710-1 Bus Mode 1 Slave Write Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	AS/ setup to CS/ clocked active	5	–	ns
t_2	A[5:0], SIZ[1:0], R_W/ setup to AS/	4	–	ns
t_3	A[5:0], SIZ[1:0], R_W/ hold from AS/	8	–	ns
t_4	CS/ setup to BCLK HIGH after AS/	5	–	ns
t_5	CS/ hold from BCLK HIGH after AS/	5	–	ns
t_6	BCLK HIGH to CBACK/ HIGH	5	20	ns
t_7	AS/ HIGH to CBACK/ LOW	3	15	ns
t_8	BCLK HIGH to SLACK/, BERR/ LOW	–	20	ns
t_9	AS/ HIGH to SLACK/, BERR/ HIGH	–	20	ns
t_{10}	STERM/ (input) setup to BCLK HIGH	2	–	ns
t_{11}	STERM/ (input) hold from BCLK HIGH	7	–	ns
t_{12}	Write data setup to BCLK LOW	4	–	ns
t_{13}	Write data hold from BCLK LOW	6	–	ns

1. The SYM53C710 must see address strobes paired up with synchronous cycle terminations, even though the slave cycle may not be intended for the SYM53C710.

Figure 6.10 Bus Mode 1 Slave Write Cycle[1]



1. Shaded area indicates that the signal is a don't care.
2. This signal may be driven by the SYM53C710 if the ENABLE ACK (EA) bit is set (DCNTL, bit 5). See explanation in Chapter 2 for use of this signal as an output.

6.5 Host Bus Arbitration

6.5.1 Bus Arbitration Sequence

1. The SYM53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2. Bus Request is asserted.
3. The SYM53C710 waits for Bus Grant and checks that Bus Grant Acknowledge is deasserted. Then the SYM53C710 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request on the next rising edge of BCLK.

Table 6.22 SYM53C710 Bus Mode 1 Host Bus Arbitration Timings[1]

Symbol	Parameter	Min	Max	Unit
t_1	SC0 HIGH to BR/ LOW[2]	1	2	BCLK
t_2	BCLK HIGH to SC0 LOW on start phase of last cycle[2]	5	28	ns
t_3	BCLK HIGH to BR/ LOW	4	20	ns
t_4	BCLK HIGH to BR/ HIGH	5	25	ns
t_5	BG/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_6	BG/ hold from BCLK HIGH (any rising edge after BR/)	5	–	ns
t_7	BGACK/ setup to BCLK HIGH (any rising edge after BR/)	5	–	ns
t_8	BCLK HIGH to BGACK/ LOW	4	24	ns
t_9	BCLK HIGH to BGACK/ HIGH	3	15	ns
t_{10}	BCLK HIGH to BGACK/ HIGH-Z	7	32	ns
t_{11}	BCLK HIGH to MASTER/ LOW	5	22	ns
t_{12}	BCLK HIGH to MASTER/ HIGH	6	26	ns
t_{13}	BCLK HIGH to FETCH/ LOW	5	36	ns
t_{14}	BCLK HIGH to FETCH/ HIGH	5	36	ns
t_{15}	FETCH/ LOW to BR/ LOW	1	2	BCLK
t_{16}	BGACK/ HIGH to FETCH/ HIGH[3]	1	2	BCLK

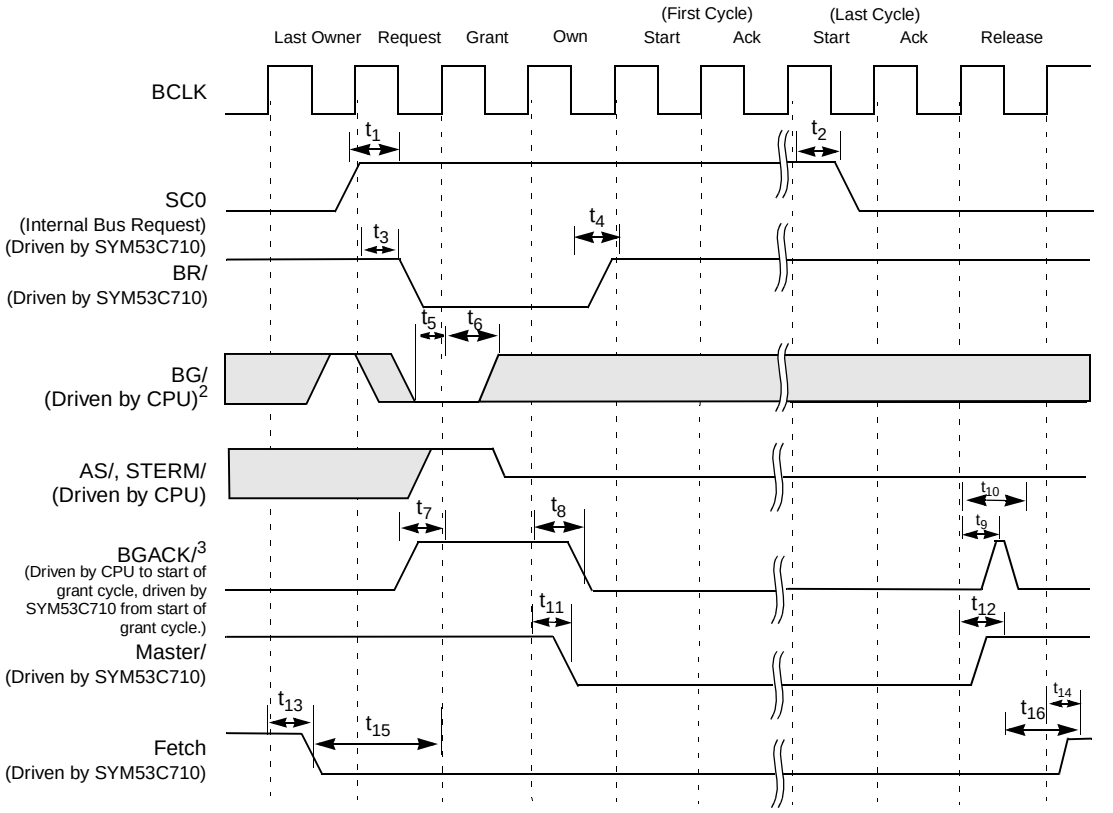
1. The SYM53C710 periodically asserts the BR/ signal and receives a SCSI interrupt at the same time. When this happens, the chip waits for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access. It deasserts the BR/, MASTER/, and all control lines after one BCLK and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip generates an interrupt, which the system may then service.
2. When the Snoop Mode bit (CTEST8, bit 0) is set to 1.
3. During a retry operation, FETCH/ remains LOW until a successful completion of the opcode fetch or a fatal bus error.

Table 6.23 SYM53C710-1 Bus Mode 1 Host Bus Arbitration Timings[1]

Symbol	Parameter	Min	Max	Unit
t_1	SC0 HIGH to BR/ LOW[2]	1	2	BCLK
t_2	BCLK HIGH to SC0 LOW on start phase of last cycle[2]	5	22	ns
t_3	BCLK HIGH to BR/ LOW	4	16	ns
t_4	BCLK HIGH to BR/ HIGH	5	21	ns
t_5	BG/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_6	BG/ hold from BCLK HIGH (any rising edge after BR/)	5	–	ns
t_7	BGACK/ setup to BCLK HIGH (any rising edge after BR/)	5	–	ns
t_8	BCLK HIGH to BGACK/ LOW	4	20	ns
t_9	BCLK HIGH to BGACK/ HIGH	3	12	ns
t_{10}	BCLK HIGH to BGACK/ HIGH-Z	7	28	ns
t_{11}	BCLK HIGH to MASTER/ LOW	5	18	ns
t_{12}	BCLK HIGH to MASTER/ HIGH	6	21	ns
t_{13}	BCLK HIGH to FETCH/ LOW	5	28	ns
t_{14}	BCLK HIGH to FETCH/ HIGH	5	28	ns
t_{15}	FETCH/ LOW to BR/ LOW	1	2	BCLK
t_{16}	BGACK/ HIGH to FETCH/ HIGH[3]	1	2	BCLK

1. The SYM53C710 periodically asserts the BR/ signal and receives a SCSI interrupt at the same time. When this happens, the chip waits for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access. It deasserts the BR/, MASTER/, and all control lines after one BCLK and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip generates an interrupt, which the system may then service.
2. When the Snoop Mode bit (CTEST8, bit 0) is set to 1.
3. During a retry operation, FETCH/ remains LOW until a successful completion of the opcode fetch or a fatal bus error.

Figure 6.11 Bus Mode 1 Host Bus Arbitration Cycle[1]



1. Shaded area indicates that the signal is a don't care. The SYM53C710 inserts a fairness delay of 5–8 clocks between host bus arbitrations.
2. In order for Bus Grant to be recognized, AS/ and STERM/ must be false.
3. If the Fast Arbitration bit is set (DCNTL, bit 1) the SYM53C710 drives the Bus Grant Acknowledge signal as soon as it receives a Bus Grant. One clock cycle of arbitration is saved.

6.6 Bus Mode 1 Fast Arbitration

6.6.1 Fast Arbitration Sequence

1. The SYM53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2. Bus Request is asserted.
3. The SYM53C710 waits for Bus Grant. Then the SYM53C710 becomes bus master asynchronously on the leading edge of BG/. The SYM53C710 asynchronously asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.
4. The SYM53C710 issues a start cycle on the next rising edge of BCLK.

Note: In fast arbitration mode, the SYM53C710 takes bus ownership on the assertion of BG/ regardless of the state of BR/ or BGACK/.

Table 6.24 SYM53C710 Bus Mode 1 Fast Arbitration Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to BR/ asserted	–	20	ns
t_2	BG/ setup to BCLK HIGH	16	–	ns
t_3	BG/ asserted to BR/ deasserted	–	22	ns
t_4	BG/ asserted to BGACK/ asserted	–	20	ns
t_5	BG/ asserted to MASTER/ asserted	–	16	ns
t_6	BG/ hold after BR/ deasserted[1]	0	–	ns
t_7	BR/ asserted to BG/ asserted	0	–	ns
t_8	BG/ to BCLK HIGH in ACK phase of last cycle	–	29	ns

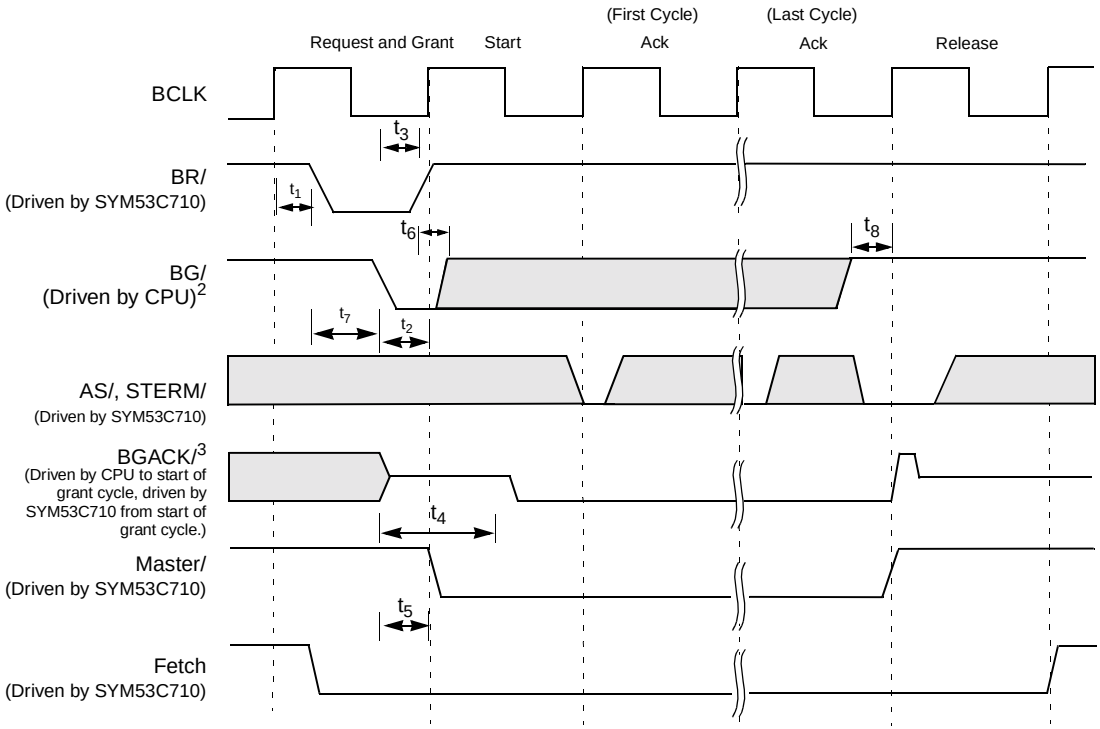
1. BG/ may not be asserted prior to BR/.

Table 6.25 SYM53C710-1 Bus Mode 1 Fast Arbitration Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to BR/ asserted	–	16	ns
t_2	BG/ setup to BCLK HIGH	16	–	ns
t_3	BG/ asserted to BR/ deasserted	–	18	ns
t_4	BG/ asserted to BGACK/ asserted	–	16	ns
t_5	BG/ asserted to MASTER/ asserted	–	14	ns
t_6	BG/ hold after BR/ deasserted[1]	0	–	ns
t_7	BR/ asserted to BG/ asserted	0	–	ns
t_8	BG/ to BCLK HIGH in ACK phase of last cycle	–	29	ns

1. BG/ may not be asserted prior to BR/.

Figure 6.12 Bus Mode 1 Fast Arbitration[1]



1. Shaded area indicates that the signal is a don't care. The SYM53C710 inserts a fairness delay of 5–8 clocks between host bus arbitrations.
2. In order for Bus Grant to be recognized, AS/ and STERM/ must be false.
3. If the Fast Arbitration bit is set (DCNTL, bit 1) the SYM53C710 drives the Bus Grant Acknowledge signal as soon as it receives a Bus Grant. One clock cycle of arbitration is saved.

6.7 Bus Mode 1 Bus Master Cycle

6.7.1 Bus Mode 1 Bus Master Read Sequence

1. The SYM53C710 has attained bus mastership.
2. The SYM53C710 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.
3. The SYM53C710 asserts the Address and Size lines.
4. The SYM53C710 asserts Address Strobe, Cache Burst Request (if appropriate), and Data Strobe.
5. The SYM53C710 waits for Synchronous Termination, Valid Data, Cache Burst Acknowledge, Bus Error, and HALT.
   - If Cache Burst Acknowledge is asserted, attempt bursting.
   - If Bus Error and HALT are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or HALT, and the SYM53C710 requires more cycles, then return to Step 3.
6. Upon acknowledgment of the last bus cycle, the SYM53C710 deasserts Master and Bus Grant Acknowledge.
7. The SYM53C710 floats the Control and Address lines.

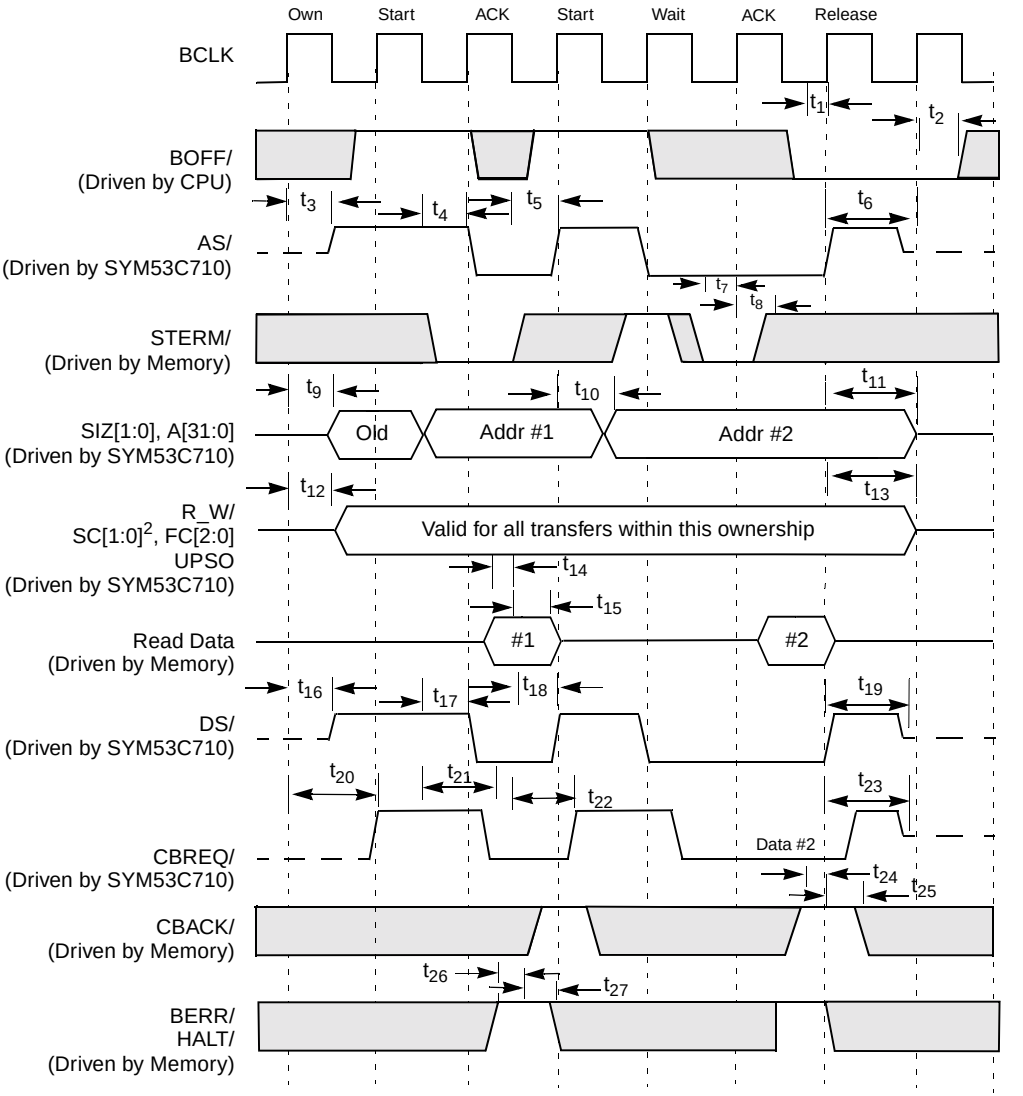
Table 6.26 SYM53C710 Bus Mode 1 Bus Master Read Timings (Noncache Line and Cache Line Burst)

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to AS/ driven	5	32	ns
t_4	BCLK LOW to AS/ LOW	3	15	ns
t_5	BCLK LOW to AS/ HIGH	3	15	ns
t_6	BCLK HIGH to AS/ HIGH-Z	7	34	ns
t_7	STERM/ (input) setup to BCLK HIGH	3	–	ns
t_8	STERM/ (Input) hold from BCLK HIGH	7	–	ns
t_9	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	28	ns
t_{10}	BCLK HIGH to A[31:0], SIZ[1:0] valid	4	18	ns
t_{11}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	34	ns
t_{12}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO driven and valid	5	28	ns
t_{13}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO HIGH-Z	6	30	ns
t_{14}	Read data setup to BCLK LOW	4	–	ns
t_{15}	Read data hold from BCLK LOW	6	–	ns
t_{16}	BCLK HIGH to DS/ driven	5	32	ns
t_{17}	BCLK LOW to DS/ LOW	3	16	ns
t_{18}	BCLK LOW to DS/ HIGH	3	16	ns
t_{19}	BCLK HIGH to DS/ HIGH-Z	7	34	ns
t_{20}	BCLK HIGH to CBREQ/ driven	5	30	ns
t_{21}	BCLK LOW to CBREQ/ LOW	3	16	ns
t_{22}	BCLK LOW to CBREQ/ HIGH	3	16	ns
t_{23}	BCLK HIGH to CBREQ/ HIGH-Z	7	32	ns
t_{24}	CBACK/ setup to BCLK LOW	8	–	ns
t_{25}	CBACK/ hold from BCLK LOW	4	–	ns
t_{26}	BERR/, HALT/ setup to BCLK LOW	6	–	ns
t_{27}	BERR/, HALT/ hold from BCLK LOW	4	–	ns

Table 6.27 SYM53C710-1 Bus Mode 1 Bus Master Read Timings (Noncache Line and Cache Line Burst)

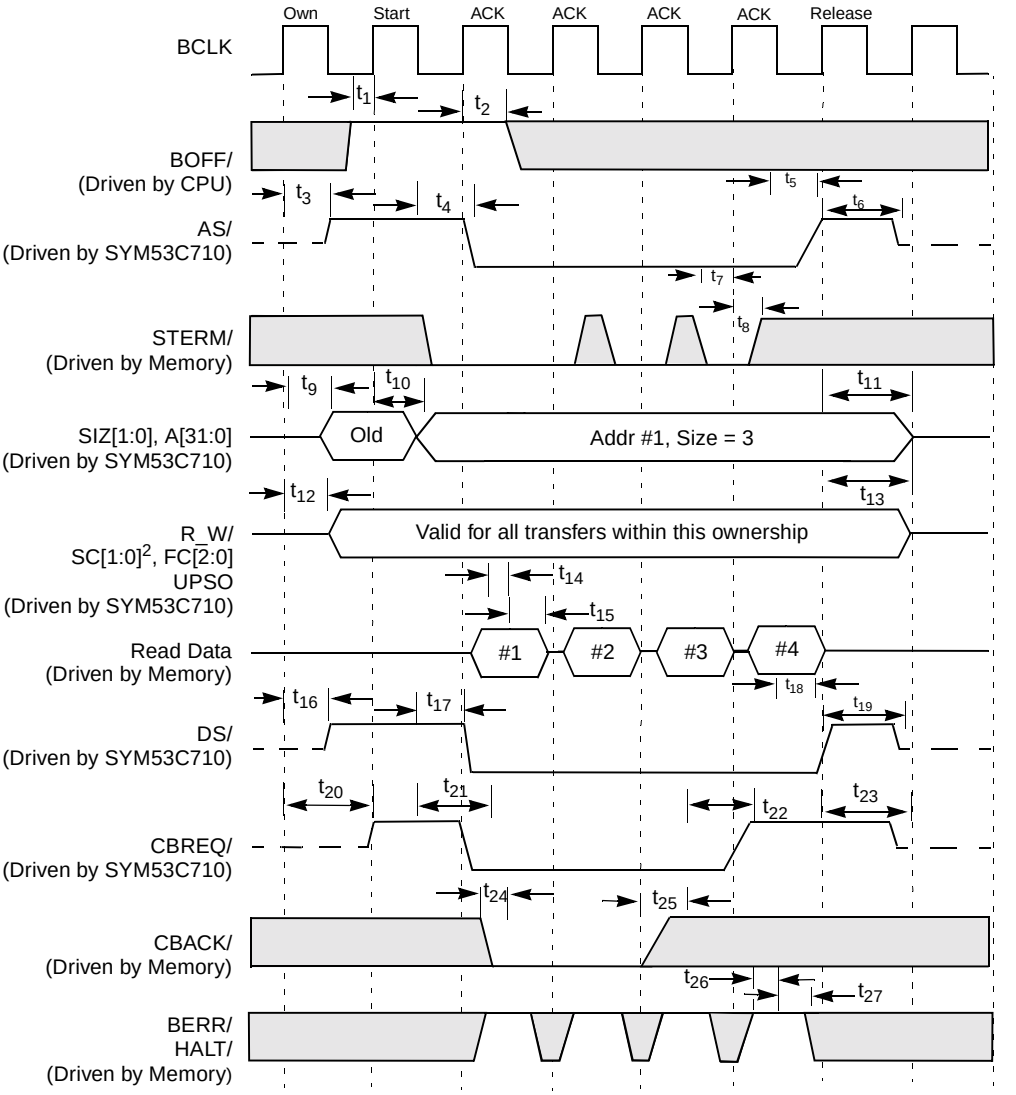
Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to AS/ driven	5	26	ns
t_4	BCLK LOW to AS/ LOW	3	14	ns
t_5	BCLK LOW to AS/ HIGH	3	14	ns
t_6	BCLK HIGH to AS/ HIGH-Z	7	28	ns
t_7	STERM/ (input) setup to BCLK HIGH	3	–	ns
t_8	STERM/ (input) hold from BCLK HIGH	7	–	ns
t_9	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	24	ns
t_{10}	BCLK HIGH to A[31:0], SIZ[1:0] valid	4	15	ns
t_{11}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	28	ns
t_{12}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO driven and valid	5	24	ns
t_{13}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO HIGH-Z	6	25	ns
t_{14}	Read data setup to BCLK LOW	4	–	ns
t_{15}	Read data hold from BCLK LOW	6	–	ns
t_{16}	BCLK HIGH to DS/ driven	5	25	ns
t_{17}	BCLK LOW to DS/ LOW	3	14	ns
t_{18}	BCLK LOW to DS/ HIGH	3	14	ns
t_{19}	BCLK HIGH to DS/ HIGH-Z	7	28	ns
t_{20}	BCLK HIGH to CBREQ/ driven	5	25	ns
t_{21}	BCLK LOW to CBREQ/ LOW	3	14	ns
t_{22}	BCLK LOW to CBREQ/ HIGH	3	14	ns
t_{23}	BCLK HIGH to CBREQ/ HIGH-Z	7	26	ns
t_{24}	CBACK/ setup to BCLK LOW	8	–	ns
t_{25}	CBACK/ hold from BCLK LOW	4	–	ns
t_{26}	BERR/, HALT/ setup to BCLK LOW	6	–	ns
t_{27}	BERR/, HALT/ hold from BCLK LOW	4	–	ns

Figure 6.13 Bus Mode 1 Bus Master Read Cycle (Noncache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Figure 6.14 Bus Mode 1 Bus Master Read Cycle (Cache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

6.7.2 Bus Mode 1 Bus Master Write Sequence

1. The SYM53C710 has attained bus mastership.
2. The SYM53C710 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.
3. The SYM53C710 asserts the Address, Size, and Data lines.
4. The SYM53C710 asserts Address Strobe and Cache Burst Request (and Data Strobe if Read).
5. The SYM53C710 asserts Data Strobe.
6. The SYM53C710 waits for Synchronous Termination, Cache Burst Acknowledge, Bus Error, and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the SYM53C710 requires more cycles, then return to Step 3.
7. Upon acknowledgment of the last bus cycle, the SYM53C710 deasserts Master and Bus Grant Acknowledge
8. The SYM53C710 floats the Control, Address, and Data lines.

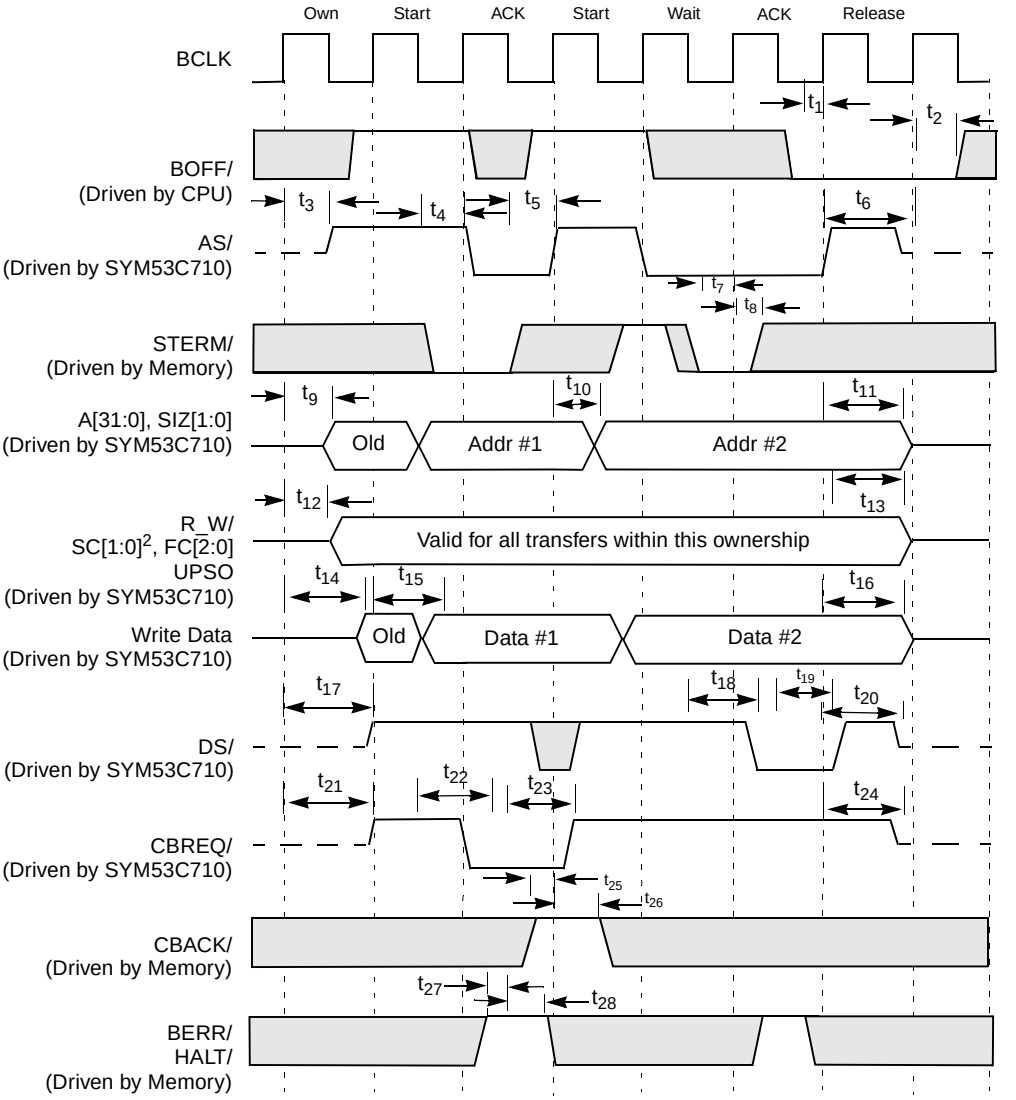
Table 6.28 SYM53C710 Bus Mode 1 Master Write Timings (Noncache Line and Cache Line Burst)

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to AS/ driven	5	32	ns
t_4	BCLK LOW to AS/ LOW	3	15	ns
t_5	BCLK LOW to AS/ HIGH	3	15	ns
t_6	BCLK HIGH to AS/ HIGH-Z	7	34	ns
t_7	STERM/ setup to BCLK HIGH	3	–	ns
t_8	STERM/ hold from BCLK HIGH	7	–	ns
t_9	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	28	ns
t_{10}	BCLK HIGH to A[31:0], SIZ[1:0] valid	4	18	ns
t_{11}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	34	ns
t_{12}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO driven and valid	5	28	ns
t_{13}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO HIGH-Z	6	30	ns
t_{14}	BCLK HIGH to write data driven	6	34	ns
t_{15}	BCLK HIGH to write data valid	6	24	ns
t_{16}	BCLK HIGH to write data HIGH-Z	6	32	ns
t_{17}	BCLK HIGH to DS/ driven	5	32	ns
t_{18}	BCLK LOW to DS/ LOW	3	16	ns
t_{19}	BCLK LOW to DS/ HIGH	3	16	ns
t_{20}	BCLK HIGH to DS/ HIGH-Z	7	34	ns
t_{21}	BCLK HIGH to CBREQ/ driven	5	30	ns
t_{22}	BCLK LOW to CBREQ/ LOW	3	16	ns
t_{23}	BCLK LOW to CBREQ/ HIGH	3	16	ns
t_{24}	BCLK HIGH to CBREQ/ HIGH-Z	7	32	ns
t_{25}	CBACK/ setup to BCLK LOW	8	–	ns
t_{26}	CBACK/ hold from BCLK LOW	4	–	ns
t_{27}	BERR/, HALT/ setup to BCLK LOW	6	–	ns
t_{28}	BERR/, HALT/ hold from BCLK LOW	4	–	ns

Table 6.29 SYM53C710-1 Bus Mode 1 Bus Master Write Timings (Noncache Line and Cache Line Burst)

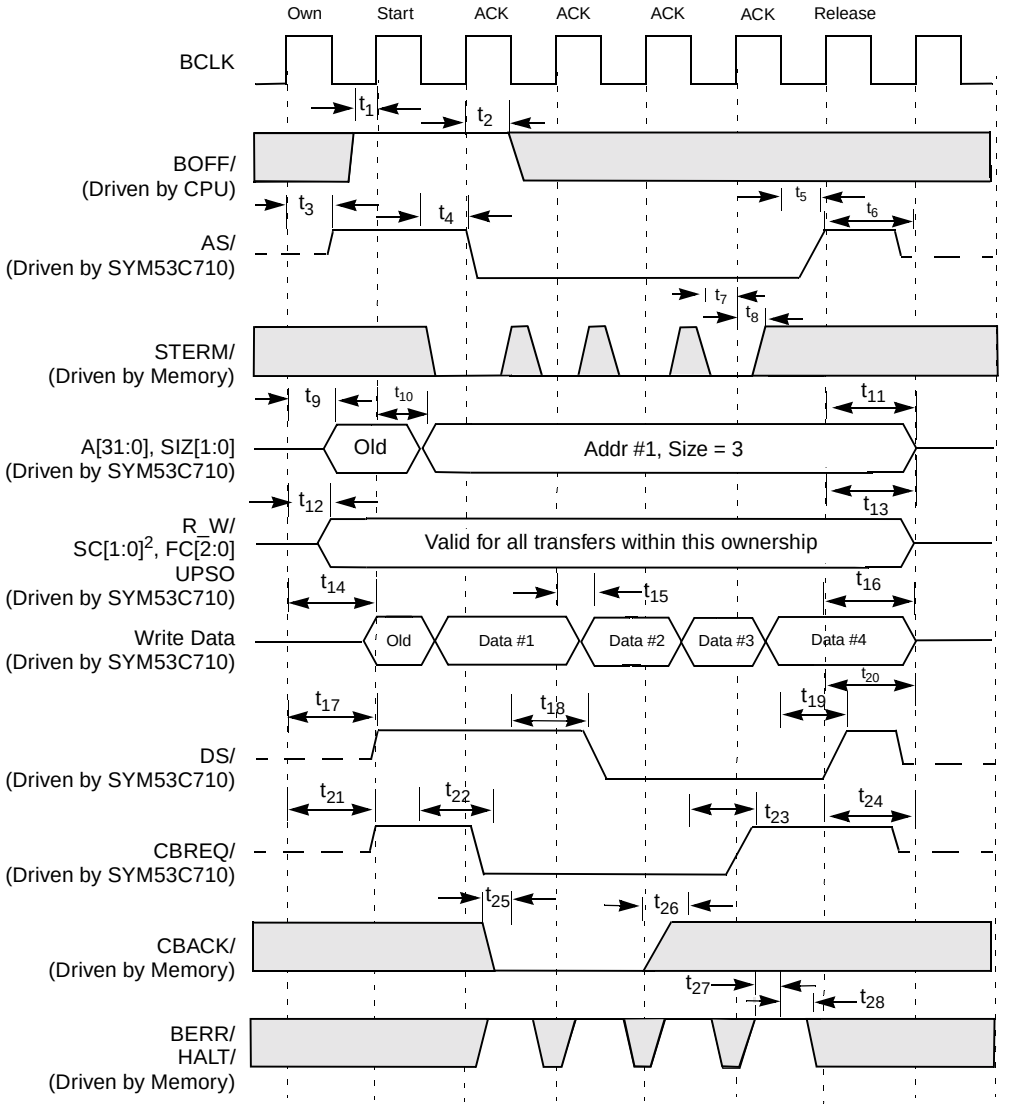
Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to AS/ driven	5	26	ns
t_4	BCLK LOW to AS/ LOW	3	14	ns
t_5	BCLK LOW to AS/ HIGH	3	14	ns
t_6	BCLK HIGH to AS/ HIGH-Z	7	28	ns
t_7	STERM/ setup to BCLK HIGH	3	–	ns
t_8	STERM/ hold from BCLK HIGH	7	–	ns
t_9	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	24	ns
t_{10}	BCLK HIGH to A[31:0], SIZ[1:0] valid	4	15	ns
t_{11}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	28	ns
t_{12}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO driven and valid	5	24	ns
t_{13}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], UPSO HIGH-Z	6	25	ns
t_{14}	BCLK HIGH to write data driven	6	28	ns
t_{15}	BCLK HIGH to write data valid	6	20	ns
t_{16}	BCLK HIGH to data HIGH-Z	6	26	ns
t_{17}	BCLK HIGH to DS/ driven	5	25	ns
t_{18}	BCLK LOW to DS/ LOW	3	14	ns
t_{19}	BCLK LOW to DS/ HIGH	3	14	ns
t_{20}	BCLK HIGH to DS/ HIGH-Z	7	28	ns
t_{21}	BCLK HIGH to CBREQ/ driven	5	25	ns
t_{22}	BCLK LOW to CBREQ/ LOW	3	14	ns
t_{23}	BCLK LOW to CBREQ/ HIGH	3	14	ns
t_{24}	BCLK HIGH to CBREQ/ HIGH-Z	7	26	ns
t_{25}	CBACK/ setup to BCLK LOW	8	–	ns
t_{26}	CBACK/ hold from BCLK LOW	4	–	ns
t_{27}	BERR/, HALT/ setup to BCLK LOW	6	–	ns
t_{28}	BERR/, HALT/ hold from BCLK LOW	4	–	ns

Figure 6.15 Bus Mode 1 Bus Master Write Cycle (Noncache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Figure 6.16 Bus Mode 1 Bus Master Write Cycle (Cache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

6.8 Bus Mode 2 Slave Cycle

6.8.1 Bus Mode 2 Slave Read Sequence

1. The Read/Write, Address, Transfer Start, and the Size lines are asserted by the CPU.
2. Chip Select is validated by the SYM53C710 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. Three clock cycles of wait state are inserted and the Data lines are asserted.
6. Slave Acknowledge is asserted by the SYM53C710, if no errors are detected.
7. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8. Slave Acknowledge or Transfer Error Acknowledge is deasserted.
9. The SYM53C710 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.
10. The Data lines are 3-stated by the SYM53C710.

Table 6.30 SYM53C710 Bus Mode 2 Slave Read Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	TS/ setup to BCLK HIGH	4	–	ns
t_2	TS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to any BCLK HIGH after TS/	5	–	ns
t_4	CS/ hold from any BCLK HIGH after TS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	30	ns
t_6	BCLK HIGH to TBI/ HIGH	4	22	ns
t_7	BCLK HIGH to SLACK/, TEA/ LOW	5	20	ns
t_8	BCLK HIGH to SLACK/, TEA/ HIGH	4	20	ns
t_9	TA/ setup to BCLK HIGH during or after SLACK/, TEA/	9	–	ns
t_{10}	TA/ hold from BCLK HIGH during or after SLACK/, TEA/	5	–	ns
t_{11}	BCLK HIGH to data bus driven	8	28	ns
t_{12}	BCLK HIGH to read data valid	–	75	ns
t_{13}	BCLK HIGH to data bus HIGH-Z	7	30	ns
t_{14}	A[5:0], SIZ[1:0], R_W/ setup to BCLK HIGH	4	–	ns
t_{15}	A[5:0], SIZ[1:0], R_W/ hold from BCLK HIGH	12	–	ns

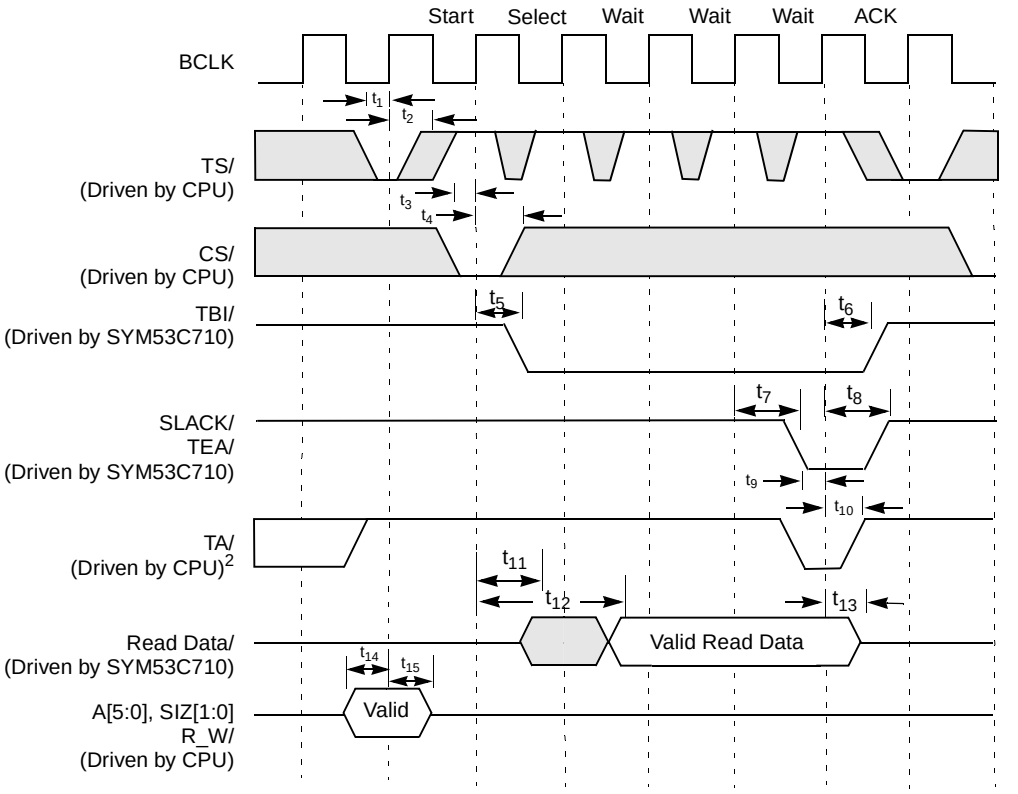
1. The SYM53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the SYM53C710.

Table 6.31 SYM53C710-1 Bus Mode 2 Slave Read Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	TS/ setup to BCLK HIGH	4	–	ns
t_2	TS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to BCLK HIGH after TS/	5	–	ns
t_4	CS/ hold from BCLK HIGH after TS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	25	ns
t_6	BCLK HIGH to TBI/ HIGH	4	18	ns
t_7	BCLK HIGH to SLACK/, TEA/ LOW	5	17	ns
t_8	BCLK HIGH to SLACK/, TEA/ HIGH	4	17	ns
t_9	TA/ setup to BCLK HIGH during or after SLACK/, TEA/	9	–	ns
t_{10}	TA/ hold from BCLK HIGH during or after SLACK/, TEA/	5	–	ns
t_{11}	BCLK HIGH to data bus driven	8	28	ns
t_{12}	BCLK HIGH to read data valid	–	60	ns
t_{13}	BCLK HIGH to data bus HIGH-Z	7	25	ns
t_{14}	A[5:0], SIZ[1:0], R_W/ setup to BCLK HIGH	4	–	ns
t_{15}	A[5:0], SIZ[1:0], R_W/ hold from BCLK HIGH	12	–	ns

1. The SYM53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the SYM53C710.

Figure 6.17 Bus Mode 2 Slave Read Cycle[1]



1. Shaded area indicates that the signal is a don't care.
2. This signal may be driven by the SYM53C710 if the ENABLE ACK (EA) bit is set (DCNTL, bit 5). See explanation in Chapter 2 for the use of this signal as an output.

6.8.2 Bus Mode 2 Slave Write Sequence

1. The Read/Write, Address, Transfer Start, and Size Lines are asserted by the CPU.
2. Chip Select is validated by the SYM53C710 on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. The Data lines are asserted by the CPU.
6. Three clock cycles of wait state are inserted.
7. Slave Acknowledge is asserted by the SYM53C710, if no errors are detected.
8. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9. The SYM53C710 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.
10. Slave Acknowledge or Transfer Error Acknowledge is deasserted.

Table 6.32 SYM53C710 Bus Mode 2 Slave Write Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	TS/ setup to BCLK HIGH	4	–	ns
t_2	TS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to BCLK HIGH after TS/	5	–	ns
t_4	CS/ hold from BCLK HIGH after TS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	30	ns
t_6	BCLK HIGH to TBI/ HIGH	4	22	ns
t_7	BCLK HIGH to SLACK/, TEA/ LOW	5	20	ns
t_8	BCLK HIGH to SLACK/, TEA/ HIGH	4	20	ns
t_9	TA/ setup to BCLK HIGH during or after SLACK/, TEA/	9	–	ns
t_{10}	TA/ hold from BCLK HIGH during or after SLACK/, TEA/	5	–	ns
t_{11}	Valid write data Setup to BCLK HIGH	5	–	ns
t_{12}	Valid write data hold from BCLK HIGH	14	–	ns
t_{13}	A[5:0], SIZ[1:0], R_W/ setup to BCLK HIGH	4	–	ns
t_{14}	A[5:0], SIZ(1:0], R_W/ hold from BCLK HIGH	12	–	ns

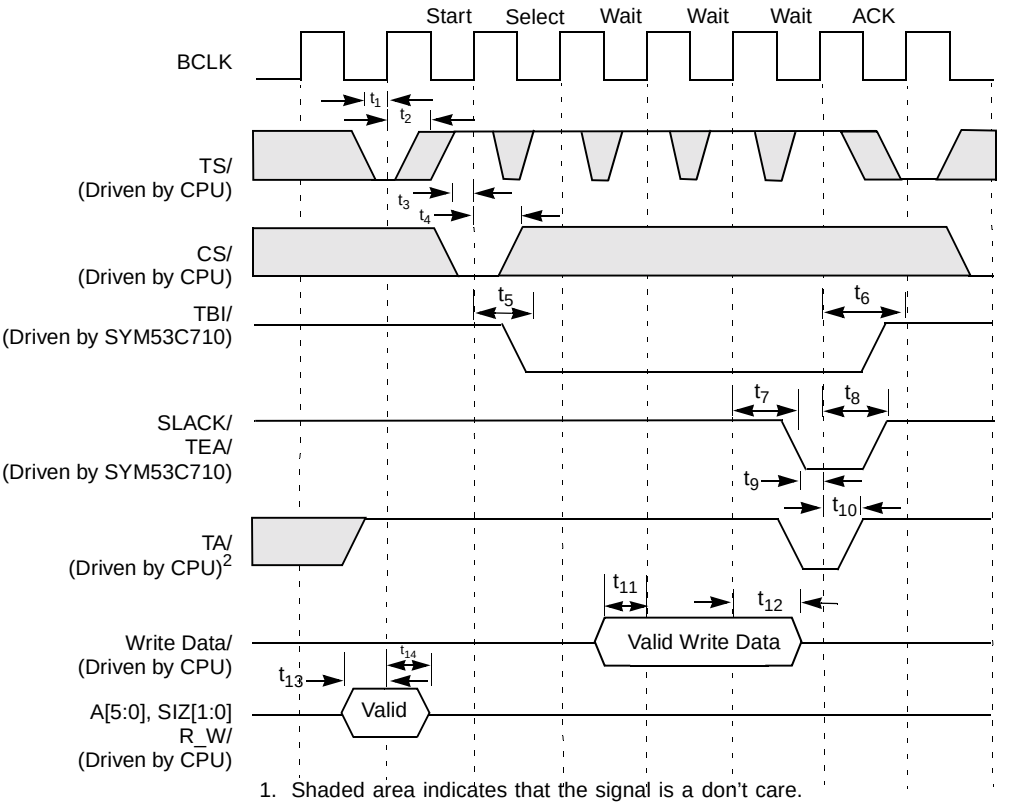
1. The SYM53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the SYM53C710.

Table 6.33 SYM53C710-1 Bus Mode 2 Slave Write Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	TS/ setup to BCLK HIGH	4	–	ns
t_2	TS/ hold from BCLK HIGH	4	–	ns
t_3	CS/ setup to BCLK HIGH after TS/	5	–	ns
t_4	CS/ hold from BCLK HIGH after TS/	5	–	ns
t_5	BCLK HIGH to TBI/ LOW	5	25	ns
t_6	BCLK HIGH to TBI/ HIGH	4	18	ns
t_7	BCLK HIGH to SLACK/, TEA/ LOW	5	17	ns
t_8	BCLK HIGH to SLACK/, TEA/ HIGH	4	17	ns
t_9	TA/ setup to BCLK HIGH during or after SLACK/, TEA/	9	–	ns
t_{10}	TA/ hold from BCLK HIGH during or after SLACK/, TEA/	5	–	ns
t_{11}	Valid write data setup to BCLK HIGH	5	–	ns
t_{12}	Valid write data hold from BCLK HIGH	14	–	ns
t_{13}	A[5:0], SIZ[1:0], R_W/ setup to BCLK HIGH	4	–	ns
t_{14}	A[5:0], SIZ(1:0], R_W/ hold from BCLK HIGH	12	–	ns

1. The SYM53C710 must see transfer starts paired up with transfer acknowledges, even though the slave cycle may not be intended for the SYM53C710.

Figure 6.18 Bus Mode 2 Slave Write Cycle[1]



1. Shaded area indicates that the signal is a don't care.
2. This signal may be driven by the SYM53C710 if the ENABLE ACK (EA) bit is set (DCNTL, bit 5). See explanation in Chapter 2 for the use of this signal as an output.

6.9 Host Bus Arbitration

6.9.1 Bus Arbitration Sequence

1. The SYM53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2. Bus Request is asserted.
3. The SYM53C710 waits for Bus Grant and checks that Bus Busy is deasserted. Then the SYM53C710 asserts Bus Busy and Master, and deasserts Bus Request.

Table 6.34 SYM53C710 Bus Mode 2 Host Bus Arbitration Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	SC0 HIGH to BR/ LOW[2]	1	2	BCLK
t_2	BCLK HIGH to SC0 LOW on start phase of last cycle[2]	5	28	ns
t_3	BCLK HIGH to BR/ LOW	4	20	ns
t_4	BCLK HIGH to BR/ HIGH	5	25	ns
t_5	BG/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_6	BG/ hold from BCLK HIGH (any rising edge after BR/)	5	–	ns
t_7	BB/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_8	BCLK HIGH to BB/ LOW	4	24	ns
t_9	BCLK HIGH to BB/ HIGH	3	19	ns
t_{10}	BCLK HIGH to BB/ HIGH-Z	7	32	ns
t_{11}	BCLK HIGH to MASTER/ LOW	5	22	ns
t_{12}	BCLK HIGH to MASTER/ HIGH	6	26	–
t_{13}	BCLK HIGH to FETCH/ LOW	5	36	ns
t_{14}	BCLK HIGH to FETCH/ HIGH	5	36	ns
t_{15}	FETCH/ LOW to BR/ LOW	1	2	BCLK
t_{16}	BB/ HIGH to FETCH/ HIGH[3]	1	2	BCLK

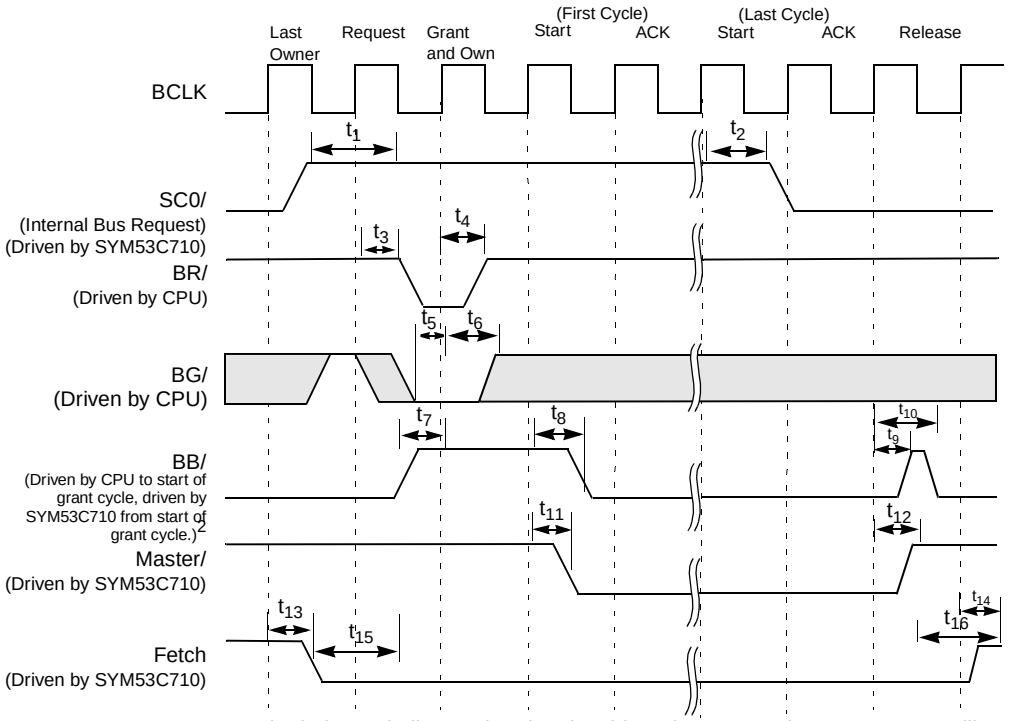
1. The SYM53C710 periodically asserts the BR/ signal and receives a SCSI interrupt at the same time. When this happens, the chip waits for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access. It deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip next generates an interrupt, which the system may then service.
2. When the Snoop Mode bit (CTEST8, bit 0) is set to 1.
3. During a retry operation, FETCH/ remains low until successful completion of an opcode fetch or a fatal bus error.

Table 6.35 SYM53C710-1 Bus Mode 2 Host Bus Arbitration Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	SC0 HIGH to BR/ LOW[2]	1	2	BCLK
t_2	BCLK HIGH to SC0 LOW on start phase of last cycle[2]	5	22	ns
t_3	BCLK HIGH to BR/ LOW	4	16	ns
t_4	BCLK HIGH to BR/ HIGH	5	21	ns
t_5	BG/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_6	BG/ hold from BCLK HIGH (any rising edge after BR/)	5	–	ns
t_7	BB/ setup to BCLK HIGH (any rising edge after BR/)	4	–	ns
t_8	BCLK HIGH to BB/ LOW	4	20	ns
t_9	BCLK HIGH to BB/ HIGH	3	12	ns
t_{10}	BCLK HIGH to BB/ HIGH-Z	7	28	ns
t_{11}	BCLK HIGH to MASTER/ LOW	5	18	ns
t_{12}	BCLK HIGH to MASTER/ HIGH	6	21	–
t_{13}	BCLK HIGH to FETCH/ LOW	5	28	ns
t_{14}	BCLK HIGH to FETCH/ HIGH	5	28	ns
t_{15}	FETCH/ LOW to BR/ LOW	1	2	BCLK
t_{16}	BB/ HIGH to FETCH/ HIGH[3]	1	2	BCLK

1. The SYM53C710 will periodically assert the BR/ signal and receives a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access. It deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will next generate an interrupt, which the system may then service.
2. When the Snoop Mode bit (CTEST8, bit 0) is set to 1.
3. During a retry operation, FETCH/ will remain low until successful completion of an opcode fetch or a fatal bus error.

Figure 6.19 Bus Mode 2 Host Bus Arbitration[1]



1. Shaded area indicates that the signal is a don't care. The SYM53C710 will insert a fairness delay of 5–8 clocks between host bus arbitrations.
2. If the Fast Arbitration bit is set (DCNTL, bit 1), the SYM53C710 will drive the Bus Grant Acknowledge signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.

6.10 Bus Mode 2 Fast Arbitration

6.10.1 Fast Arbitration Sequence

1. The SYM53C710 determines bus mastership is required. If appropriate, FETCH/ is asserted.
2. Bus request is asserted.
3. The SYM53C710 waits for Bus Grant. The SYM53C710 becomes bus master asynchronously on the leading edge of BG/. Then the SYM53C710 asynchronously asserts Bus Busy and Master, and deasserts Bus Request.
4. The SYM53C710 issues a start cycle on the next rising edge of BCLK.

Note: In fast arbitration mode, the SYM53C710 will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BB/.

Table 6.36 SYM53C710 Bus Mode 2 Fast Arbitration Timings

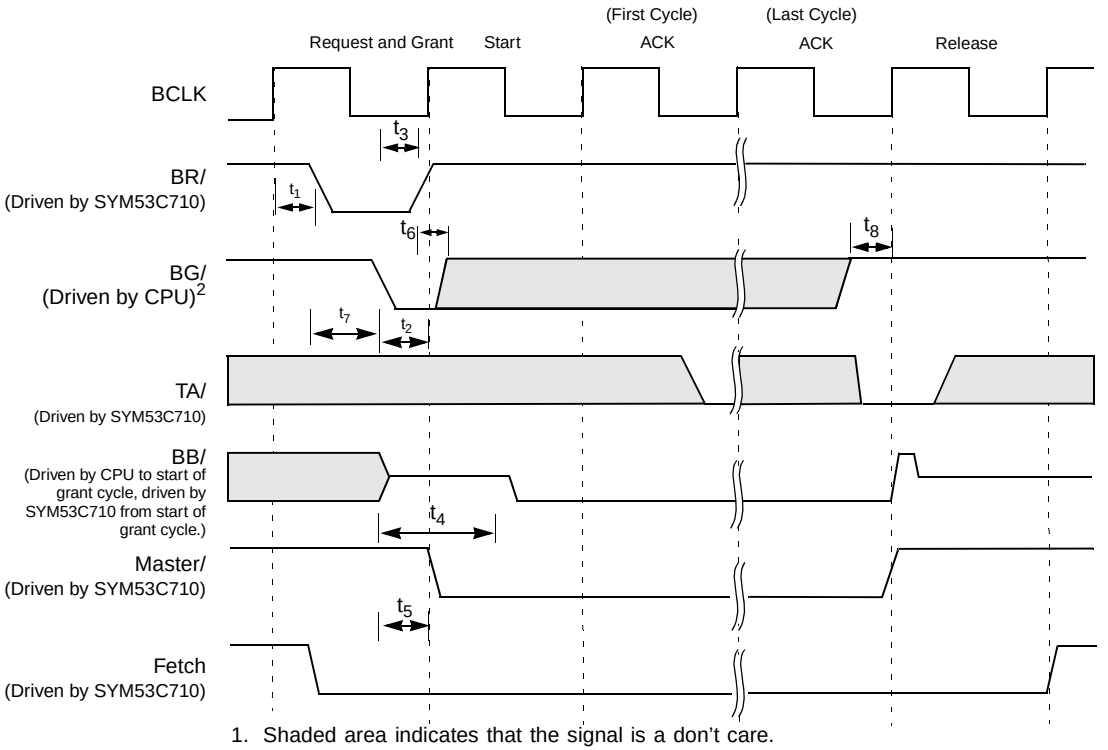
Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to BR/ asserted	–	20	ns
t_2	BG/ setup to BCLK HIGH	16	–	ns
t_3	BG/ asserted to BR/ deasserted	–	22	ns
t_4	BG/ asserted to BB/ asserted	–	20	ns
t_5	BG/ asserted to MASTER/ asserted	–	16	ns
t_6	BG/ hold after BR/ deasserted	0	–	ns
t_7	BR/ asserted to BG/ asserted	0	–	ns
t_8	BG/ to BCLK HIGH, in ACK phase of last cycle	–	29	ns

Table 6.37 SYM53C710-1 Bus Mode 2 Fast Arbitration Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to BR/ asserted	–	16	ns
t_2	BG/ setup to BCLK HIGH	16	–	ns
t_3	BG/ asserted to BR/ deasserted	–	18	ns
t_4	BG/ asserted to BB/ asserted	–	16	ns
t_5	BG/ asserted to MASTER/ asserted	–	14	ns
t_6	BG/ hold after BR/ deasserted[1]	0	–	ns
t_7	BR/ asserted to BG/ asserted	0	–	ns
t_9	BG/ to BCLK HIGH, in ACK phase of last cycle	–	29	ns

1. BG/ may not be asserted prior to BR/.

Figure 6.20 Bus Mode 2 Fast Arbitration[1]



1. Shaded area indicates that the signal is a don't care.

6.11 Bus Mode 2 Bus Master Cycle

6.11.1 Bus Mode 2 Bus Master Read Sequence

1. The SYM53C710 has attained bus mastership.
2. The SYM53C710 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.

3a. The SYM53C710 asserts Transfer in Progress and Transfer Start.

3b. The SYM53C710 asserts Transfer Start, Address, and Size lines.

4. The SYM53C710 deasserts Transfer Start.
5. The SYM53C710 waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated on the next rising edge of BCLK.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the SYM53C710 requires more cycles, then return to Step 3b.
6. The SYM53C710 deasserts the Control and Address lines.
7. Upon acknowledgment of the last bus cycle, the SYM53C710 deasserts Master and Bus Grant Acknowledge.

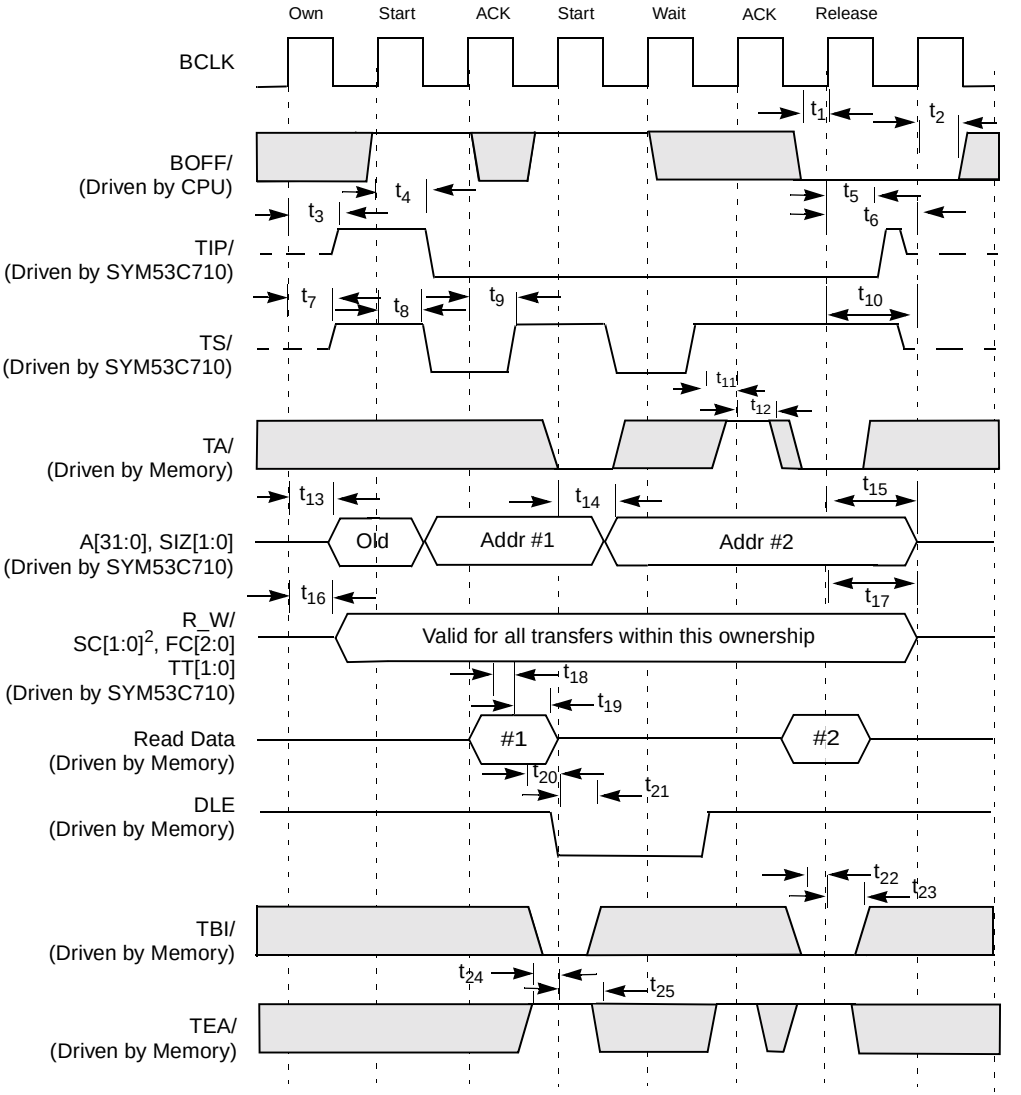
Table 6.38 SYM53C710 Bus Mode 2 Bus Master Cycle Read Timings (Noncache Line and Cache Line Burst)

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	17	ns
t_5	BCLK HIGH to TIP/ HIGH	3	16	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK HIGH to TS/ driven	5	30	ns
t_8	BCLK HIGH to TS/ LOW	3	14	ns
t_9	BCLK HIGH to TS/ HIGH	4	13	ns
t_{10}	BCLK HIGH to TS/ HIGH-Z	7	32	ns
t_{11}	TA/ setup to BCLK HIGH	9	–	ns
t_{12}	TA/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	28	ns
t_{14}	BCLK HIGH to A[31:0], SIZ[1:0] valid	5	18	ns
t_{15}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	32	ns
t_{16}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] driven and valid	5	30	ns
t_{17}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] HIGH-Z	–	32	ns
t_{18}	Read data setup to BCLK HIGH	5	–	ns
t_{19}	Read data hold from BCLK HIGH	6	–	ns
t_{20}	Read Data setup to DLE LOW	4	–	ns
t_{21}	Read data hold from DLE LOW	6	–	ns
t_{22}	TBI/ setup to BCLK HIGH	6	–	ns
t_{23}	TBI/ hold from BCLK HIGH	4	–	ns
t_{24}	TEA/ setup to BCLK HIGH	9	–	ns
t_{25}	TEA/ hold from BCLK HIGH	5	–	ns

Table 6.39 SYM53C710-1 Bus Mode 2 Bus Master Read Cycle Timings (Noncache Line and Cache Line Burst)

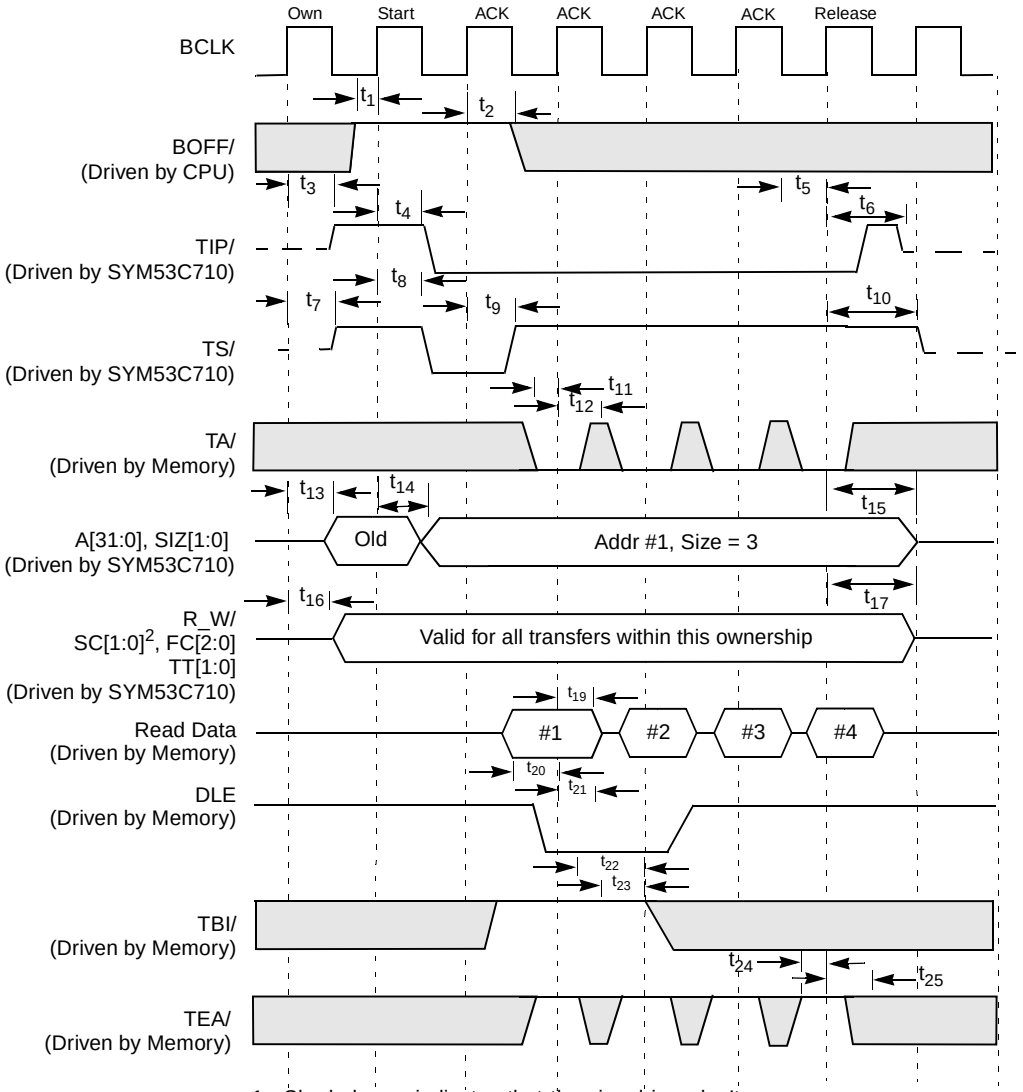
Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	26	ns
t_4	BCLK HIGH to TIP/ LOW	3	14	ns
t_5	BCLK HIGH to TIP/ HIGH	3	14	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	28	ns
t_7	BCLK HIGH to TS/ driven	5	25	ns
t_8	BCLK HIGH to TS/ LOW	3	12	ns
t_9	BCLK HIGH to TS/ HIGH	4	12	ns
t_{10}	BCLK HIGH to TS/ HIGH-Z	7	28	ns
t_{11}	TA/ setup to BCLK HIGH	9	–	ns
t_{12}	TA/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	24	ns
t_{14}	BCLK HIGH to A[31:0], SIZ[1:0] valid	5	15	ns
t_{15}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	28	ns
t_{16}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] driven and valid	5	25	ns
t_{17}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] HIGH-Z	–	28	ns
t_{18}	Read data setup to BCLK HIGH	5	–	ns
t_{19}	Read data hold from BCLK HIGH	6	–	ns
t_{20}	Read data setup to DLE LOW	4	–	ns
t_{21}	Read data hold from DLE LOW	6	–	ns
t_{22}	TBI/ setup to BCLK HIGH	6	–	ns
t_{23}	TBI/ hold from BCLK HIGH	4	–	ns
t_{24}	TEA/ setup to BCLK HIGH	9	–	ns
t_{25}	TEA/ hold from BCLK HIGH	5	–	ns

Figure 6.21 Bus Mode 2 Bus Master Read Cycle (Noncache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Figure 6.22 Bus Mode 2 Bus Master Read Cycle (Cache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

6.11.2 Bus Mode 2 Bus Master Write Sequence

1. The SYM53C710 has attained bus mastership.
2. The SYM53C710 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.

3a. The SYM53C710 asserts Transfer in Progress and Transfer Start.

3b. The SYM53C710 asserts Transfer Start, Address, Size lines, and Data lines.

4. The SYM53C710 deasserts Transfer Start.
5. The SYM53710 waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the SYM53C710 requires more cycles, return to Step 3b.
6. Upon acknowledgment of the last bus cycle, the SYM53C710 deasserts Master and Bus Grant Acknowledge.
7. The SYM53C710 floats the Control, Address, and Data lines.

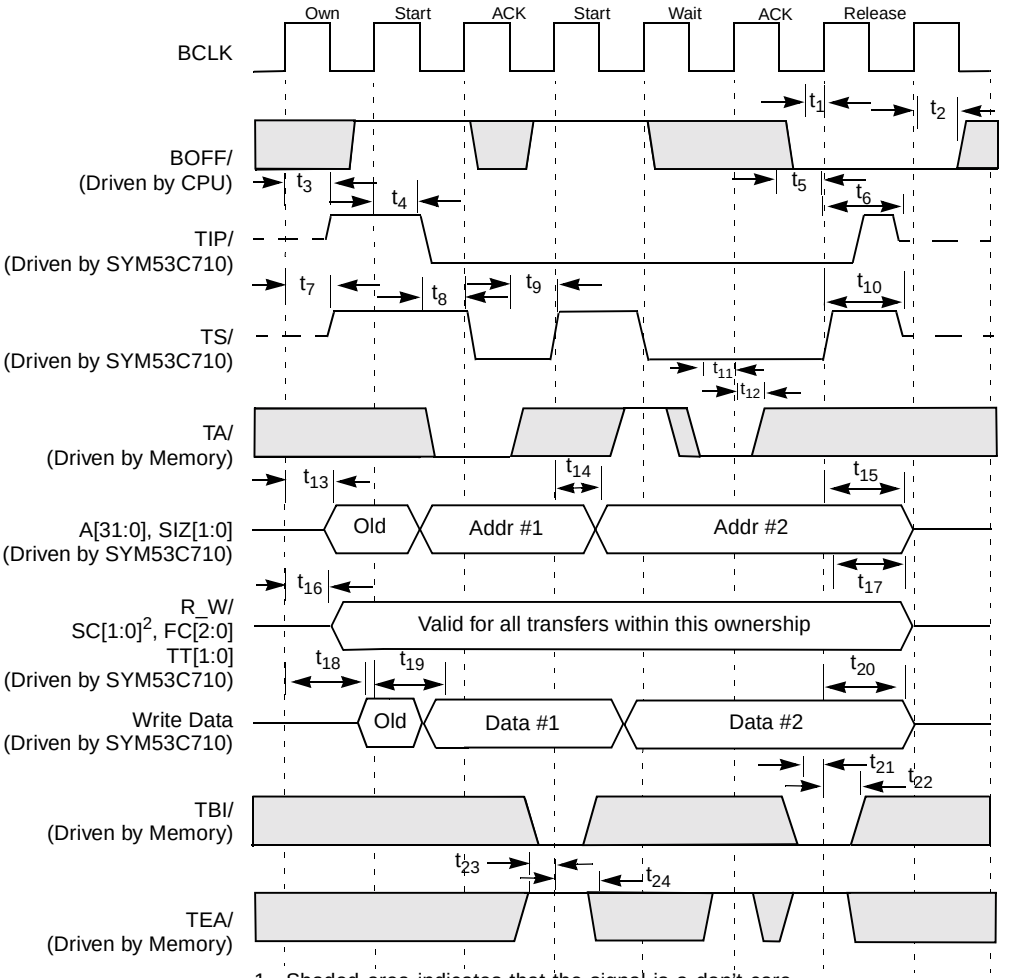
Table 6.40 SYM53C710 Bus Mode 2 Bus Master Write Timings (Noncache Line and Cache Line Burst)

Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	32	ns
t_4	BCLK HIGH to TIP/ LOW	3	17	ns
t_5	BCLK HIGH to TIP/ HIGH	3	16	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	32	ns
t_7	BCLK HIGH to TS/ driven	5	30	ns
t_8	BCLK HIGH to TS/ LOW	3	14	ns
t_9	BCLK HIGH to TS/ HIGH	3	13	ns
t_{10}	BCLK HIGH to TS/ HIGH-Z	7	32	ns
t_{11}	TA/ setup to BCLK HIGH	9	–	ns
t_{12}	TA/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	28	ns
t_{14}	BCLK HIGH to A[31:0], SIZ[1:0] valid	3	18	ns
t_{15}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	32	ns
t_{16}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] driven and valid	5	30	ns
t_{17}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] HIGH-Z	5	32	ns
t_{18}	BCLK HIGH to write data driven	5	34	ns
t_{19}	BCLK HIGH to write data valid	7	24	ns
t_{20}	BCLK HIGH to write data HIGH-Z	5	30	ns
t_{21}	TBI/ setup to BCLK HIGH	6	–	ns
t_{22}	TBI/ hold from BCLK HIGH	4	–	ns
t_{23}	TEA/ setup to BCLK HIGH	9	–	ns
t_{24}	TEA/ hold from BCLK HIGH	5	–	ns

Table 6.41 SYM53C710-1 Bus Mode 2 Bus Master Write Timings (Noncache Line and Cache Line Burst)

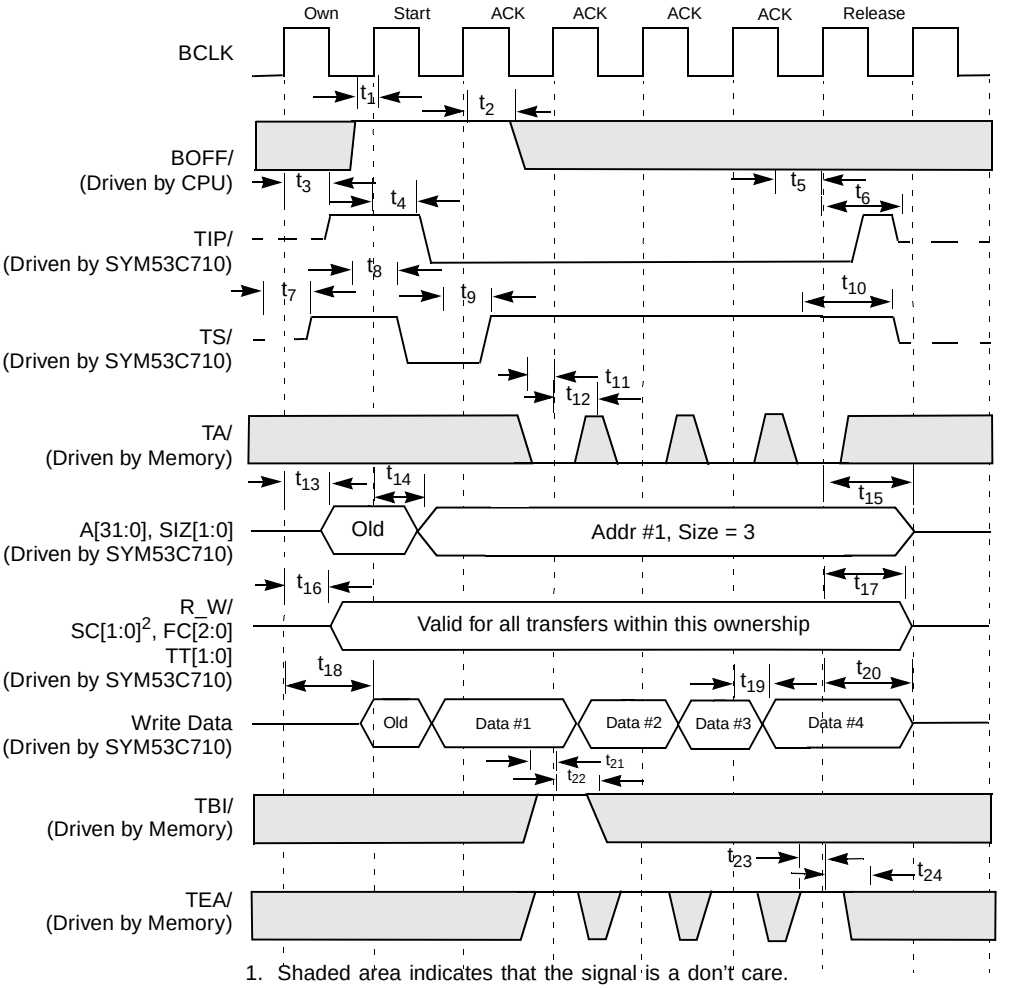
Symbol	Parameter	Min	Max	Units
t_1	BOFF/ setup to BCLK HIGH	8	–	ns
t_2	BOFF/ hold from BCLK HIGH	7	–	ns
t_3	BCLK HIGH to TIP/ driven	5	26	ns
t_4	BCLK HIGH to TIP/ LOW	3	14	ns
t_5	BCLK HIGH to TIP/ HIGH	3	14	ns
t_6	BCLK HIGH to TIP/ HIGH-Z	7	28	ns
t_7	BCLK HIGH to TS/ driven	5	25	ns
t_8	BCLK HIGH to TS/ LOW	3	12	ns
t_9	BCLK HIGH to TS/ HIGH	3	12	ns
t_{10}	BCLK HIGH to TS/ HIGH-Z	7	28	ns
t_{11}	TA/ setup to BCLK HIGH	9	–	ns
t_{12}	TA/ hold from BCLK HIGH	5	–	ns
t_{13}	BCLK HIGH to A[31:0], SIZ[1:0] driven	5	24	ns
t_{14}	BCLK HIGH to A[31:0], SIZ[1:0] valid	3	15	ns
t_{15}	BCLK HIGH to A[31:0], SIZ[1:0] HIGH-Z	7	28	ns
t_{16}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] driven and valid	5	25	ns
t_{17}	BCLK HIGH to R_W/, SC[1:0], FC[2:0], TT[1:0] HIGH-Z	5	28	ns
t_{18}	BCLK HIGH to write data driven	5	28	ns
t_{19}	BCLK HIGH to write data valid	7	18	ns
t_{20}	BCLK HIGH to write data HIGH-Z	5	25	ns
t_{21}	TBI/ setup to BCLK HIGH	6	–	ns
t_{22}	TBI/ hold from BCLK HIGH	4	–	ns
t_{23}	TEA/ setup to BCLK HIGH	9	–	ns
t_{24}	TEA/ hold from BCLK HIGH	5	–	ns

Figure 6.23 Bus Mode 2 Bus Master Write Cycle (Noncache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

Figure 6.24 Bus Mode 2 Bus Master Write Cycle (Cache Line Burst)[1]



1. Shaded area indicates that the signal is a don't care.
2. SC[1:0] timings apply only if the Snoop Mode bit (CTEST8, bit 0) equals zero.

6.12 Bus Mode 2 Mux Mode Operation

6.12.1 Mux Mode Read Cycle (Cache Line and Noncache Line Burst)

Mux Mode Read Sequence

1. The SYM53C710 has attained bus mastership.
2. The SYM53C710 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.

3a. The SYM53C710 asserts Transfer in Progress and Transfer Start.

3b. The SYM53C710 asserts the Transfer Start, Address, and Size lines.

4. The SYM53C710 deasserts Transfer Start and floats the Address lines.
5. The SYM53C710 waits for Transfer Acknowledge, Valid Data driven on the data pins, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the SYM53C710 requires more cycles, then return to Step 4.
6. The SYM53C710 deasserts the Control lines.
7. Upon acknowledgment of the last bus cycle, the SYM53C710 deasserts Master and Bus Grant Acknowledge.

   Note: This mode of operation expects D[31:0] to be tied to A[31:0], respectively.

Table 6.42 SYM53C710 Bus Mode 2 Mux Mode Read Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to address driven	6	22	ns
t_2	BCLK HIGH to address HIGH-Z	–	23	ns
t_3	Read data setup to BCLK HIGH	5	–	ns
t_4	Read data hold from BCLK HIGH	6	–	ns

Table 6.43 SYM53C710-1 Bus Mode 2 Mux Mode Read Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to address driven	6	18	ns
t_2	BCLK HIGH to address HIGH-Z	–	18	ns
t_3	Read data setup to BCLK HIGH	5	–	ns
t_4	Read data hold from BCLK HIGH	6	–	ns

Figure 6.25 Mux Mode Read Cycle (Noncache Line Burst)

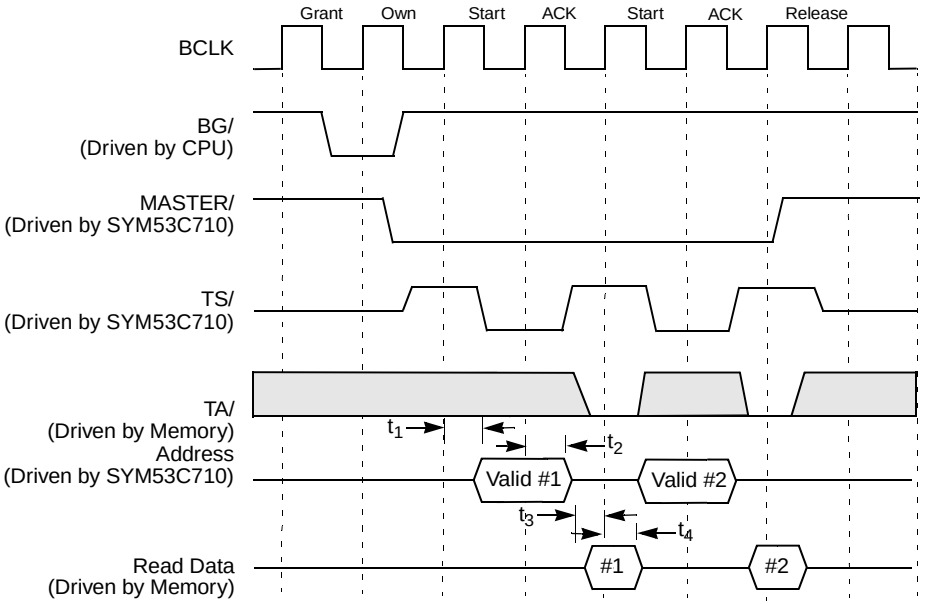
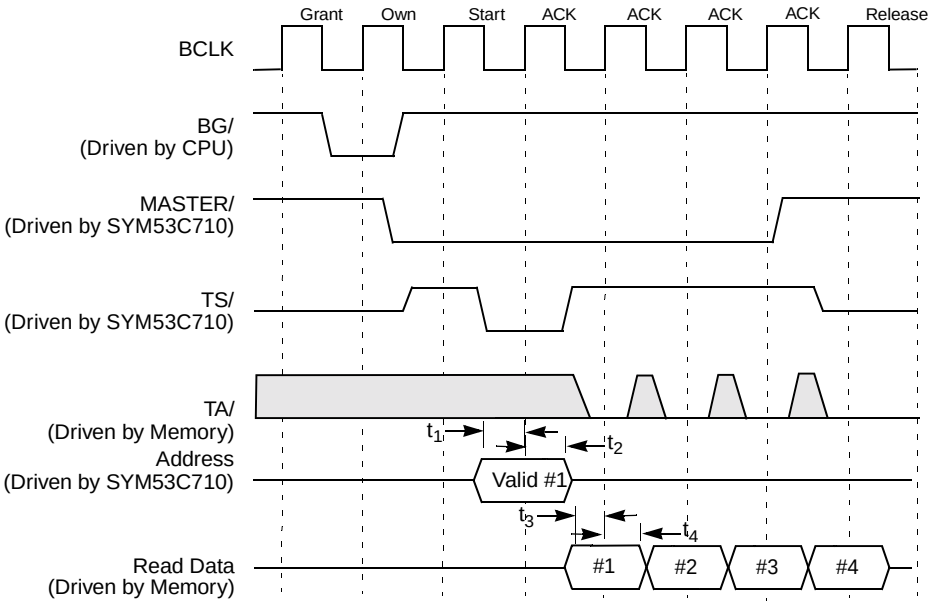


Figure 6.26 Mux Mode Read Cycle (Cache Line Burst)



6.12.2 Mux Mode Write Cycle (Cache Line and Noncache Line Burst)

Mux Mode Write Sequence

1. The SYM53C710 has attained bus mastership.
2. The SYM53C710 asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.

3a. The SYM53C710 asserts Transfer in Progress and Transfer Start.

3b. The SYM53C710 asserts Transfer Start, Address, Size lines, and floats the Data lines.

4. The SYM53C710 deasserts Transfer Start, floats the address bus, and asserts the data bus.
5. The SYM53C710 waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the SYM53C710 requires more cycles, return to Step 4.
6. The SYM53C710 deasserts the Control and Data lines.
7. Upon acknowledgment of the last bus cycle, the SYM53C710 deasserts Master and Bus Grant Acknowledge.

   Note: This mode of operation expects D[31:0] to be physically tied to A[31:0], respectively.

Table 6.44 SYM53C710 Bus Mode 2 Mux Mode Write Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to old data driven	–	34	ns
t_2	BCLK HIGH to address driven	6	22	ns
t_3	BCLK HIGH to new data driven	8	24	ns
t_4	HIGH-Z to driven switching time	1	–	ns
t_5	BCLK HIGH to next data	–	19	ns

Table 6.45 SYM53C710-1 Bus Mode 2 Mux Mode Write Timings

Symbol	Parameter	Min	Max	Units
t_1	BCLK HIGH to old data driven	–	28	ns
t_2	BCLK HIGH to address driven	6	18	ns
t_3	BCLK HIGH to new data driven	8	18	ns
t_4	HIGH-Z to driven switching time	1	–	ns
t_5	BCLK HIGH to next data	–	16	ns

Figure 6.27 Mux Mode Write Cycle (Noncache Line Burst)

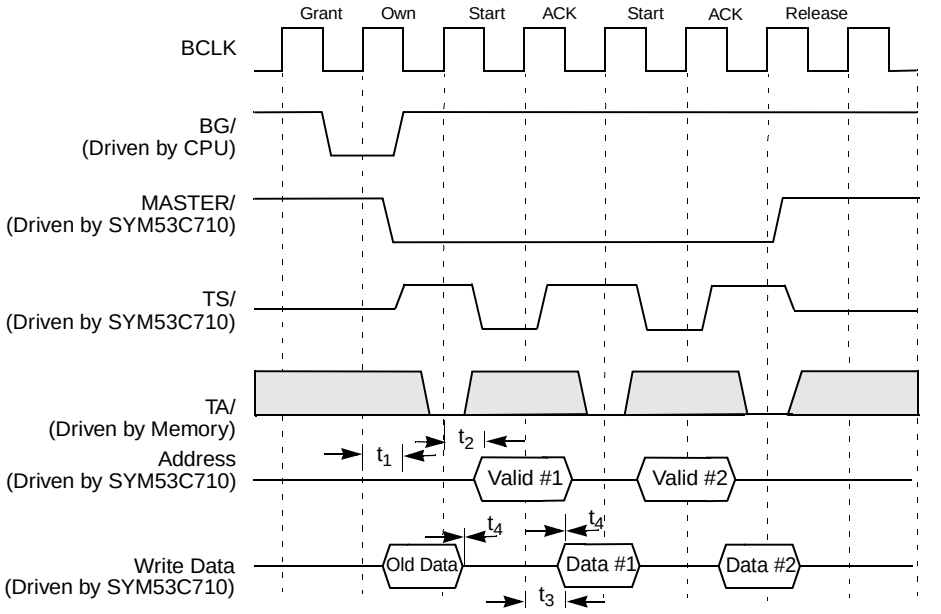


Figure 6.28 Mux Mode Write Cycle (Cache Line Burst)

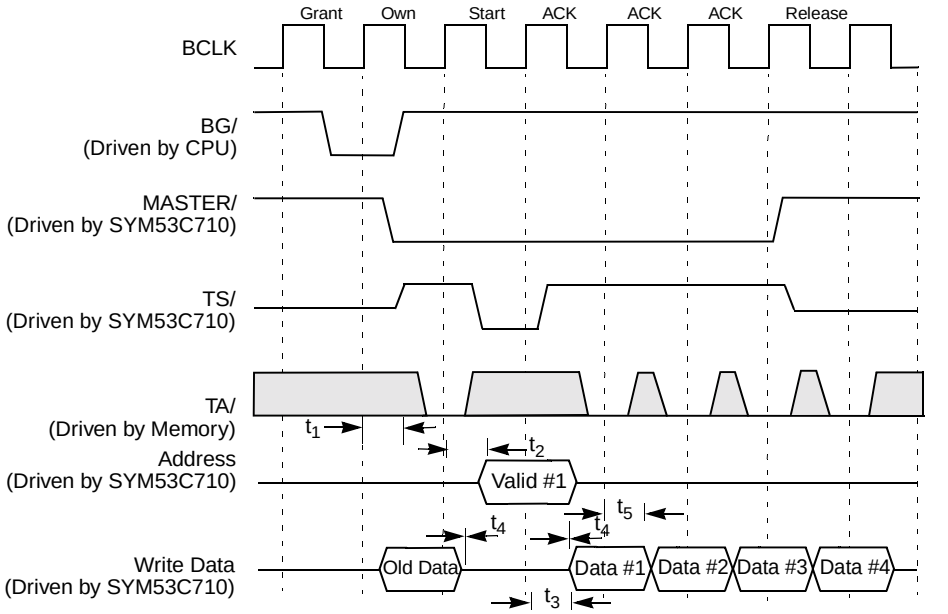


Figure 6.29 Initiator Asynchronous Send

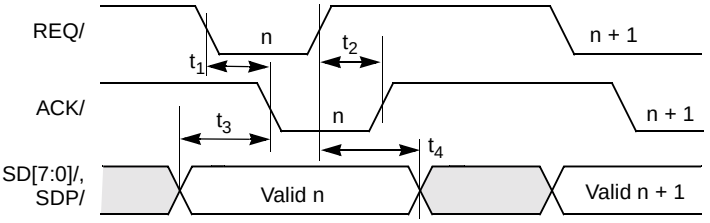


Table 6.46 Initiator Asynchronous Send Timings

Symbol	Parameter	Min	Max	Units
t_1	ACK/ asserted from REQ/ asserted	10	–	ns
t_2	ACK/ deasserted from REQ/ deasserted	10	–	ns
t_3	Data setup to ACK/ asserted	55	–	ns
t_4	Data hold from REQ/ deasserted	20	–	ns

Figure 6.30 Initiator Asynchronous Receive

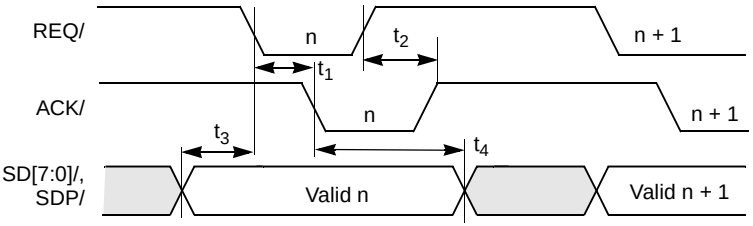


Table 6.47 Initiator Asynchronous Receive Timings

Symbol	Parameter	Min	Max	Units
t_1	ACK/ asserted from REQ/ asserted	10	–	ns
t_2	ACK/ deasserted from REQ/ deasserted	10	–	ns
t_3	Data setup to REQ/ asserted	0	–	ns
t_4	Data hold from ACK/ deasserted	0	–	ns

Figure 6.31 Target Asynchronous Send

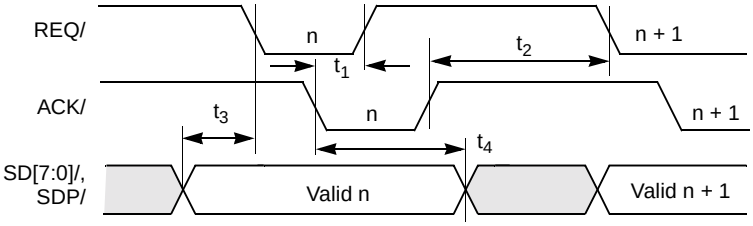


Table 6.48 Target Asynchronous Send Timings

Symbol	Parameter	Min	Max	Units
t_1	REQ/ deasserted from ACK/ asserted	10	–	ns
t_2	REQ/ asserted from ACK/ deasserted	10	–	ns
t_3	Data setup to REQ/ asserted	55	–	ns
t_4	Data hold from ACK/ asserted	20	–	ns

Figure 6.32 Target Asynchronous Receive

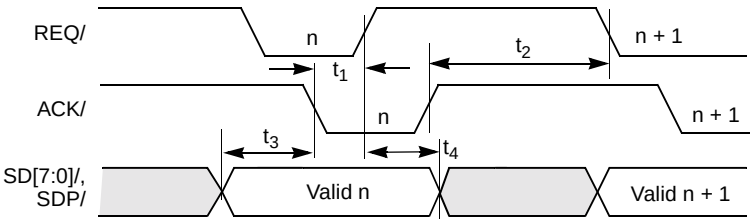


Table 6.49 Target Asynchronous Receive Timings

Symbol	Parameter	Min	Max	Units
t_1	REQ/ deasserted from ACK/ asserted	10	–	ns
t_2	REQ/ asserted from ACK/ deasserted	10	–	ns
t_3	Data setup to ACK/ asserted	0	–	ns
t_4	Data hold from REQ/ deasserted	0	–	ns

Figure 6.33 Initiator and Target Synchronous Transfers

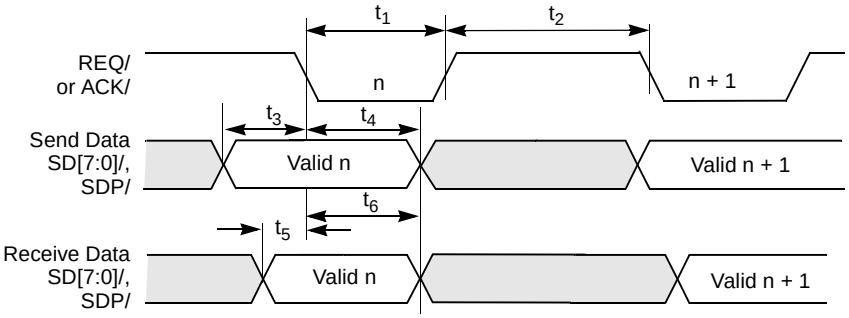


Table 6.50 SCSI-1 Transfers (SE 5.0 Mbytes/s)

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	90	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	90	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	90	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	90	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	55	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	100	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	45	–	ns

Table 6.51 SCSI-1 Transfers (Differential, 4.17 Mbytes/s)

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	95	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	95	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	84	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	84	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	63	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	110	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	45	–	ns

Table 6.52 SCSI-2 Fast Transfers (10.0 Mbytes/s, 40 MHz Clock)

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	35	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	35	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	24	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	24	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	33	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	45	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	10	–	ns

Table 6.53 SCSI-2 Fast Transfers (10.0 Mbytes/s, 50 MHz Clock)[1]

Symbol	Parameter	Min	Max	Units
t_1	Send REQ/ or ACK/ assertion pulse width	35	–	ns
t_2	Send REQ/ or ACK/ deassertion pulse width	35	–	ns
t_1	Receive REQ/ or ACK/ assertion pulse width	24	–	ns
t_2	Receive REQ/ or ACK/ deassertion pulse width	24	–	ns
t_3	Send data setup to REQ/ or ACK/ asserted	33	–	ns
t_4	Send data hold from REQ/ or ACK/ asserted	40[2]	–	ns
t_5	Receive data setup to REQ/ or ACK/ asserted	0	–	ns
t_6	Receive data hold from REQ/ or ACK/ asserted	10	–	ns

1. For fast SCSI, the Enable Active Negation bit (Chip Test Zero (CTEST0), bit 4) should be set. Transfer period bits (Bits [6:4] in SCSI Transfer (SXFER) register) are set to zero and the Extra Clock Cycle of Data Setup bit (Bit 7 in SCSI Control One (SCNTL1)) is set.
2. Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.

Appendix A
Register Summary

Table A.1 SYM53C710 Register Map

Register Name	Big Endian/Little Endian	Read/Write	Page
SCSI Control Zero (SCNTL0)	0x00 (0x03)	Read/Write	4-3
SCSI Control One (SCNTL1)	0x01 (0x02)	Read/Write	4-6
SCSI Destination ID (SDID)	0x02 (0x01)	Read/Write	4-8
SCSI Interrupt Enable (SIEN)	0x03 (0x00)	Read/Write	4-9
SCSI Chip ID (SCID)	0x04 (0x07)	Read/Write	4-10
SCSI Transfer (SXFER)	0x05 (0x06)	Read/Write	4-10
SCSI Output Data Latch (SODL)	0x06 (0x05)	Read/Write	4-14
SCSI Output Control Latch (SOCL)	0x07 (0x04)	Read/Write	4-14
SCSI First Byte Received (SFBR)[1]	0x08 (0x0B)	Read/Write	4-15
SCSI Input Data Latch (SIDL)	0x09 (0x0A)	Read Only	4-16
SCSI Bus Data Lines (SBDL)	0x0A	Read Only	4-17
SCSI Bus Control Lines (SBCL)	0x0B (0x08)	Read/Write	4-17
DMA Status (DSTAT)	0x0C (0x0F)	Read Only	4-18
SCSI Status Zero (SSTAT0)	0x0D (0x0E)	Read Only	4-20
SCSI Status One (SSTAT1)	0x0E (0x0D)	Read Only	4-23
SCSI Status Two (SSTAT2)	0x0F (0x0C)	Read Only	4-25
Data Structure Address (DSA)	0x10–0x13 (0x10–0x13)	Read/Write	4-26
Chip Test Zero (CTEST0)	0x14 (0x17)	Read/Write	4-26
Chip Test One (CTEST1)	0x15 (0x16)	Read Only	4-28

Table A.1 SYM53C710 Register Map (Cont.)

Register Name	Big Endian/Little Endian	Read/Write	Page
Chip Test Two (CTEST2)	0x16 (0x15)	Read Only	4-28
Chip Test Three (CTEST3)	0x17 (0x14)	Read Only	4-30
Chip Test Four (CTEST4)	0x18 (0x1B)	Read/Write	4-30
Chip Test Five (CTEST5)	0x19 (0x1A)	Read/Write	4-32
Chip Test Six (CTEST6)	0x1A (0x19)	Read/Write	4-34
Chip Test Seven (CTEST7)	0x1B (0x18)	Read/Write	4-35
Temporary Stack (TEMP)	0x1C (0x1C–0x1F)	Read/Write	4-37
DMA FIFO (DFIFO)	0x20 (0x23)	Read/Write	4-37
Interrupt Status (ISTAT)	0x21 (0x22)	Read/Write	4-38
Chip Test Eight (CTEST8)	0x22 (0x21)	Read/Write	4-41
Longitudinal Parity (LCRC)	0x23 (0x20)	Read/Write	4-43
DMA Byte Counter (DBC)	0x24–0x26 (0x25–0x27)	Read/Write	4-44
DMA Command (DCMD)	0x27 (0x24)	Read/Write	4-44
DMA Next Data Address (DNAD)	0x28–0x2B (0x28–0x2B)	Read/Write	4-45
DMA SCRIPTS Pointer (DSP)	0x2C–0x2F (0x2C–0x2F)	Read/Write	4-45
DMA SCRIPTS Pointer Save (DSPS)	0x30–0x33 (0x30–0x33)	Read/Write	4-46
Scratch (SCRATCH)	0x34–0x37 (0x34–0x37)	Read/Write	4-46
DMA Mode (DMODE)	0x38 (0x3B)	Read/Write	4-47
DMA Interrupt Enable (DIEN)	0x39 (0x3A)	Read/Write	4-49
DMA Watchdog Timer (DWT)	0x3A (0x39)	Read/Write	4-50
DMA Control (DCNTL)	0x3B (0x38)	Read/Write	4-51
Adder Sum Output (ADDER)	0x3C–0x3F (0x3C–0x3F)	Read Only	4-53

1. Write restrictions apply; refer to register description.

Appendix B
Register and Bit Differences Between the SYM53C710 and SYM53C700

The SYM53C710 can execute all SYM53C700 SCRIPTS without recompilation. However, because there are new registers and bits, and some registers and bits have been relocated or deleted, firmware drivers need to be modified. Table B.1 through Table B.3 summarize the differences between the SYM53C700 and SYM53C710 register sets. The byte addresses are referenced using little endian byte orientation.

Table B.1 New Registers and Bits

Item	SYM53C700	SYM53C710
Synchronous SCSI Clock Control Bits	N/A	SBCL, Bits [1:0]
Bus Fault Bit	N/A	DSTAT, Bit 5
Data Structure Address Register	N/A	DSA
SIGnal Process Test & Reset Bit	N/A	CTEST2, Bit 6
MUX Mode Bit	N/A	CTEST4, Bit 7
Cache Burst Disable Bit	N/A	CTEST7, Bit 7
Snoop Control Bits [1:0]	N/A	CTEST7, Bits [6:5]
Transfer Type One Bit	N/A	CTEST7, Bit 1
Byte Offset Six Bit	N/A	DFIFO, Bit 6
SIGnal Process Set Bit	N/A	ISTAT, Bit 5
CTEST8 Register	N/A	CTEST8
FETCH/ Pin Control Bit	N/A	CTEST8, Bit 1
Snoop Mode Bit	N/A	CTEST8, Bit 0
LCRC Register	N/A	LCRC
Scratch Register	N/A	SCRATCH
Function Code Bits [2:1]	N/A	DMODE, Bits [5:4]
Program/Data Function Code 0 Control Bit	N/A	DMODE, Bit 3
UPSO-TT0/Bit	N/A	DMODE, Bit 1
Bust Fault Interrupt Enable Bit	N/A	DIEN, Bit 5
Enable Acknowledge Control Bit	N/A	DCNTL, Bit 5
Fast Arbitration Mode Bit	N/A	DCNTL, Bit 1
SYM53C700 Compatibility Bit	N/A	DCNTL, Bit 0
Adder Output Register	N/A	ADDER
Filter Delay Select Bit	N/A	CTEST0, Bit 2
Halt SCSI Clock Bit	N/A	CTEST0, Bit 3
Enable Active Deassertion Bit	N/A	CTEST0, Bit 4
Generate Receive Parity Bit	N/A	CTEST0, Bit 5
Byte-to-Byte Disable Bit	N/A	CTEST0, Bit 6

Table B.2 Deleted Bits

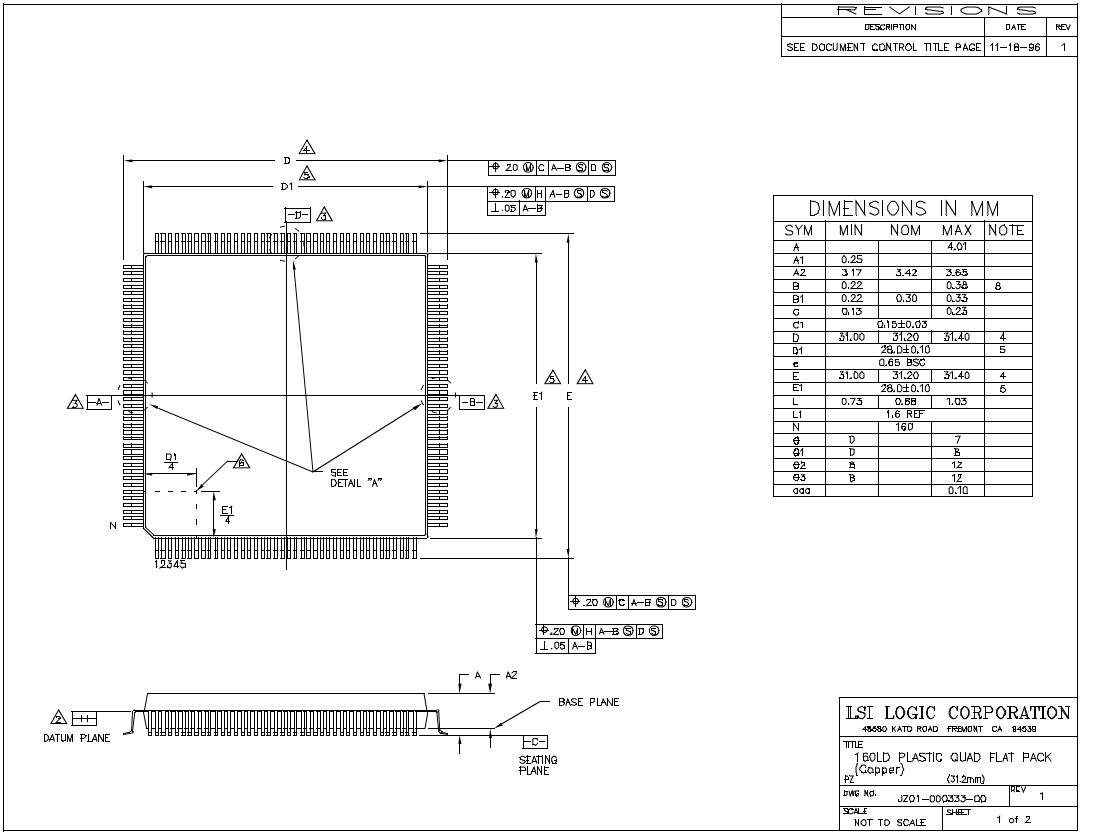
Item	SYM53C700	SYM53C710
DC/Pin Control Bit	CTEST7, Bit 1	N/A
DSPS and DSP Empty Bit	ISTAT, Bit 2	N/A
16-bit DMA, 286 Mode Bits	DMODE, Bits [5:4]	N/A
I/O Memory Mapped DMA Bit	DMODE, Bit 3	N/A
Pipeline Mode Bit	DMODE, Bit 1	N/A
16-bit SCSI SCRIPTS Mode Bit	DCNTL, Bit 5	N/A
Real Target Mode Bit	CTEST0, Bit 1	N/A
Start SCSI Send	SCNTL, Bit 1	N/A
Start SCSI Receive	SCNTL, Bit 0	N/A

Table B.3 Moved Registers and Bits

Item	SYM53C700	SYM53C710
Flush FIFO Bit	DFIFO, Bit 7	CTEST8, Bit 3
Clear FIFO Bit	DFIFO, Bit 6	CTEST8, Bit 2
Software Reset Bit	DCNTL, Bit 0	ISTAT, Bit 6
Chip Revision Level Bits	CTEST7, Bits [7:4]	CTEST8, Bits [7:4]
DMODE Register	Address 34h	Address 38h

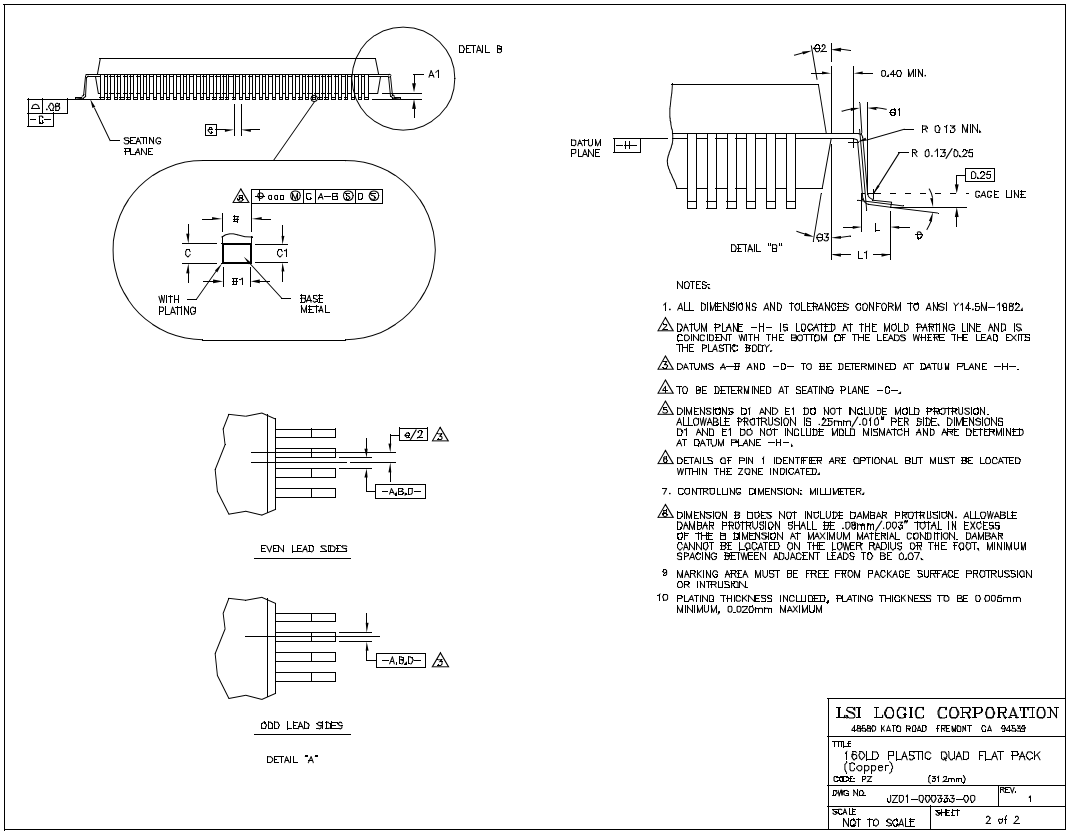
Appendix C
Mechanical Drawing

Figure C.1 160-Pin PQFP (PZ) Mechanical Drawing (Sheet 1 of 2)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PZ.**

Figure C.1 160-Pin PQFP (PZ) Mechanical Drawing (Sheet 2 of 2)



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Appendix D
Setting Data Transfer Rates

This appendix contains the following sections:

D.1 Setting the SYM53C700-66 Transfer Rate

This appendix explains how to get the proper data transfer speed on the SCSI bus when using the SYM53C700-66 SCSI I/O Processor chip.

Data transfer rates are controlled by the configuration of the following bits.

Register 0x0B SCSI Bus Control Line (SBCL) - bits 1 (SSCF1) and 0 (SSCF0) – SSCF[1:0] bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The output from this divider must not exceed 50 MHz.

Register 0x3B DMA Control (DCNTL) - bits 7 (CF1) and 6 (CF0) – CF[1:0] bits select the factor by which the frequency of SCLK is divided before being presented to the asynchronous SCSI core logic. This divider must be set according to the input clock frequency in the table. The output from this divider must not exceed 25 MHz.

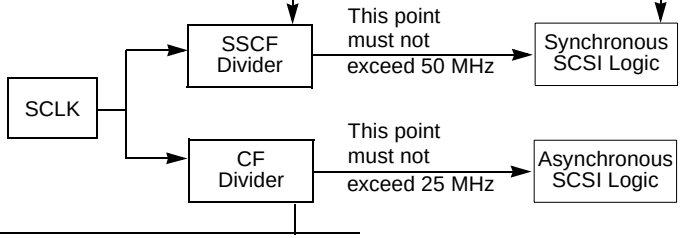
Register 0x05 SCSI Transfer (SXFER) - bits 6 (TP2), 5 (TP1) and 4 (TP0) – TP[2:0] determines the SCSI synchronous transfer period when sending synchronous SCSI data in either initiator or target mode.

These bits control the programmable dividers in the chip. On the following page are tables of these bits and the division factors they produce. Figure D.1 shows how the chip uses the divisors.

Figure D.1 Divisor Usage

SSCF1	SSCF0	SSCF Divisor
0	0	Set by DCNTL
0	1	1.0
1	0	1.5
1	1	2.0

TP2	TP1	TP0	XFERP Divisor
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11



CF1	CF0	CF Divisor	SCLK (MHz)
0	0	2.0	37.51–50.00
0	1	1.5	25.01–37.50
1	0	1.0	16.67–25.00
1	1	3.0	50.01–66.67

Example:
SCLK = 40 MHz, SCSI Transfer Rate = 10 Mbytes/s
SSCF = 1, CF = 0, XFERP = 4 (TP = 0)
(40 MHz / 1 = 40 MHz synchronous logic speed)
(40 MHz / 2 = 20 MHz asynchronous logic speed)
SCSI synchronous logic speed / XFERP = SCSI synchronous rate
(40 MHz / 4 = 10 MHz = 10 Mbytes/s)

D.2 SYM53C7XX, SYM53C8XX to 75LBC976/76A Differential Interface

Following is a suggested interface between the SYM53C700, SYM53C700-66, SYM53C710, SYM53C720, or SYM53C820 SCSI I/O Processors (SIOP) and the Texas Instruments 75LBC976 differential transceiver. This appendix does not apply to the SYM53C810, which has a Single-Ended (SE) interface only. The 75LBC976 is capable of 10 Mbytes/s transfers and contains nine differential transceivers in one package, which reduces the board space required to implement a differential SCSI interface. The purpose of this appendix is to guide people in their own designs. The designer should perform a thorough design analysis before implementing this interface.

D.2.1 Differential Mode

The SIOP must be placed in differential mode by setting the DIF bit, bit 5 of the STEST2 register (0x4E) in the SYM53C720 and SYM53C820, or bit 0 of the CTEST7 register (0x1B) in the SYM53C700, SYM53C700-66, and SYM53C710. Setting this bit 3-states the BSY/, SEL/, and RST/ pads so they can be used as pure input pins. In addition to the standard SCSI lines, the following signals are used during differential operation by the SIOP in all bus modes:

Signal	Function
BSYDIR, SELDIR, RSTDIR	Active high signals used to enable 75LBC976 differential drivers as outputs for SCSI signals BSY/, SEL/, and RST/ respectively
SDIR[15:0], SDIRP[1:0]	Active high signals used to control direction of 75LBC976 differential drivers for SCSI data and parity lines, respectively
IGS	Active high signal used to control direction of 75LBC976 differential driver for initiator group signals ATN/ and ACK/
TGS	Active high signal used to control direction of 75LBC976 differential drivers for target group signals MSG/, C/D/, I/O/, and REQ/
DIFFSENS	Input to SIOP used to detect the presence of a SE device on a differential system. If a logical zero is detected on this pin, then it is assumed that a SE device is on the bus and all SCSI outputs will be 3-stated to avoid damage to the transceiver

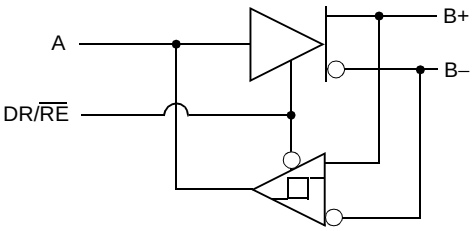
D.2.2 TI 75LBC976 Architecture

The 75LBC976 is made up of nine differential transceiver channels. Each of these channels has a direction control pin and bidirectional data pin. The direction control pin, labeled nDE/RE/ (where n is a value from 1 through 9), controls the direction of the transceiver. Pulling the signal high enables the channel as an output to the SCSI bus, and low enables the channel as an input from the SCSI bus. These direction control pins will be connected to the DIR, IGS, and TGS pins of the Symbios SIOP.

The bidirectional data pins, labeled nA (n is a value from 1 through 9), are configured as inputs or outputs depending upon the state of their respective direction control (nDE/RE/) pins. When the direction control pin is high, the data line is configured as an input; when the direction control pin is low, the line is configured as an output. These data lines are connected to the Symbios SIOP's SCSI data and control pins.

The nA and nDE/RE/ pins are the only direct contact with the transceiver. There are no separate pins for the input and output of the channel, nor are there separate input and output enables. The signals from the inputs and outputs of the transceiver are tied together internally to form the bidirectional data pin (nA). This is also true of the enables for the input and output of the transceiver channel. These two enables, one active high and the other active low, are tied together internally to form the direction control pin (nDE/RE/). An example transceiver channel is shown in Figure D.2. There are five other control pins on the 75LBC976 labeled CDE0, CDE1, CDE2, BSR, and CRE/. All of these lines are grounded in the interface except for CDE0. This pin controls the functionality of all the channels on the transceiver. When this pin is high, the channels are configured as fully functional bidirectional transceivers. When it is low, they are configured as input only transceivers. The CDE0 pin is connected to the DIFFSENS SCSI signal, to protect the transceiver if a SE device is plugged onto the SCSI bus.

Figure D.2 TI 75LBC976 Differential Transceiver



D.2.3 Interface

To interface the Symbios SIOP to the 75LBC976, connect the DIR pins, as well as IGS and TGS, of the SIOP directly to the transceiver enables (nDE/RE/). These signals control the direction of the channels on the 75LBC976. The SCSI bidirectional control and data pins (SD[7:0]/, SDP0/, REQ/, ACK/, MSG/, I_O/, C_D/, and ATN/) of the Symbios SIOP connect to the bidirectional data pins (nA) of the 75LBC976 with a pull-up resistor. The three remaining pins, SEL/, BSY/, and RST/ are connected to the 75LBC976 with a pull-down resistor. The pull-down resistors are required when the data pins (nA) of the 75LBC976 are configured as inputs. When the data pins are inputs, the resistors provide a bias voltage to both the SIOP pins (SEL/, BSY/, and RST/) and the 75LBC976 data pins. Because the SEL/, BSY/, and RST/ pins on the Symbios SIOP are inputs only, this configuration allows for the SEL/, BSY/ and RST/ SCSI signals to be asserted on the SCSI bus. The interface in shown in Figure D.3.

D.2.4 Pull-up Resistor Value

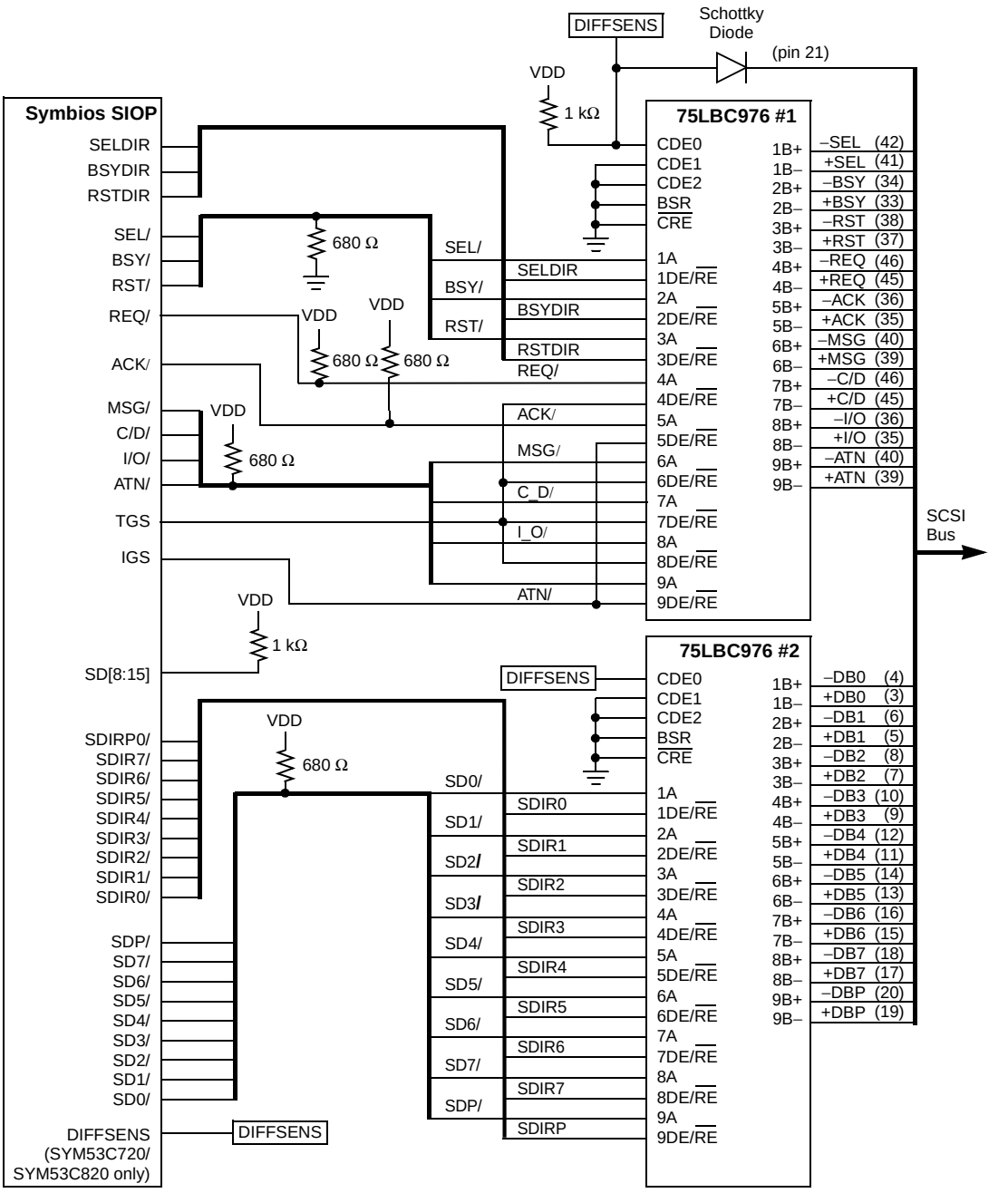
The recommended value of the pull-up resistor on the REQ/, ACK/, MSG/, C/D/, I/O/, ATN/, SD[0:7]/, and SDP0/ lines is 680 Ω when the Active Negation portion of Symbios TolerANT technology is not enabled. When TolerANT is enabled, the recommended resistor value on the REQ/, ACK/, SD[7:0]/, and SDP0/ signals is 1.5 kΩ. The electrical characteristics of these pins change when TolerANT is enabled, permitting a higher resistor value.

D.2.5 8-Bit/16-Bit SCSI and the Differential Interface

The interface described in this appendix is for an 8-bit SCSI bus. For a 16-bit bus (Wide SCSI, supported on SYM53C720 and SYM53C820 only) another 75LBC976 should be used in the same fashion as the 75LBC976 #2 in Figure D.3. SD[8:15]/, SDIR[8:15], SDP1/ and SDIRP1 should be connected to the third 75LBC976.

Note: In an 8-bit SCSI bus, the SD[15:8] pins on the Symbios SIOP should be pulled up with a 1 kΩ resistor or terminated like the rest of the SCSI bus lines. This is very important, as errors may occur during reselection if these lines are left floating.

Figure D.3 Symbios SIOP to 75LBC976 Differential Interface



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