MPC7400 Part Number Specification

This document describes part number specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7400 Hardware Specifications*.

Specifications provided in this Part Number Specification supersede those in the *MPC7400 Hardware Specifications* dated 9/99 (order #: MPC7400EC/D) for these part numbers only; specifications not addressed herein are unchanged. This document is frequently updated, refer to the website at http://www.mot.com/SPS/PowerPC/ for the latest version.

Note that headings and table numbers in this data sheet are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table A. For more detailed ordering information see Table B.

Table A. Part Numbers Addressed by this Data Sheet

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	Vdd	T_J (°C)	
XSC7400RX350PE	350 MHz	2.15V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve350Mhz frequency
XSC7400RX400PE	400 MHz	2.15V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 400Mhz frequency
XSC7400RX350PG	350 MHz	2.15V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 350Mhz frequency
XSC7400RX350NG	350 MHz	2.10V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 350Mhz frequency
XSC7400RX400NG	400 MHz	2.10V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 400Mhz frequency

Note: The X prefix in a Motorola PowerPC part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes
The S designation in XSC indicates that these parts have been screened for the “global waitr” problem. (See your local Motorola sales office.)

1.2 General

This section summarizes changes to the features of the MPC7400 described in the *MPC7400 Hardware Specifications*.

- None.

Any functional differences (errata) for these parts from the functional description provided in the *MPC7400 RISC Microprocessor User’s Manual* (order # MPC7400UM/AD) are described below.

- This part has known functional errata. Consult your local Motorola Sales Office.

1.4.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7400 part numbers described herein.

Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		Vdd	2.15V±50mV	
PLL supply voltage		AVdd	2.15V±50mV	
L2 DLL supply voltage		L2AVdd	2.15V±50mV	
Processor bus supply voltage	BVSEL = 0	OVdd	Not Recommended	V
	BVSEL = 1	OVdd	3.15 to 3.45	V
L2 bus supply voltage	L2VSEL = 0	L2OVdd	Not Recommended	V
	L2VSEL = $\overline{\text{HRESET}}$	L2OVdd	2.4 to 2.6	V
	L2VSEL = 1	L2OVdd	3.15 to 3.45	V
Input voltage	Processor bus	V_{in}	GND to OVdd	V
	L2 Bus	V_{in}	GND to L2OVdd	V
	JTAG Signals	V_{in}	GND to OVdd	V
Die-junction temperature		T_j	0-65	°C

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. Operation at OVdd = 1.8V or L2OVdd = 1.8V when Vdd is at 2.15V is not recommended

Table 7 provides the power consumption for the MPC7400 part at the frequencies described herein.

Table 7. Power Consumption for MPC7400

	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	450Mhz		
Full-On Mode				
Typical	7.9	8.9	W	1, 3, 4
Maximum	15.5	16.3	W	1, 2, 4
Doze Mode				
Maximum	6.7	7.5	W	1, 2
Nap Mode				
Maximum	2.7	3.0	W	1, 2
Sleep Mode				
Maximum	2.7	3.0	W	1, 2
Sleep Mode—PLL and DLL Disabled				
Typical	600	600	mW	1, 3
Maximum	1.0	1.0	W	1, 2

Notes:
See General hardware specification

1.4.2.1 Clock AC Specifications

Table 8 provides the additional clock AC timing specifications described in this Part Number Specification. Refer to the MPC7400 Hardware Specification for the remaining frequencies.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (See Table 3)

Characteristic	Symbol	400 MHz		450 MHz		Unit	Notes
		Min	Max	Min	Max		
Processor frequency	f_{core}	225	400	225	450	MHz	
VCO frequency	f_{VCO}	450	800	450	900	MHz	
SYSCLK frequency	f_{SYSCLK}	33	133	33	150	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	6.67	30	ns	
SYSCLK rise and fall time	t_{KR} & t_{KF}	—	1.0	—	1.0	ns	2
		—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at OVdd/2	t_{KHKL}/t_{SYSCLK}	40	60	40	60	%	4
SYSCLK jitter		—	±150	—	±150	ps	5
Internal PLL relock time		—	100	—	100	μs	6

Notes:
See General hardware specification.

1.4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7400 part described in this Part Number Specification.

Table 9. Processor Bus AC Timing Specifications[1]

At Vdd=AVdd=2.15V±50mV; 0 ≤ Tj ≤ 105°C, OVdd = 3.3V±165mV and OVdd = 2.5V±100mV, Times for OVdd=1.8V±100mV are TBD

Parameter	Symbol	400, 450 Mhz		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	2,3,4,5
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	2,3,5
Setup Times:				ns	10
Address/Transfer Attribute	t_{AVKH}	1.4	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSVKH}	1.4	—		—
Data/Data Parity	t_{DVKH}	1.4	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARVKH}	1.4	—		—
All Other Inputs	t_{IVKH}	1.4	—		8
Input Hold Times:				ns	11
Address/Transfer Attribute	t_{AXKH}	0	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSXKH}	0	—		—
Data/Data Parity	t_{DXKH}	0	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARXKH}	0	—		—
All Other Inputs	t_{IXKH}	0	—		8
Valid Times:				ns	12
Address/Transfer Attribute	t_{KHAV}	—	3.0		6
$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$	t_{KHTSV}	—	3.0		—
Data	t_{KHDV}	—	3.5		7
Data Parity	t_{KHDPV}	—	3.5		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{KHARV}	—	2.3		—
All Other Outputs	t_{KHOV}	—	3.0		9
Output Hold Times:				ns	13
Address/Transfer Attribute	t_{KHAX}	0.75	—		6
$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$	t_{KHTSX}	0.75	—		—
Data/Data Parity	t_{KHDX}	0.6	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{KHARX}	0.75	—		—
All Other Outputs	t_{KHOX}	0.75	—		9
SYSCLK to Output Enable	t_{KHOE}	0.5	—	ns	14
SYSCLK to Output High Impedance (all except $\overline{\text{TS}}$, $\overline{\text{ABB}}$/$\overline{\text{AMON(0)}}$, $\overline{\text{ARTRY}}$/$\overline{\text{SHD}}$, $\overline{\text{DBB}}$/$\overline{\text{DMON(0)}}$)	t_{KHOZ}	—	3.5	ns	15
SYSCLK to $\overline{\text{TS}}$, $\overline{\text{ABB}}$/$\overline{\text{AMON(0)}}$, $\overline{\text{DBB}}$/$\overline{\text{DMON(0)}}$ High Impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	4,15, 16,17
Maximum Delay to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ Precharge	t_{KHARP}	—	1	t_{sysclk}	4,17
SYSCLK to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ High Impedance After Precharge	t_{KHARPZ}	—	2	t_{sysclk}	4,17

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.
2. Maximum power is measured at Vdd = 2.2V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 2.15V, OVdd = L2OVdd = 3.3V in a system while running a codec application that is AltiVec intensive.

1.4.2.3 L2 Clock AC Specifications

Table 10 provides the L2CLK Output AC Timing Specifications for the MPC7400 part described in this Part Number Specification.

Table 10. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3)

Parameter	Symbol	400 MHz		450 MHz		Unit	Notes
		Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	150	400	150	450	MHz	1
L2CLK cycle time	t_{L2CLK}	2.5	6.67	2.22	6.67	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	50		50		%	2
Internal DLL-relock time		640	—	640	—	L2CLK	4
DLL capture window			±200		±200	ns	5

Notes:
See General hardware specification.

1.4.2.4 L2 Bus AC Specifications

Table 11 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this Part Number Specification.

Table 11. L2 Bus Interface AC Timing Specifications

At Vdd=AVdd=L2AVdd= 2.15V±50mV; 0 ≤ Tj ≤ 65°C, L2OVdd = 3.3V±165mV and L2OVdd = 2.5V±100mV, Times for L2OVdd=1.8V±100mV are TBD

Parameter	Symbol	400, 450 MHz		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} & t_{L2CF}	—	1.0	ns	1
Setup Times: Data and parity	t_{DVL2CH}	1.5	—	ns	2
Input Hold Times: Data and parity	t_{DXL2CH}	—	0.0	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOV}	 - - - -	 2.5 3.0 3.5 4.0	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOX}	 0.6 1.0 1.4 1.8	 - - - -	ns	3

Table 11. L2 Bus Interface AC Timing Specifications

At Vdd=AVdd=L2AVdd= 2.15V±50mV; 0 ≤ Tj ≤ 65°C, L2OVdd = 3.3V±165mV and L2OVdd = 2.5V±100mV, Times for L2OVdd=1.8V±100mV are TBD

Parameter	Symbol	400, 450 MHz		Unit	Notes
		Min	Max		
L2SYNC_IN to high impedance: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOZ}	 - - - -	 2.0 2.5 3.0 3.5	ns	
Notes: See General Hardware Specification					

1.10 Ordering Information

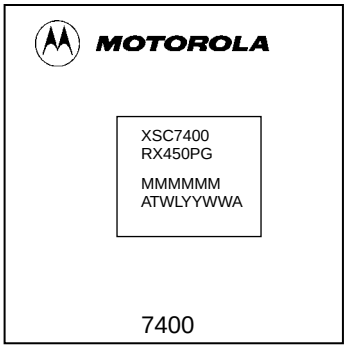
Table B provides the ordering information for the MPC7400 part described in this Part Number Specification..

Table B. Ordering Information for the MPC7400 Microprocessor

Package Type	Device Rev	Process	Mask Code	CPU Frequency (MHz)	Motorola Part Number
360 CBGA	2.2	HIP 5.0	72J87W	350MHz	XSC7400RX350PE
				400MHz	XSC7400RX400PE
	2.6		76J87W	350MHz	XSC7400RX350PG
				350MHz	XSC7400RX350NG
				400MHz	XSC7400RX400NG

1.10.1 Part Marking

Parts are marked as the example shown in Figure A.



BGA

Notes:

MMMMMM is the 6-digit mask number

ATWLYYWWA is the traceability code

CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

Figure A. Motorola Part Marking for BGA Devices