FUJITSU

256K x 8 CMOS SRAM MODULE

MB85403A-40
MB85403A-50

TS261-A88Y
Nov. 1988

CMOS 262,144 Words x 8-Bit STATIC RANDOM ACCESS MEMORY MODULE

PRELIMINARY

The Fujitsu MB85403A is a fully decoded, CMOS static random access memory module consists of eight MB81C81A devices mounted on a 44-pin ceramic board. Organized as eight 256K x 1 devices, the MB85403 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

- Organized as 262,144 x 8-bit Words
- Memory : MB81C81A, 8 pcs
- Access Time : 40 ns max (MB85403A-40)
  50 ns max (MB85403A-50)
- Low Power Dissipation
  Standby: 660 mW max (CMOS level)
  1320 mW max (TTL level)
  Active : 5280 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- 44-Pin 100 MIL Ceramic Twin SIP (TSIP)

CERAMIC PACKAGE
MTP-44C-C02

PIN ASSIGNMENT
TOP VIEW

GND	1	44	VCC
DOUT0	2	43	DOUT7
DIN0	3	42	DIN7
A16	4	41	A0
A17	5	40	A1
A13	6	39	A2
GND	7	38	A3
DOUT1	8	37	DOUT6
DIN1	9	36	DIN6
A12	10	35	A4
A11	11	34	A7
NC	12	33	/WE
/CSA	13	32	/CSB
DOUT2	14	31	DOUT5
DIN2	15	30	DIN5
A14	16	29	GND
A15	17	28	A6
A10	18	27	A5
A9	19	26	A8
DOUT3	20	25	DOUT4
DIN3	21	24	DIN4
VCC	22	23	GND

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ABSOLUTE MAXIMUM RATING (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM

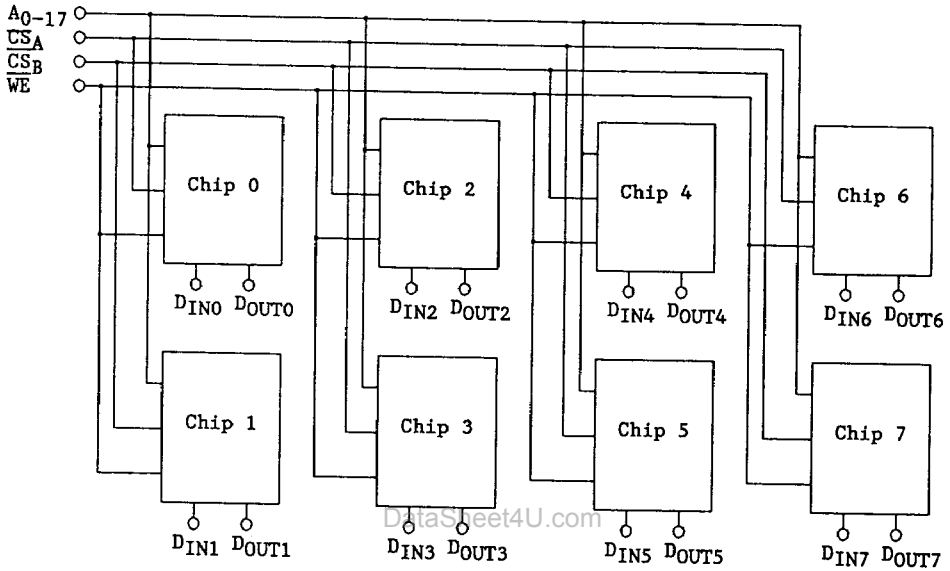

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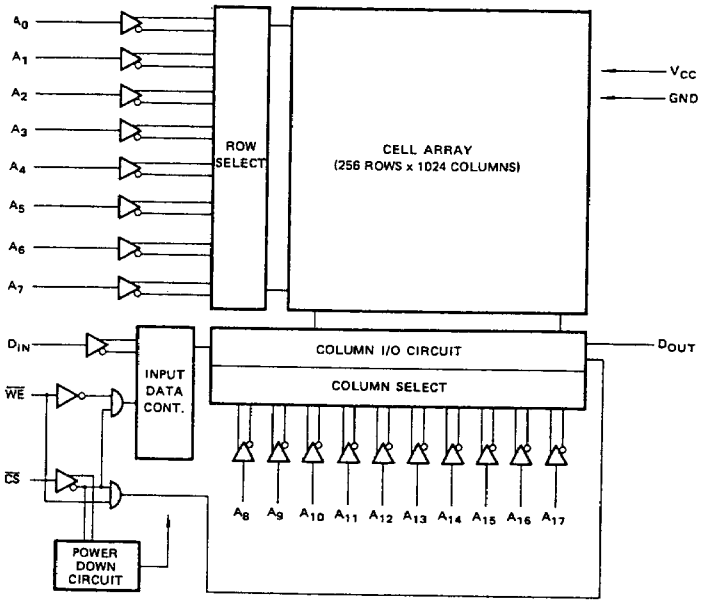
Fig. 2 – BLOCK DIAGRAM for EACH MEMORY



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (except $\overline{CS}_A$, $\overline{CS}_B$)	C_{IN}		100	pF
Input Capacitance ($\overline{CS}_A$+$\overline{CS}_B$)	$C_{\overline{CS}}$		120	pF
Output Capacitance	C_{OUT}		20	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}_A$	$\overline{CS}_B$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	DON'T CARE	V_{IH}	V_{IH}	DON'T CARE	HIGH-Z	HIGH-Z	STANDBY
WRITE	VALID	V_{IL}	V_{IL}	V_{IL}	D_{IN}	HIGH-Z	ACTIVE
READ	VALID	V_{IL}	V_{IL}	V_{IH}	HIGH-Z	D_{OUT}	ACTIVE

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-80		80	μA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-50		50	μA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			120	mA
	TTL level	I_{SB2}			240	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA)	MB85403A-40	I_{CC}			960	mA
	MB85403A-50				800	
PEAK POWER ON SUPPLY CURRENT ($\overline{CS}$=Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *1		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=16mA)		V_{OL}			0.4	V

Note: *1 -3.0V min. for pulse width less than 20ns.

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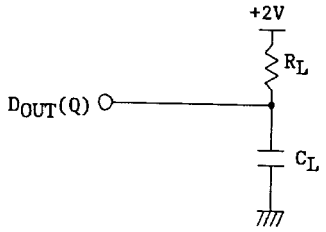
Fig. 3 - AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns
- Timing Reference Levels : V_{IL}/V_{OL}=0.8V, V_{IH}/V_{OH}=2.2V
- Output Load :



	R_L	C_L
Load I	100Ω	30pF
Load II	100Ω	5pF

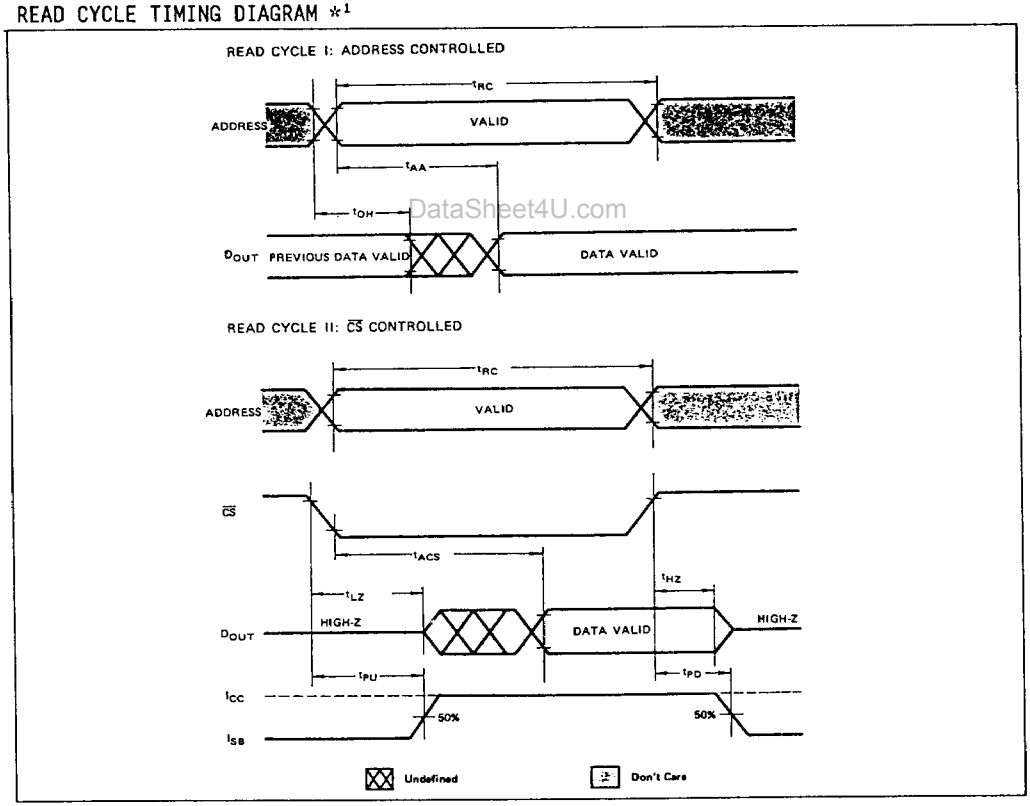
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB85403A-40		MB85403A-50		Unit
		Min	Max	Min	Max	
Read Cycle Time *2	t_{RC}	40		50		ns
Address Access Time	t_{AA}		40		50	ns
CS Access Time *3	t_{ACS}		40		50	ns
Output Hold from Address Change	t_{OH}	5		5		ns
CS to Output Low-Z *4*5	t_{LZ}	5		5		ns
CS to Output High-Z *4*5	t_{HZ}	0	25	0	30	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		40		50	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high during Read cycle.
*2 Device is continuously selected, $\overline{CS}$=V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 3.

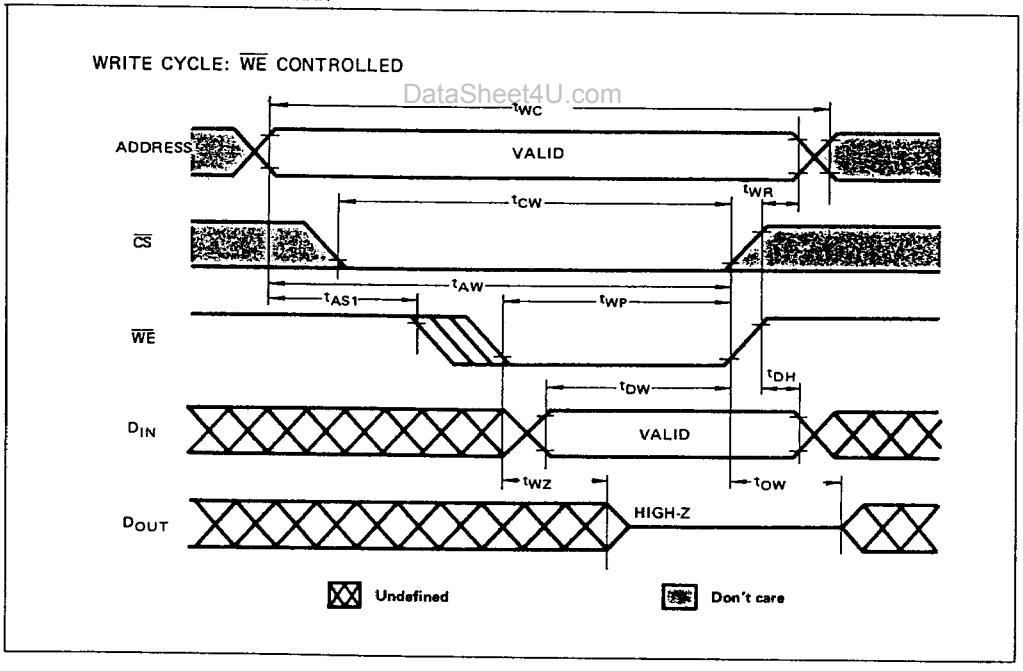
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85403A-40		MB85403A-50		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	40		50		ns
Address Valid to End of Write	t_{AW}	35		45		ns
CS to End of Write	t_{CW}	35		45		ns
Data Valid to End of Write	t_{DW}	25		30		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	25		30		ns
Address Setup Time	t_{AS1}	5		5		ns
	t_{AS2}	0		0		ns
Write Recovery Time	t_{WR}	5		5		ns
Output High-Z from WE *3*4	t_{WZ}	0	25	0	30	ns
Output Low-Z from WE *3*4	t_{OZ}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

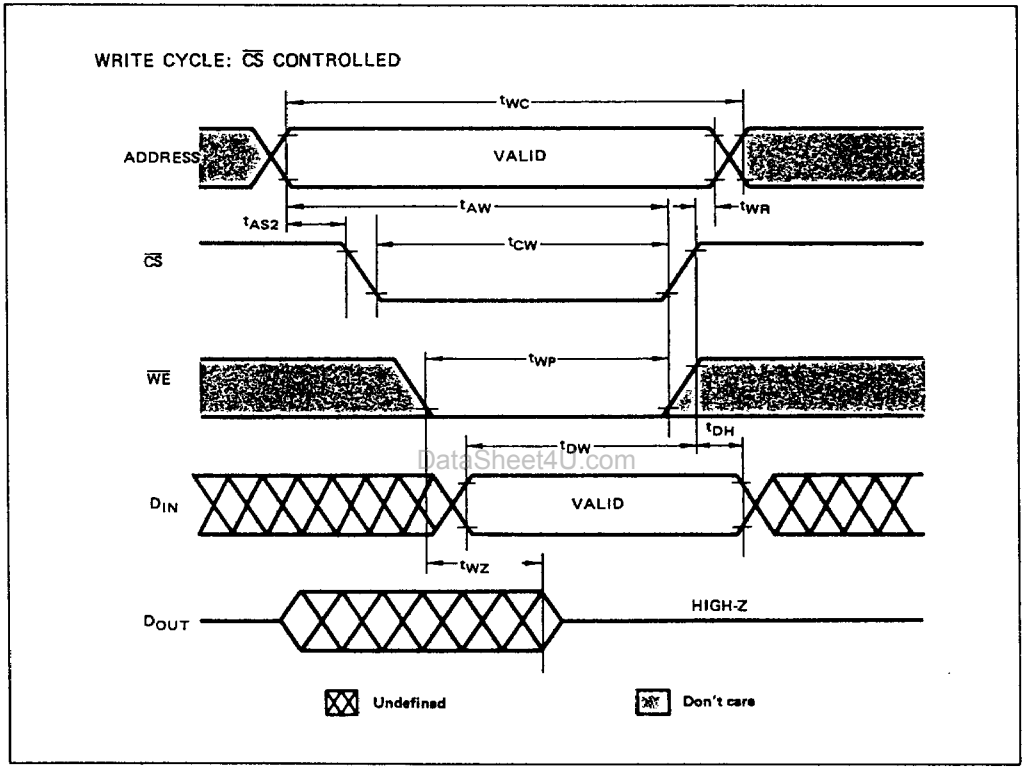
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM



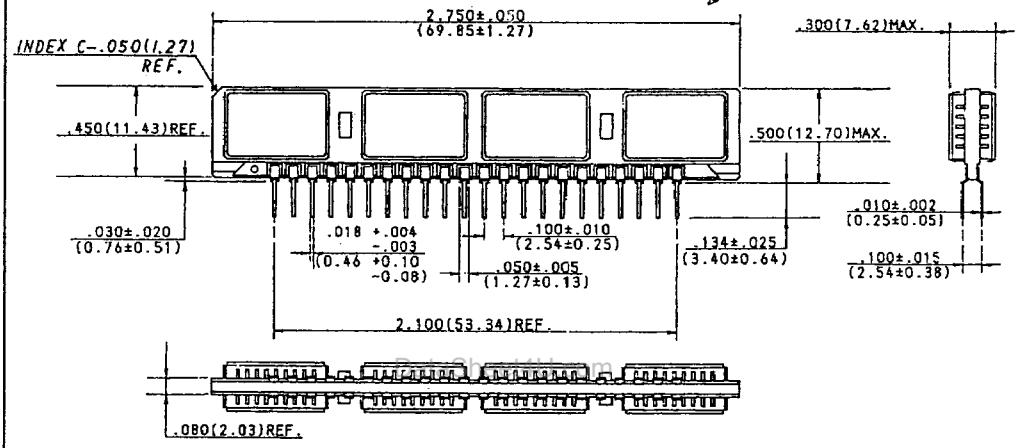
Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

PACKAGE DIMENSIONS

(Suffix: CVCT)

44-LEAD CERAMIC DUAL IN-LINE MODULE
(Case No.: MTP-44C-C02)

PRELIMINARY



NOTE
1. Dimension in inches and (millimeters).

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