

NP50P03YDG

MOS FIELD EFFECT TRANSISTOR

R07DS0019EJ0200 Rev.2.00 Mar 16, 2011

Description

The NP50P03YDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - --- $R_{DS(on)}$ = 8.4 mΩ MAX. (V_{GS} = -10 V, I_D = -25 A)
- Low C_{iss} : $C_{iss} = 2300 \text{ pF TYP}$. $(V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP50P03YDG -E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP50P03YDG -E2-AY *1			8-pin HSON, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	-30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	∓20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	∓50	A
Drain Current (pulse) *1	I _{D(pulse)}	∓200	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	102	W
Total Power Dissipation (T _A = 25°C) *2	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	−55 to +175	°C
Single Avalanche Current *3	I _{AS}	24	Α
Single Avalanche Energy *3	E _{AS}	58	mJ



<R>

Thermal Resistance

Notes: *1. $T_C = 25^{\circ}C$, PW $\leq 10 \mu s$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt

*3. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = –20 \rightarrow 0 V

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.



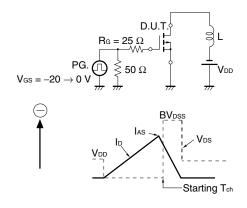
Electrical Characteristics ($T_A = 25^{\circ}C$)

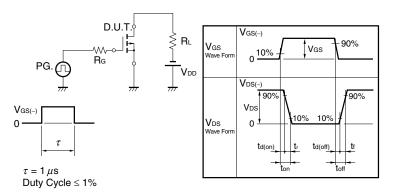
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			-1	μΑ	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			∓100	nA	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	-1.0	-1.6	-2.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$
Forward Transfer Admittance *1	y _{fs}	23	46		S	$V_{DS} = -5 \text{ V}, I_{D} = -25 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		6.7	8.4	mΩ	$V_{GS} = -10 \text{ V}, I_D = -25 \text{ A}$
Resistance *1	R _{DS(on)2}		8.5	13	mΩ	$V_{GS} = -5 \text{ V}, I_D = -25 \text{ A}$
Input Capacitance	C _{iss}		2300	3500	pF	$V_{DS} = -25 \text{ V},$
Output Capacitance	Coss		440	660	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		320	580	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		9	19	ns	$V_{DD} = -15 \text{ V}, I_D = -25 \text{ A},$
Rise Time	t _r		7	16	ns	$V_{GS} = -10 \text{ V},$
Turn-off Delay Time	$t_{d(off)}$		230	470	ns	$R_G = 0 \Omega$
Fall Time	t _f		180	440	ns	
Total Gate Charge	Q_G		64	96	nC	$V_{DD} = -24 \text{ V},$
Gate to Source Charge	Q_{GS}		9		nC	$V_{GS} = -10 \text{ V},$
Gate to Drain Charge	Q_{GD}		21		nC	I _D = -50 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		1.0	1.5	V	$I_F = -50 \text{ A}, V_{GS} = 0 \text{ V}$
Reverse Recovery Time	t _{rr}		49		ns	$I_F = -50 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		44		nC	di/dt = 100 A/μs

Note: *1. Pulsed

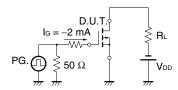
TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



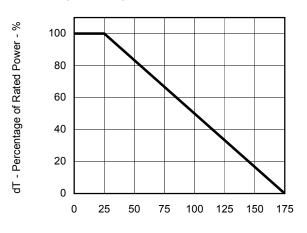


TEST CIRCUIT 3 GATE CHARGE



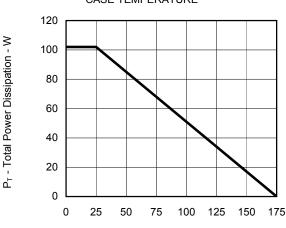
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



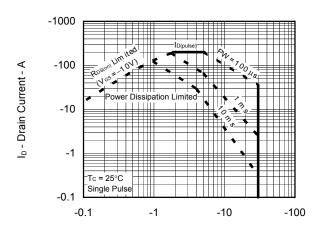
 T_{C} - Case Temperature - $^{\circ}\text{C}$

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



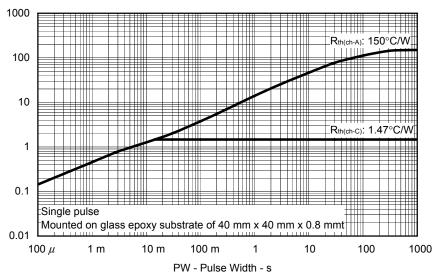
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



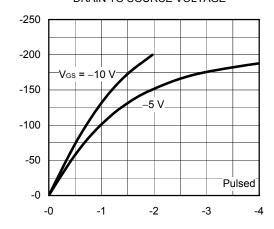


I_D - Drain Current - A

V_{GS(th)} - Gate to Source Threshold Voltage - V

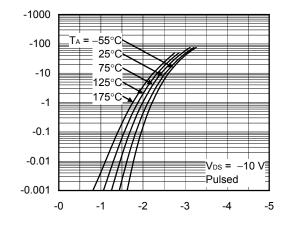
 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$





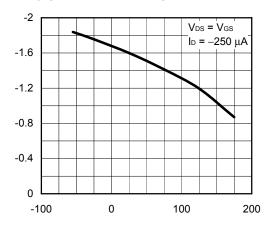
 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS



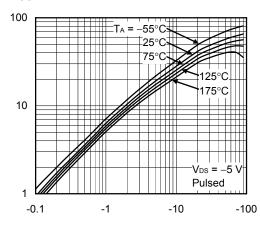
V_{GS} - Gate to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



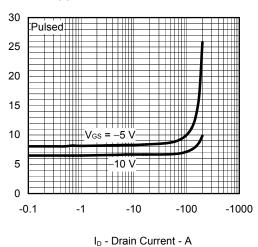
T_{ch} - Channel Temperature - °C

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



ID - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

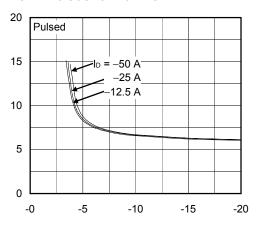


 $R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

Ip - Drain Current - A

y_{fs} | - Forward Transfer Admittance - S

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

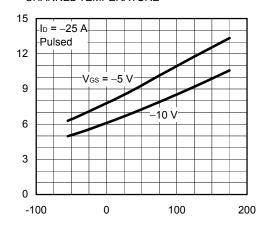


V_{GS} - Gate to Source Voltage - V

t_{d(on)}, t_r, t_{d(off)}, t_f - Switching Time - ns

I_F - Diode Forward Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



 T_{ch} - Channel Temperature - $^{\circ}C$

-1

-0.1

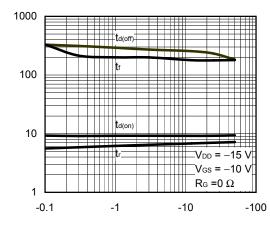
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

 V_{DS} - Drain to Source Voltage - V

-10

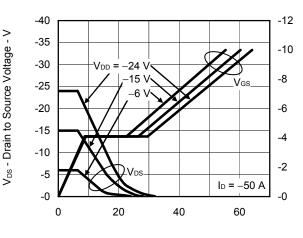
-100

SWITCHING CHARACTERISTICS



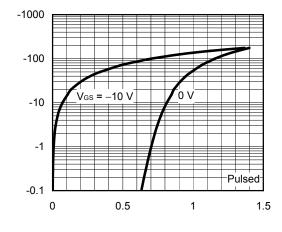
ID - Drain Current - A

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



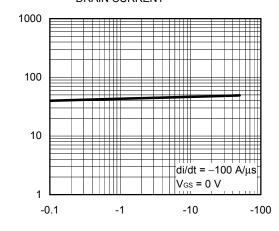
Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



 $V_{F(S\text{-}D)}$ - Source to Drain Voltage - V

REVERSE RECOVERY TIME vs. DRAIN CURRENT

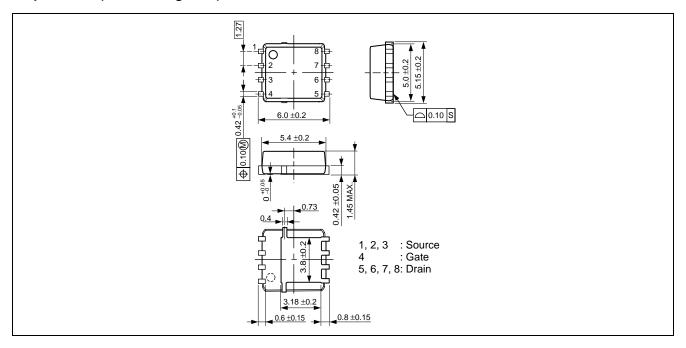


I_F - Drain Current - A

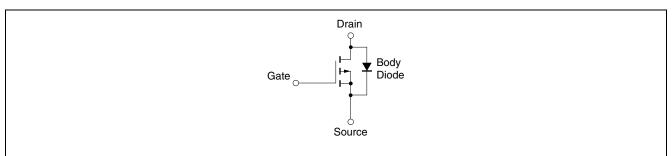
t_{rr} - Reverse Recovery Time - ns

Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP50P03YDG Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Jul 01, 2010	-	First Edition Issued	
2.00	Mar 16, 2011	p.1	Repetitive Avalanche Current -> Single Avalanche Current	
			Repetitive Avalanche Energy -> Single Avalanche Energy	
			Modification of Note *3	

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