Dual P-Channel 12-V (D-S) MOSFET

CHARACTERISTICS

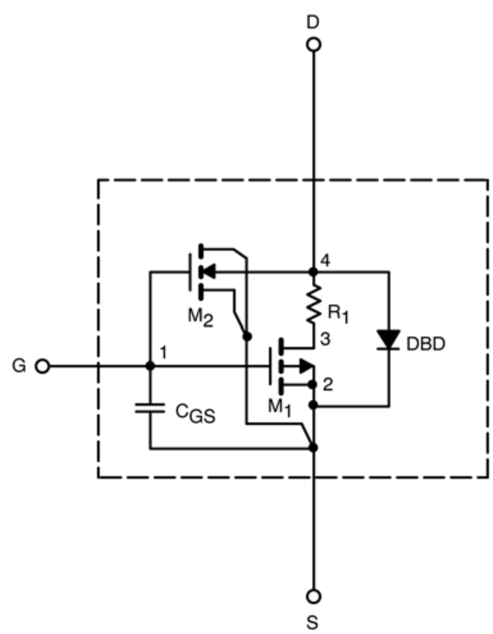
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0 to 4.5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

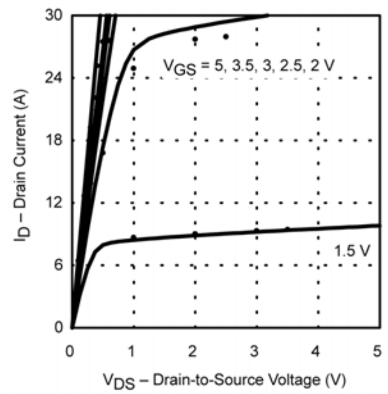


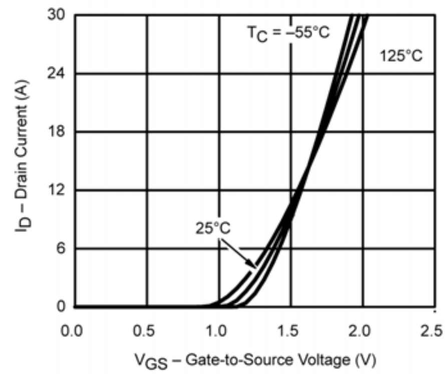
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

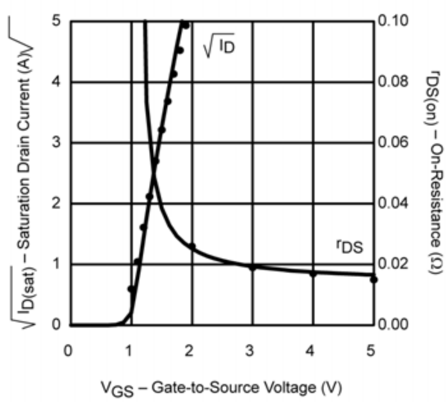
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Conditions**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = –400 µA	0.81		V
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –4.5 V	196		A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –5.8 A	0.017	0.016	Ω
		V_{GS} = –2.5 V, I_D = –5 A	0.021	0.021	
		V_{GS} = –1.8 V, I_D = –4.4 A	0.029	0.029	
Forward Transconductance[b]	g_{fs}	V_{DS} = –5 V, I_D = –5.8 A	27	25	S
Diode Forward Voltage[b]	V_{SD}	I_S = –1 A, V_{GS} = 0 V	–0.78	–0.61	V
Dynamic[a]					
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –5.8 A	19	18.5	nC
Gate-Source Charge	Q_{gs}		2.7	2.7	
Gate-Drain Charge	Q_{gd}		5	5	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω	58	45	ns
Rise Time	t_r		39	80	
Turn-Off Delay Time	$t_{d(off)}$		134	130	
Fall Time	t_f		35	80	

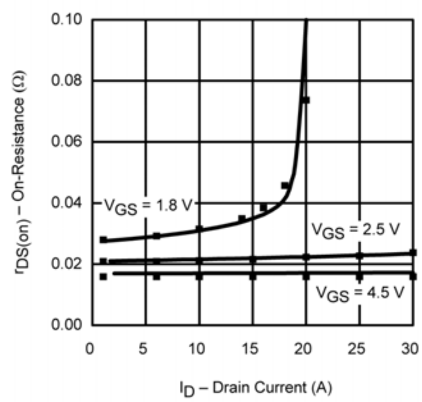
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

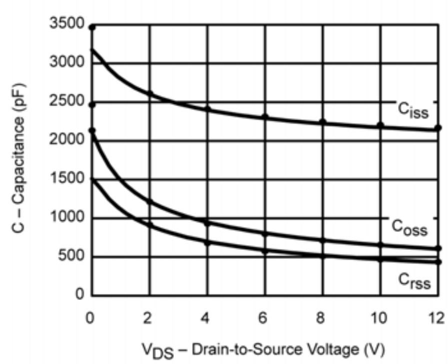
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

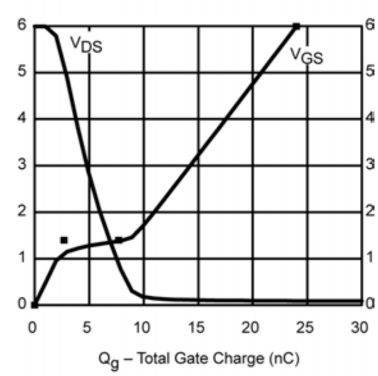












Note: Dots and squares represent measured data.

Disclaimer

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