

# FDP036N10A

## N-Channel PowerTrench® MOSFET

100V, 214A, 3.6mΩ

### Features

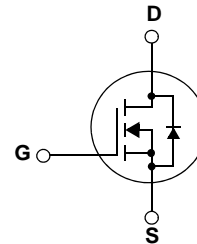
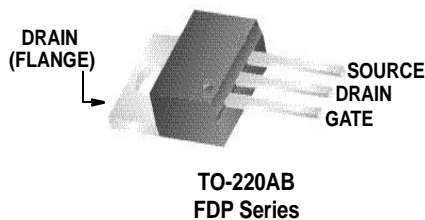
- $R_{DS(on)} = 3.2m\Omega$  (Typ.) @  $V_{GS} = 10V, I_D = 75A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC to DC Convertors / Synchronous Rectification



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	214*
		- Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	151*
		- Continuous ( $T_C = 25^\circ\text{C}$ , Package Limited)	120
$I_{DM}$	Drain Current	- Pulsed (Note 1)	856
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	658
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	333
		- Derate above $25^\circ\text{C}$	2.22
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

### Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP036N10A	FDP036N10A	TO-220	-	-	50

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ , $T_C = 25^\circ\text{C}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.07	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 80\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	500	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 75\text{A}$	-	3.2	3.6	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}$ , $I_D = 75\text{A}$ (Note 4)	-	167	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	5485	7295	pF
$C_{oss}$	Output Capacitance		-	2430	3230	pF
$C_{riss}$	Reverse Transfer Capacitance		-	210	315	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 80\text{V}$ , $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$	-	89	116	nC
$Q_{gs}$	Gate to Source Gate Charge		-	24	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	25	-	nC

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}$ , $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GEN} = 4.7\Omega$	-	22	54	ns
$t_r$	Turn-On Rise Time		-	54	118	ns
$t_{d(off)}$	Turn-Off Delay Time		-	37	84	ns
$t_f$	Turn-Off Fall Time		-	11	32	ns
ESR	Equivalent Series Resistance (G-S)		-	1.2	-	$\Omega$

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	214	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	856	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_{SD} = 75\text{A}$	-	-	1.25	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}$ , $I_{SD} = 75\text{A}$ , $V_{DD} = 80\text{V}$	-	72	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt = 100\text{A}/\mu\text{s}$	-	129	-	nC

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $I_{AS} = 36.3\text{A}$
3.  $I_{SD} \leq 75\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

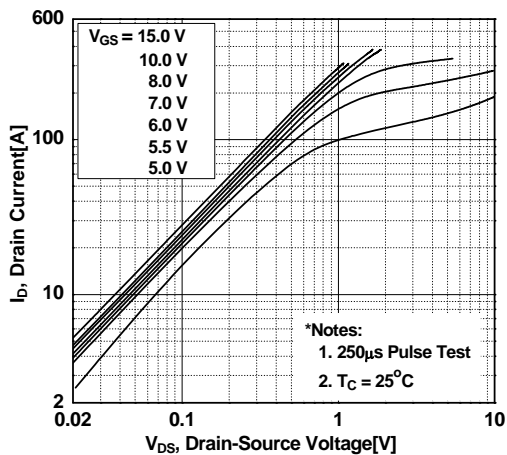


Figure 2. Transfer Characteristics

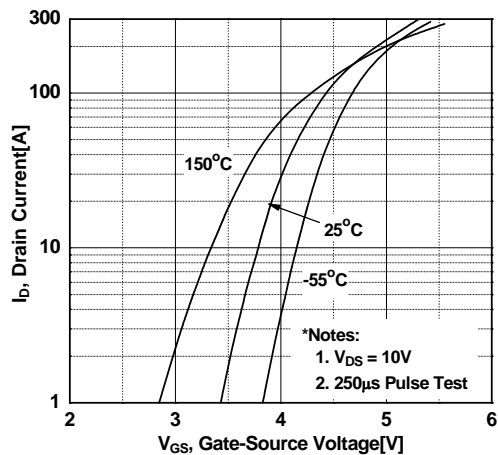


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

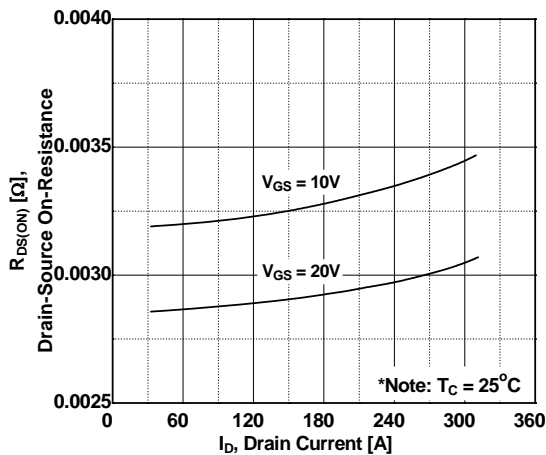


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

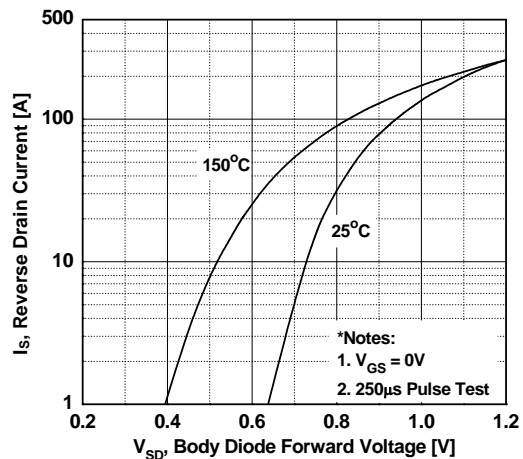


Figure 5. Capacitance Characteristics

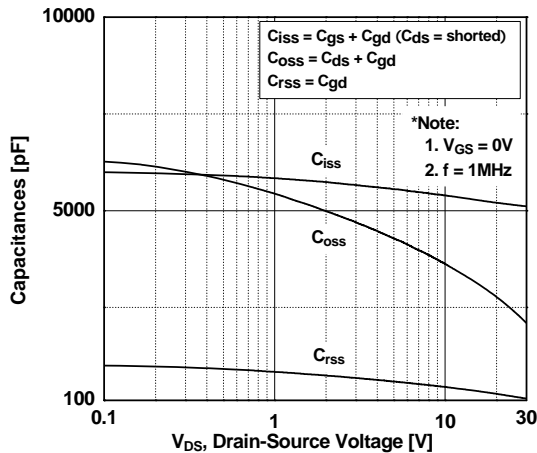
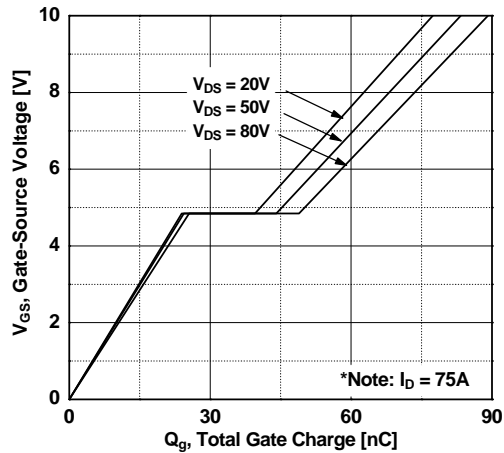
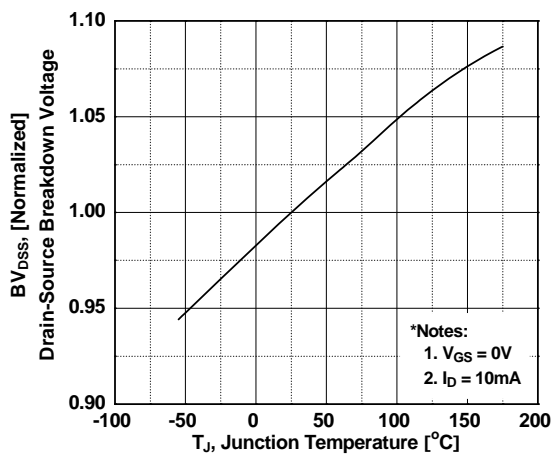


Figure 6. Gate Charge Characteristics

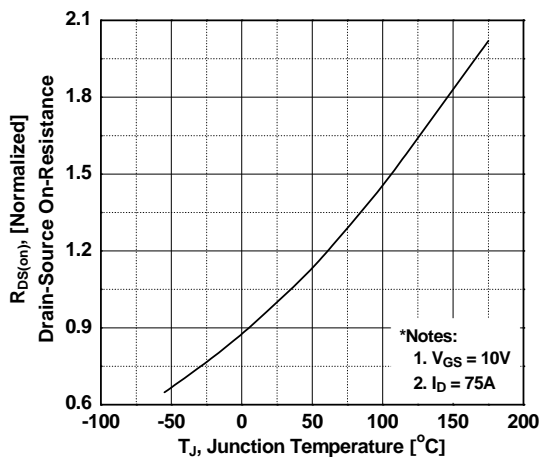


## Typical Performance Characteristics

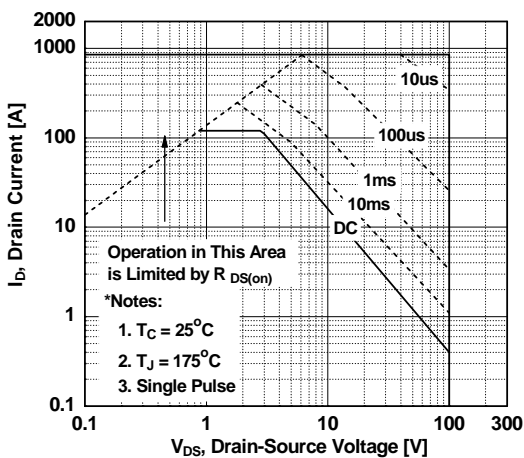
**Figure 7. Breakdown Voltage Variation vs. Temperature**



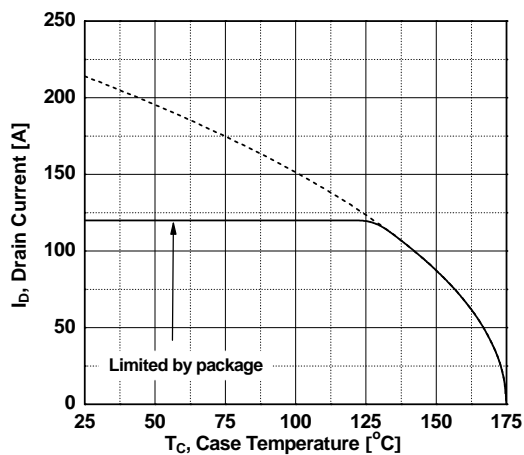
**Figure 8. On-Resistance Variation vs. Temperature**



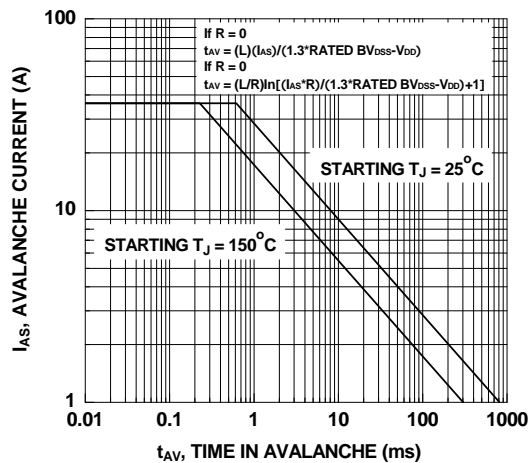
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

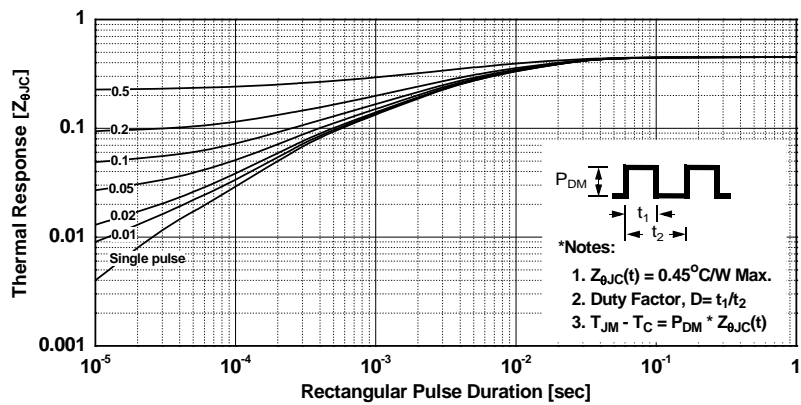


**Figure 11. Unclamped Inductive Switching Capability**

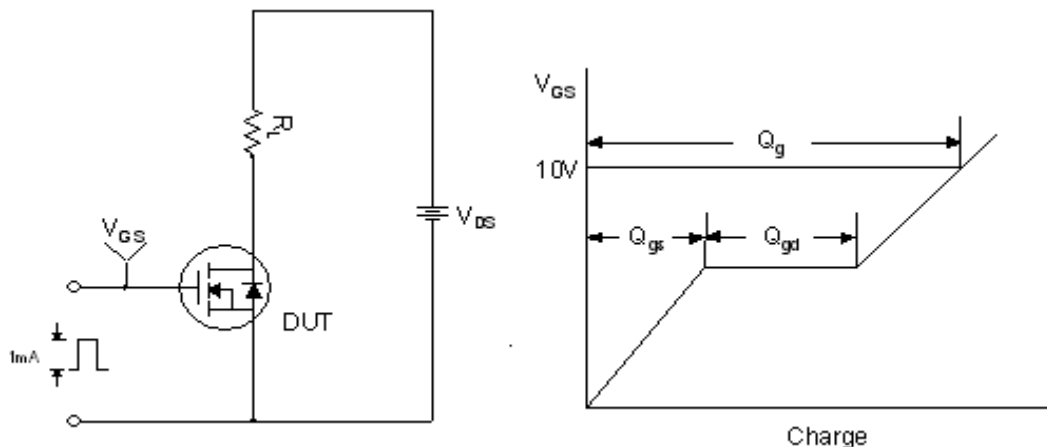


## Typical Performance Characteristics

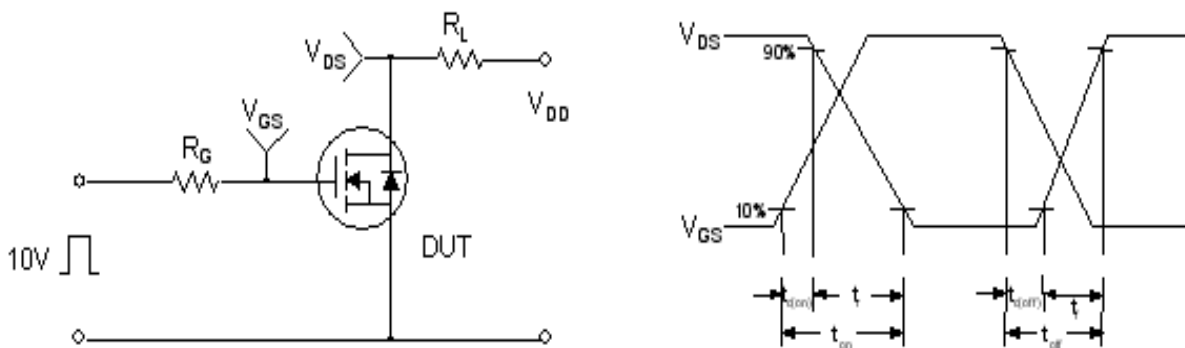
Figure 12. Transient Thermal Response Curve



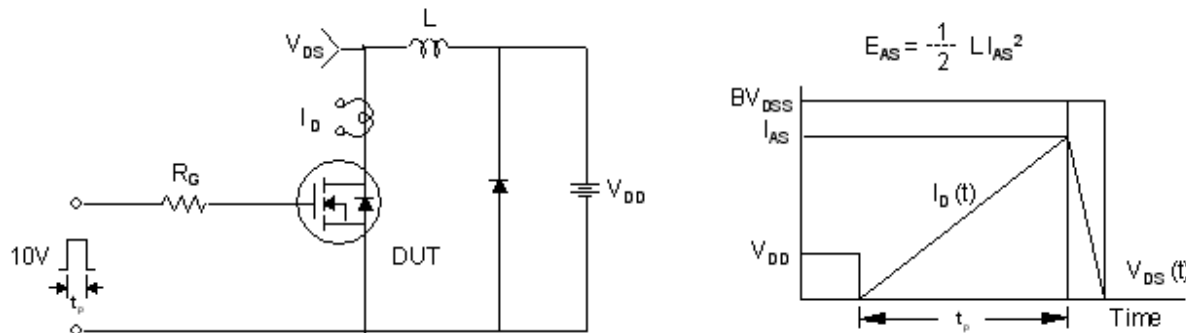
**Gate Charge Test Circuit & Waveform**



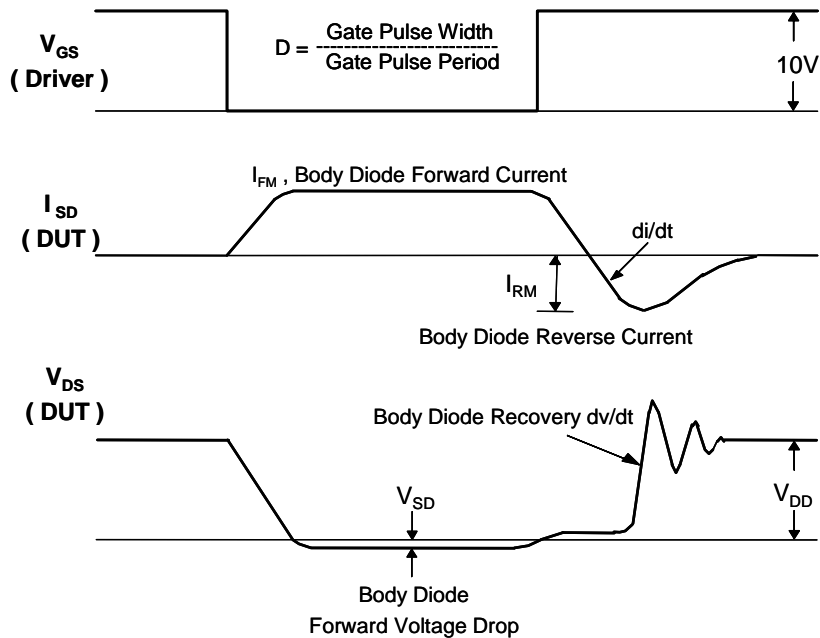
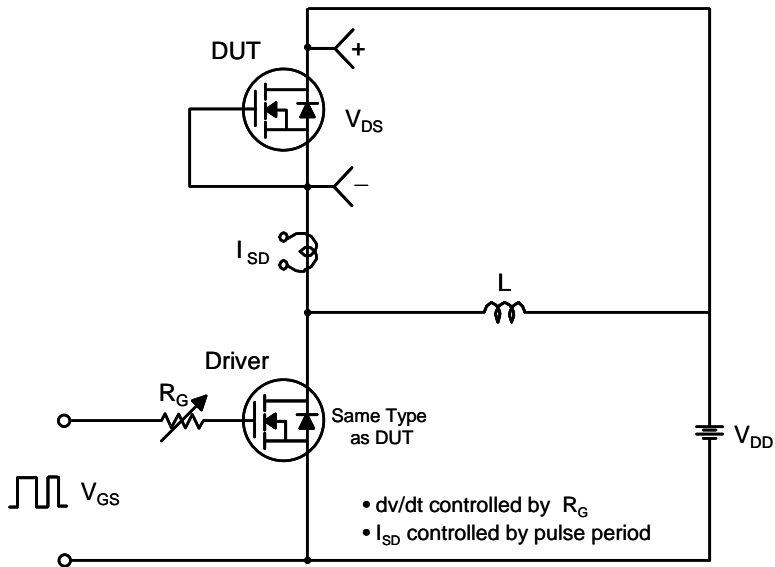
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

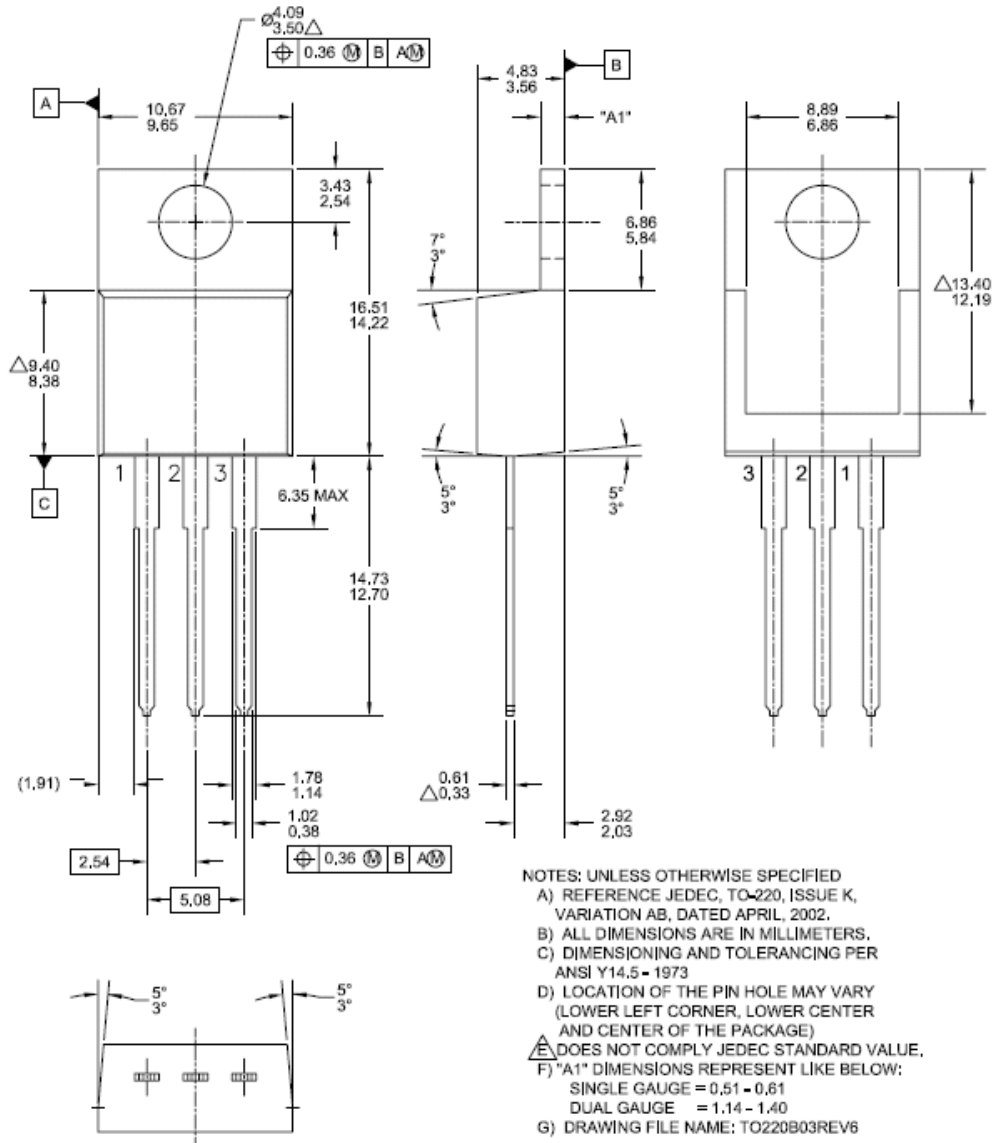


Peak Diode Recovery dv/dt Test Circuit & Waveforms



# Mechanical Dimensions

## TO-220AB



- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973  
 D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)  
 E) DOES NOT COMPLY JEDEC STANDARD VALUE.  
 F) "A1" DIMENSIONS REPRESENT LIKE BELOW:  
 SINGLE GAUGE = 0.51 - 0.61  
 DUAL GAUGE = 1.14 - 1.40  
 G) DRAWING FILE NAME: TO220B03REV6



FDP036N10A N-Channel PowerTrench<sup>®</sup> MOSFET





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| Auto-SPM™   | F-PFS™                              | PowerTrench®                          | the   |
| AX-CAPT™*   | FRFET®                              | PowerXS™                              | <b>power</b>  |
| BitSiC®   | Global Power Resource <sup>SM</sup> | Programmable Active Droop™            | franchise   |
| Build it Now™   | Green FPST™                         | QFET®                                 | TinyBoost™  |
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| CorePOWER™  | Gmax™                               | Quiet Series™                         | TinyCalc™   |
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| DEUXPEED®   | MegaBuck™                           | SignalWise™                           | TinyPWM™  |
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| Fairchild®  | MotionMax™                          | SuperSOT™-3                           |  |
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| FAST®   | OPTOLOGIC®                          | SyncFET™                              | VCX™  |
| FastvCore™  | OPTOPLANAR®                         | Sync-Lock™                            | VisualMax™  |
| FETBench™   |                                     |                                       | XS™   |

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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