YAMAHA LSI

YTD427

APPLICATION MANUAL

IAFE ISDN DSU Analog Front End

YAMAHA

YTD427 APPLICATION MANUAL
CATALOG No. : LSI-6TD427A2
1997.12

b

IMPORTANT NOTICE

1. **Yamaha reserves the right to make changes to its Products and to this document without notice. The information contained in this document has been carefully checked and is believed to be reliable. However, Yamaha assumes no responsibilities for inaccuracies and makes no commitment to update or to keep current the information contained in this document.**

2. **These Yamaha Products are designed only for commercial and normal industrial applications, and are not suitable for other uses, such as medical life support equipment, nuclear facilities, critical care equipment or any other application the failure of which could lead to death, personal injury or environmental or property damage. Use of the Products in any such application is at the customer's sole risk and expense.**

3. **Yamaha assumes no liability for incidental, consequential or special damages or injury that may result from misapplication or improper use or operation of the Products.**

4. **Yamaha makes no warranty or representation that the Products are subject to intellectual property license from Yamaha or any third party, and Yamaha makes no warranty or representation of non-infringement with respect to the Products. Yamaha specifically excludes any liability to the Customer or any third party arising from or related to the Products' infringement of any third party's intellectual property rights, including the patent, copyright, trademark or trade secret rights of any third party.**

5. **Examples of use described herein are merely to indicate the characteristics and performance of Yamaha products. Yamaha assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein. Yamaha makes no warranty with respect to the products, express or implied, including, but not limited to the warranties of merchantability, fitness for a particular use and title.**

Contents

Chapter 1

INTRODUCTION

1.1 General Description

YTD427 is a communication LSI which provides the ISDN subscriber interface (two-wire metallic time compression multiplexing operation). It is capable of providing the electric characteristics conforming to TTC Standard JT-G961.

A DSU (Digital Service Unit) can easily be constructed by combining with YTD426B.

1.2 Features

1. Automatic Gain Control (AGC) function
2. Filter function
3. Peak hold function
4. ADC (Analog Digital Converter) function
5. Low Power Consumption
   Operation mode 72mW(typ.)
6. CMOS technology
7. 64-pin QFP
8. Single +5 volt supply

Chapter 2

BLOCK DIAGRAM

YTD 427 internal block diagram is shown in Figure2.1.

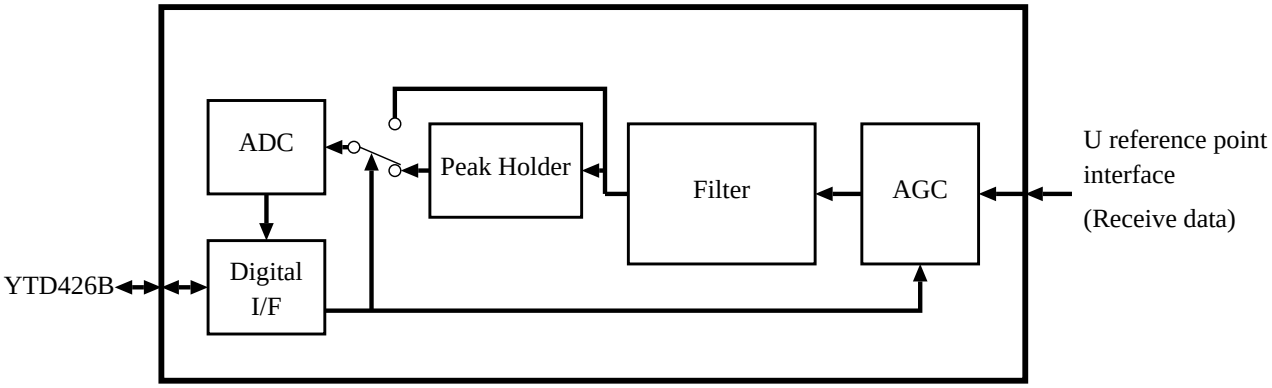


Figure 2.1: Internal Block Diagram

Chapter 3

PIN DESCRIPTIONS

3.1 Pin Assignments

The pin assignments of YTD427 are shown in Figure 3.1.

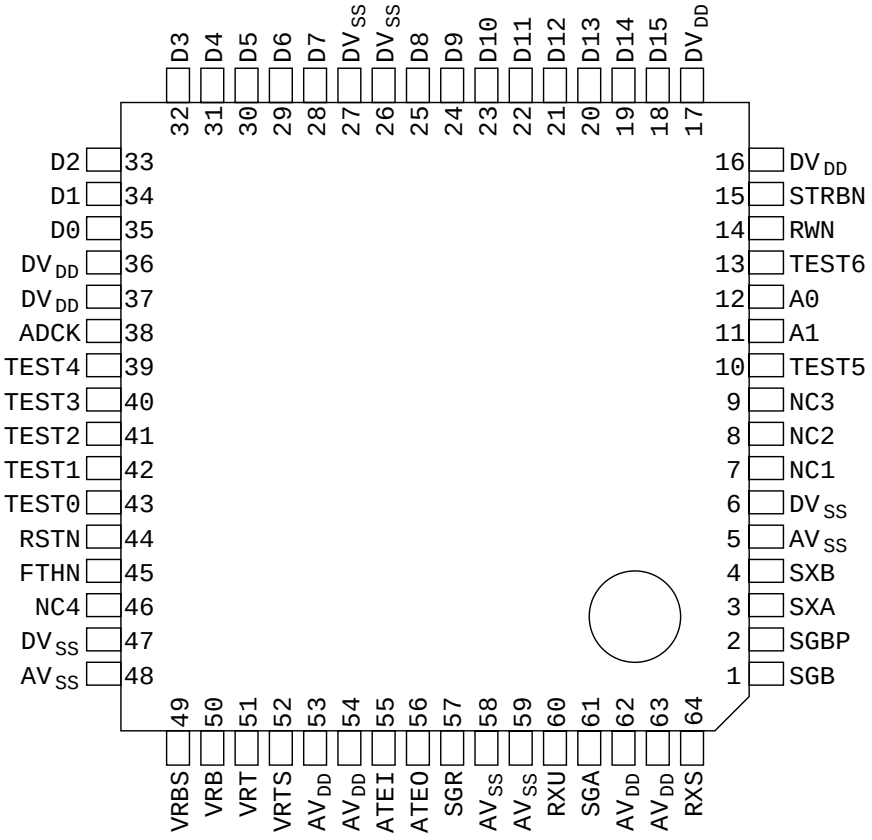


Figure 3.1: YTD427-F (64-pin QFP) Pin Assignments [Top View]

3.2 Pin Functions

Pin No.	Pin Name	I/O	Function	Remarks
1	SGB	–	Connect a 0.015μF capacitor across the SGB and SGR pins.	
2	SGBP	–	Connect a 0.015μF capacitor across the SGBP and SGR pins.	
3	SXA	–	Connected to SXB.	
4	SXB	–	Connected to SXA.	
5, 48, 58, 59	AV_{SS}	GND	Analog ground	All pins must be joined together.
6, 26, 27, 47	DV_{SS}	GND	Digital ground	All pins must be joined together.
7	NC1	IN	Unused Connected to DV_{SS}	
8	NC2	IN	Unused Connected to DV_{SS}	
9	NC3	IN	Unused Connected to DV_{SS}	
10	TEST5	IN	Test input 5 Connected to DV_{SS}	
11	A1	IN	Address bus bit 1 Connected to ADDRES1 of YTD426B	
12	A0	IN	Address bus bit 0 Connected to ADDRES0 of YTD426B	
13	TEST6	IN	Test input 6 Connected to DV_{SS}	
14	RWN	IN	Read/write signal “H” : Read “L” : Write Connected to RWN of YTD426B	
15	STRBN	IN	Strobe signal “H” : Inactive “L” : Active Connected to STRBN of YTD426B	
16, 17, 36, 37	DV_{DD}	PWR	Digital power supply	All pins must be joined together.

Pin No.	Pin Name	I/O	Function	Remarks
18	D15	OUT	Data bus bit 15 Connected to AFEDATA15 of YTD426B.	
19	D14	OUT	Data bus bit 14 Connected to AFEDATA14 of YTD426B.	
20	D13	OUT	Data bus bit 13 Connected to AFEDATA13 of YTD426B.	
21	D12	OUT	Data bus bit 12 Connected to AFEDATA12 of YTD426B.	
22	D11	OUT	Data bus bit 11 Connected to AFEDATA11 of YTD426B.	
23	D10	OUT	Data bus bit 10 Connected to AFEDATA10 of YTD426B.	
24	D9	OUT	Data bus bit 9 Connected to AFEDATA9 of YTD426B.	
25	D8	OUT	Data bus bit 8 Connected to AFEDATA8 of YTD426B.	
28	D7	IN	Data bus bit 7 Connected to AFEDATA7 of YTD426B.	
29	D6	IN	Data bus bit 6 Connected to AFEDATA6 of YTD426B.	
30	D5	IN	Data bus bit 5 Connected to AFEDATA5 of YTD426B.	
31	D4	IN	Data bus bit 4 Connected to AFEDATA4 of YTD426B.	
32	D3	IN	Data bus bit 3 Connected to AFEDATA3 of YTD426B.	
33	D2	IN	Data bus bit 2 Connected to AFEDATA2 of YTD426B.	
34	D1	IN	Data bus bit 1 Connected to AFEDATA1 of YTD426B.	
35	D0	IN	Data bus bit 0 Connected to AFEDATA0 of YTD426B.	

Pin No.	Pin Name	I/O	Function	Remarks
38	ADCK	IN	ADC operation clock signal Connected to CLK640K of YTD426B.	
39	TEST4	IN	Test input 4 Connected to DV_{SS}.	
40	TEST3N	I/O	Test input 3 Usually fixed to "H".	
41	TEST2	IN	Test input 2 Connected to DV_{SS}.	
42	TEST1	IN	Test input 1 Connected to DV_{SS}.	
43	TEST0	IN	Test input 0 Connected to DV_{SS}.	
44	RSTN	IN	Reset input pin "L" : Reset Reset time is 2μs(minimum)	
45	FTHN	IN	Test input Usually fixed to "H".	
46	NC4	IN	Unused Connected to DV_{SS}.	
49	VRBS	OUT	ADC reference power supply output (low voltage)	
50	VRB	IN	ADC reference power supply input (low voltage)	
51	VRT	IN	ADC reference power supply input (high voltage)	
52	VRTS	OUT	ADC reference power supply output (high voltage)	
53, 54, 62, 63	AV_{DD}	PWR	Analog power supply	All pins must be joined together.
55	ATEI	IN	Test signal input Connected to AV_{SS}.	
56	ATEO	I/O	Test signal input, output Connected to AV_{SS}.	
57	SGR	OUT	Analog signal reference output	
60	RXU	IN	Receive signal input	
61	SGA	–	Connect a 0.0047μF capacitor across SGA and SGR.	
64	RXS	–	Connect a 0.0022μF capacitor across RXS and SGR.	

Chapter 4

FUNCTIONS

Receive Interface Receive pin RXU has a high input impedance. An example of a reference circuit of the receive interface is shown in Figure 4.1.

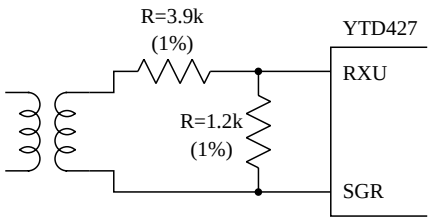


Figure 4.1: Receive Interface Connection

AGC The AGC section adjusts the gain in 0.22 dB step in the range from 0.0 to 56.1 dB at the receive signal center frequency (f=160 kHz) and amplifies the receive signal amplitude to the maximum dynamic range.

Filter The filter section is to prevent the ADC and the peak hold section from erroneous operation caused by high-frequency noise.

Peak Hold section Peak hold is performed during the initial training so that the gain of the AGC section is set to make best communication condition.

ADC The ADC section makes an A/D conversion of the received signal and transfers it to YTD426B. The A/D conversion timing is synchronized to the clock (ADCK) provided by YTD426B.

Digital Interface The digital section provides the interface to YTD426B.

Chapter 5

ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

(DV_{SS}=AV_{SS}=0.0V T_a=25 ℃)

Parameters	Symbol	Min.	Max.	Units
Supply Voltage (Digital)	DV_{DD}	−0.3	+7.0	V
Supply Voltage (Analog)	AV_{DD}	−0.3	+7.0	V
Input Voltage (Digital)	DV_{IN}	DV_{SS} − 0.3	DV_{DD}+0.3	V
Input Voltage (Analog)	AV_{IN}	AV_{SS} − 0.3	AV_{DD}+0.3	V
Output Voltage (Digital)	DV_{OUT}	DV_{SS} − 0.3	DV_{DD}+0.3	V
Output Voltage (Analog)	AV_{OUT}	AV_{SS} − 0.3	AV_{DD}+0.3	V
Power Dissipation	P_D		400	mW
Operating Temperature	T_{OP}	−20	+70	℃
Storage Temperature	T_{ST}	−55	+125	℃

Note 1 The values represent the minimum and maximum voltages that can be applied to the pins without causing damage. It does not guarantee the operation. Applying a voltage exceeding the absolute maximum ratings may cause permanent damage to YTD427.

Note 2 Use digital power supply DV_{DD} and analog power supply AV_{DD} under the condition: DV_{DD} = AV_{DD}. Also, insert a C ≥ 0.1μF across DV_{DD} and DV_{SS} and across AV_{DD} and AV_{SS} to prevent latch up.

Note 3 Use digital ground DV_{SS} and analog ground AV_{SS} under the condition: DV_{SS} = AV_{SS}.

Note 4 Even though digital power supply DV_{DD} and analog power supply AV_{DD} have the same pin name, they are not connected inside YTD427. Make sure to connect the pins that have the same name.

Note 5 Even though digital ground DV_{SS} and analog ground AV_{SS} have the same pin name, they are not connected inside YTD427. Make sure to connect the pins that have the same name.

5.2 Recommended Operating Conditions

(DV_{SS}=AV_{SS}=0.0V、T_a=25 ℃)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
Digital Power Supply Voltage	DV_{DD}		4.75	5.0	5.25	V
Analog Power Supply Voltage	AV_{DD}		4.75	5.0	5.25	V
Digital Input Voltage	DV_{IN}		DV_{SS}		DV_{DD}	V
Analog Input Voltage	AV_{IN}		AV_{SS}		AV_{DD}	V
Digital Output Voltage	DV_{IN}		DV_{SS}		DV_{DD}	V
Analog Output Voltage	AV_{IN}		AV_{SS}		AV_{DD}	V
Operating Temperature Range	T_{OP}		−20	25	70	℃
External Clock Input						
Clock Frequency	f_{CP}	**(Note1)**		0.64		MHz
Clock Frequency Allowable Deviation	Δf_{CP}	**(Note1)**	−50		50	ppm
Clock Duty	t_{DUTY}	**(Note1)**	45	50	55	%
High Level Time	t_{WCH}	**(Note1)**	400			ns
Low Level Time	t_{WCL}	**(Note1)**	400			ns
Rise Time	t_{TLHC}	**(Note1)**			20	ns
Fall Time	t_{THLC}	**(Note1)**			20	ns
YTD426 Supply Input Signal						
High-Level Pulse Width	t_{WDH}	**(Note2)**	90			ns
Low-Level Pulse Width	t_{WDL}	**(Note2)**	90			ns
Rise Time	t_{TLHD}	**(Note2)**			10	ns
Fall Time	t_{THLD}	**(Note2)**			10	ns

Note 1 With respect to ADCK pin.

Note 2 With respect to A1, A0, RWN, STRBN, D15 to D0 pins.

5.3 DC Characteristics

(DV_{DD}=AV_{DD}=4.75～5.25V, DV_{SS}=AV_{SS}=0.0V, T_a=25 ℃)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage (CMOS)	V_{IHC}	**(Note1)**	$0.7DV_{DD}$		DV_{DD}	V
Low-Level Input Voltage (CMOS)	V_{ILC}	**(Note1)**	0.0		$0.3DV_{DD}$	V
Input Leak Current (CMOS)	I_{LIC}	**(Note1)** **(Note2)**			±10	μA
High-Level Input Voltage (TTL)	V_{IHT}	**(Note3)**	2.0		DV_{DD}	V
Low-Level Input Voltage (TTL)	V_{ILT}	**(Note3)**	0.0		0.8	V
Input Leak Current (TTL)	I_{LIT}	**(Note3)** **(Note4)**			±10	μA
High-Level Output Voltage (TTL)	V_{OHT}	**(Note3)** **(Note5)**	4.4			V
Low-Level Output Voltage (TTL)	V_{OLT}	**(Note3)** **(Note6)**			0.4	V
Supply Current (Normal)	I_{DD1}	**(Note7)**		14.4	24.9	mA
Supply Current (at reset)	I_{DD4}	**(Note7)** **(Note8)**		4.4	7.6	mA
Power Consumption (Normal)	P_{tot1}	**(Note7)**		72	131	mW
Power Consumption (at reset)	P_{tot4}	**(Note7)** **(Note8)**		22	40	mW

Note1 With respect to ADCK, TEST4, TEST2 to TEST0, RSTN, FTHN, NC4 to NC1 pins.

Note2 V_{IC}=DV_{SS} - DV_{DD}

Note3 With respect to A1, A0, RWN, STRBN, D15 to D0, TEST3, TEST5, TEST6 pins.

Note4 V_{IT}=DV_{SS} - DV_{DD}

Note5 I_{OH}=−4mA

Note6 I_{OL}=12mA

Note7 Neither external circuit nor parts

Note8 ADCK pin fixed to DV_{SS}

(DV_{DD}=AV_{DD}=4.75～5.25V, DV_{SS}=AV_{SS}=0.0V, T_a=25 ℃)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
Analog Output Allowable Load Impedance	Z_O	**(Note1)**	30			kΩ
Analog Receive Buffer Input Impedance	Z_{i1}	**(Note2)**	10			MΩ
Analog Receive Buffer Input Impedance	Z_{i2}	**(Note3)**		100		kΩ
Reference Resistance	R_{REF}	**(Note4)**	1.92	2.40	3.84	kΩ
Voltage Divider Resistance	R_{DIV}	**(Note5)**	1.44	1.80	2.88	kΩ
Analog Signal Reference Voltage	V_{SG}	**(Note6)**	$0.5AV_{DD}$-0.05	$0.5AV_{DD}$	$0.5AV_{DD}$+0.05	V
ADC						
High-Level Reference Voltage Level	V_{RT}	**(Note7)**	$0.7AV_{DD}$		AV_{DD}	V
Low-Level Reference Voltage Level	V_{RB}	**(Note8)**	0.0		$0.3AV_{DD}$	V
Self-Bias VRT	V_{RTS}	**(Note9)**	$0.7AV_{DD}$-0.1	$0.7AV_{DD}$	$0.7AV_{DD}$+0.1	V
Self-Bias VRB	V_{RBS}	**(Note10)**	$0.3AV_{DD}$-0.1	$0.3AV_{DD}$	$0.3AV_{DD}$+0.1	V

Note1 With respect to SGR, SXA pins.

Note2 With respect to RXU pin.

Note3 With respect to SXB pin.

Note4 Across VRT and VRB pins. VRB=1.5 V

Note5 Across VRT and AV_{DD} pins and across VRB and AV_{SS} pins.

Note6 SGR pin is open.

Note7 With respect to VRT pin.

Note8 With respect to VRB pin.

Note9 Short VRT pin and VRTS pin

Note10 Short VRB pin and VRBS pin

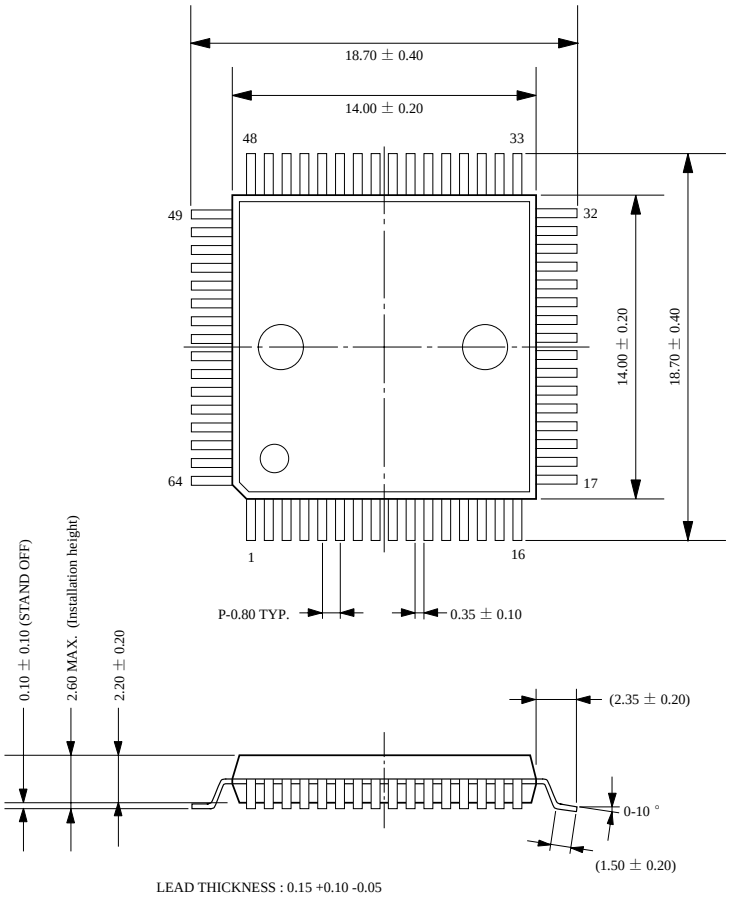
5.4 AC Characteristics

(DV_{DD}=AV_{DD}=4.75～5.25V, DV_{SS}=AV_{SS}=0.0V, T_a=25 ℃)

Parameters		Symbol	Condition	Min.	Typ.	Max.	Units
Total Harmonic Distortion		THD				1.0	%
AGC	Gain	G_A		43.76	45.76	47.76	dB
	Noise	N_{oag}				6	mV_{rms}
	DC Offset Voltage	V_{agoff}				±50	mV
Filter	Cut Off Frequency	f_c		213	320	427	kHz
	Flatness	A_p		−1.0	0.0	1.0	dB
PH	Max. Conversion Time	F_{PH}			160	200	kHz
	Refresh Time	t_{phr}			60	100	ns
	Peak Hold Error	V_{phe}				±50	mV
ADC	Resolution	R_{es}				8	Bit
	Linearity Error	EL			±1.0	±2.0	LSB
	Quantization Error	E_e		−1.0		1.0	LSB
	Max. Conversion Time	F_{AD}				1.28	MSPS
	Clock Frequency	F_{ADCK}			640		kHz

Chapter 6

PACKAGE OUTLINE



(UNIT) : mm (millimeters)

The shape of the molded corner may be slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.

Note : The LSIs for surface mount need special consideration on storage and soldering conditions. For detailed information, please contact your nearest Yamaha agent.

Appendix A

EXMAPLE OF APPLICATIONS

A.1 Example of Application Circuits

An example of an application circuit using YTD427 is shown in Figure A.1.

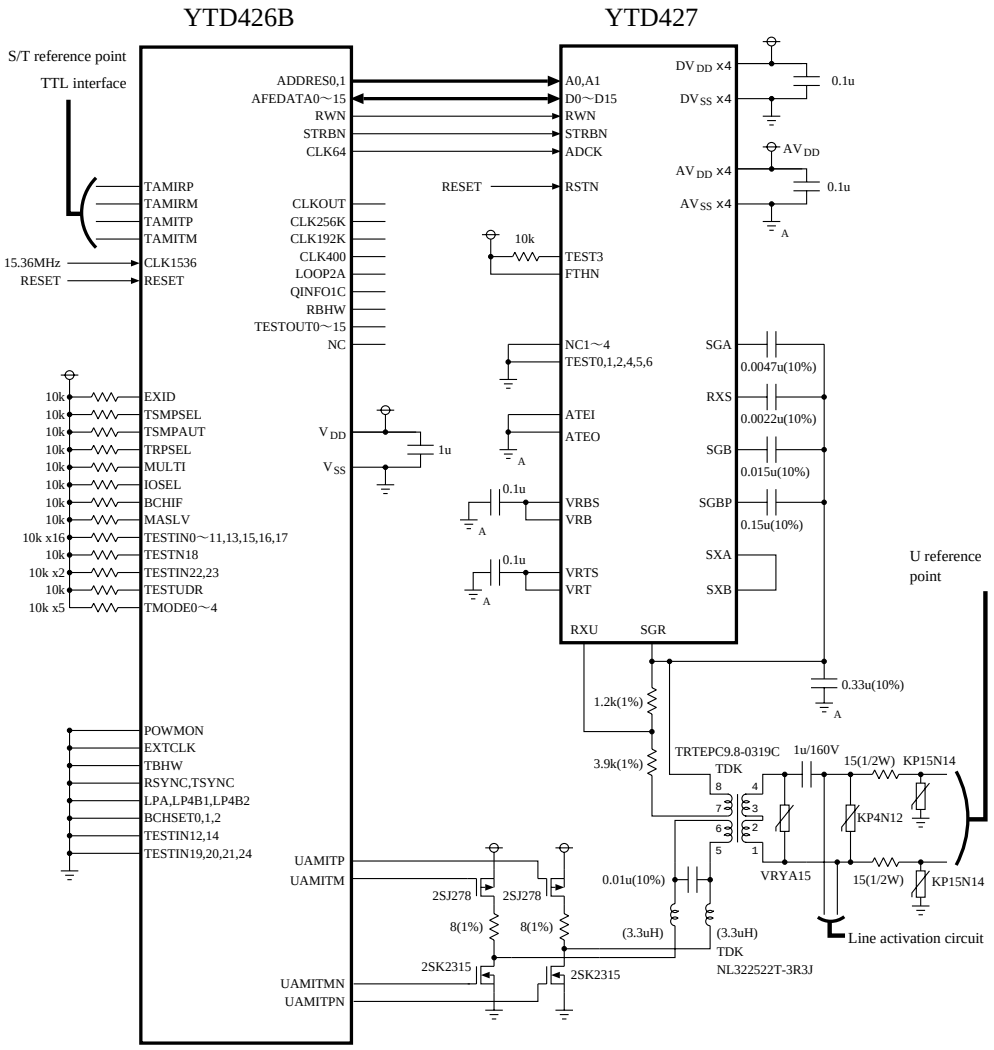


Figure A.1: Pin Connection Example