

## General Description

The AON6442 uses trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $C_{RSS}$ . In addition, switching behavior is well controlled with a "Schottky style" soft recovery body diode.

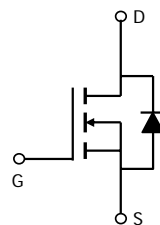
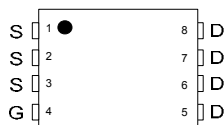
## Product Summary

$V_{DS}$	40V
$I_D$ (at $V_{GS}=10V$ )	32A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 4.8m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	< 7m $\Omega$

100% UIS Tested  
100%  $R_g$  Tested



Top View



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	$V_{DS}$	40	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	A	
		$T_C=100^\circ\text{C}$		
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	168		
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	A	
		$T_A=70^\circ\text{C}$		
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	40	A	
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}, E_{AR}$	80	mJ	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	W	
		$T_C=100^\circ\text{C}$		
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	W	
		$T_A=70^\circ\text{C}$		
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
<b>Thermal Characteristics</b>				
Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	55	
Maximum Junction-to-Case	$R_{\theta JC}$	2.6	3.5	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.4	1.9	2.4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	168			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		4 6.2	4.8 7.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A		5.5	7	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		67		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				32	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, f=1MHz	1460	1830	2200	pF
C <sub>oss</sub>	Output Capacitance		365	521	680	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		20	43	73	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.4	0.8	1.2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A	22	27.8	35	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge		10	12.8	15	nC
Q <sub>gs</sub>	Gate Source Charge		3	3.9	5	nC
Q <sub>gd</sub>	Gate Drain Charge		2	6	10	nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω		7.2		ns
t <sub>r</sub>	Turn-On Rise Time			3		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			23		ns
t <sub>f</sub>	Turn-Off Fall Time			3.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	11	16.5	21	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	28	40	52	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

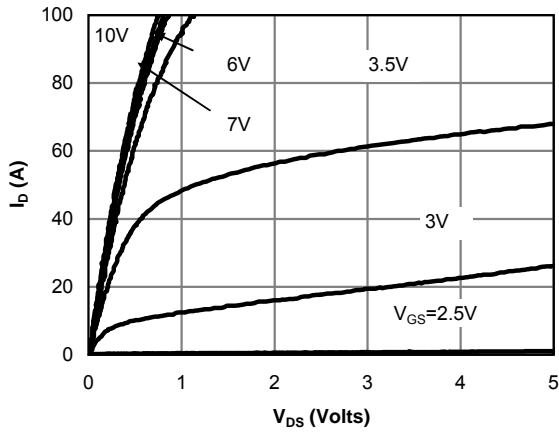


Figure 1: On-Region Characteristics (Note E)

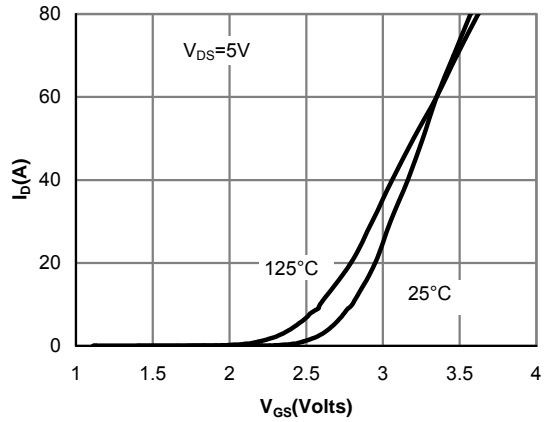


Figure 2: Transfer Characteristics (Note E)

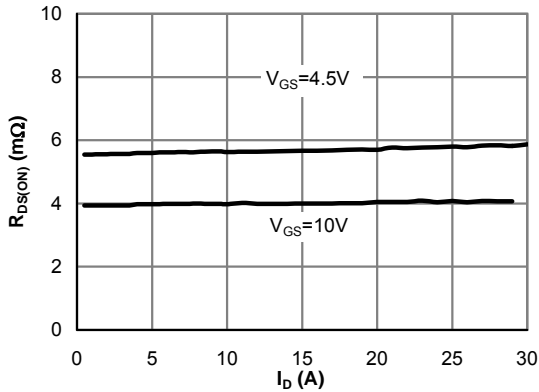


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

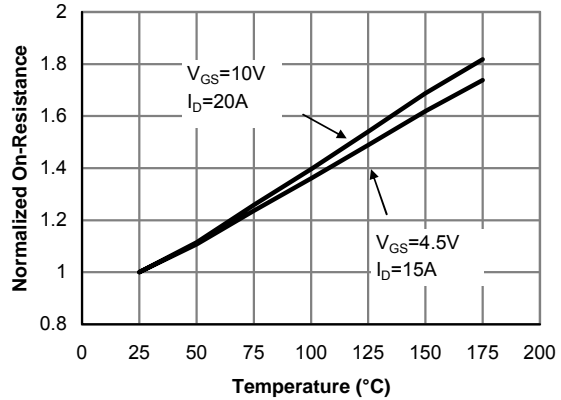


Figure 4: On-Resistance vs. Junction Temperature (Note E)

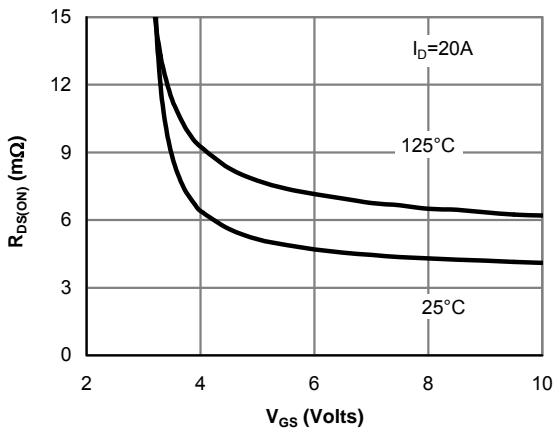


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

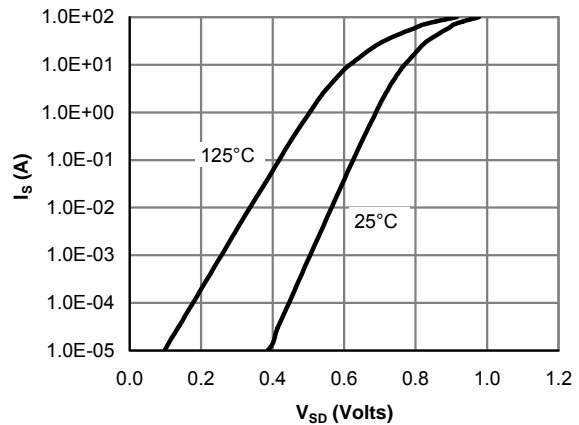


Figure 6: Body-Diode Characteristics (Note E)

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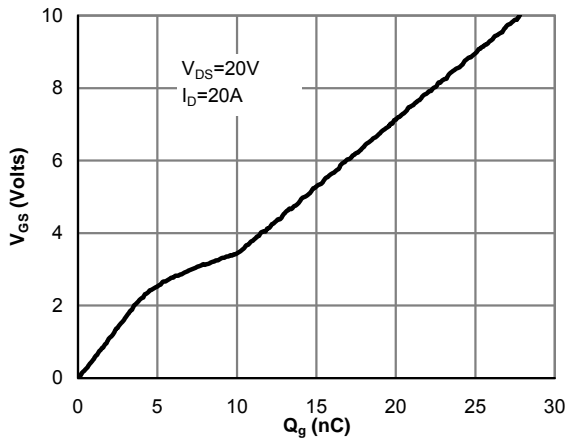


Figure 7: Gate-Charge Characteristics

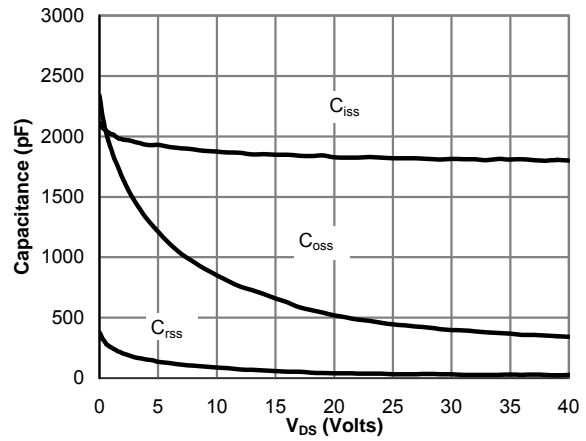


Figure 8: Capacitance Characteristics

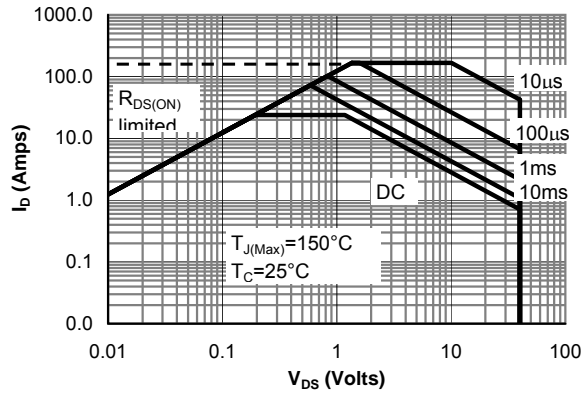


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

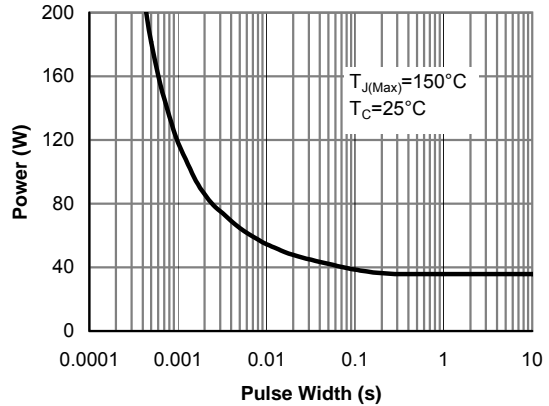


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

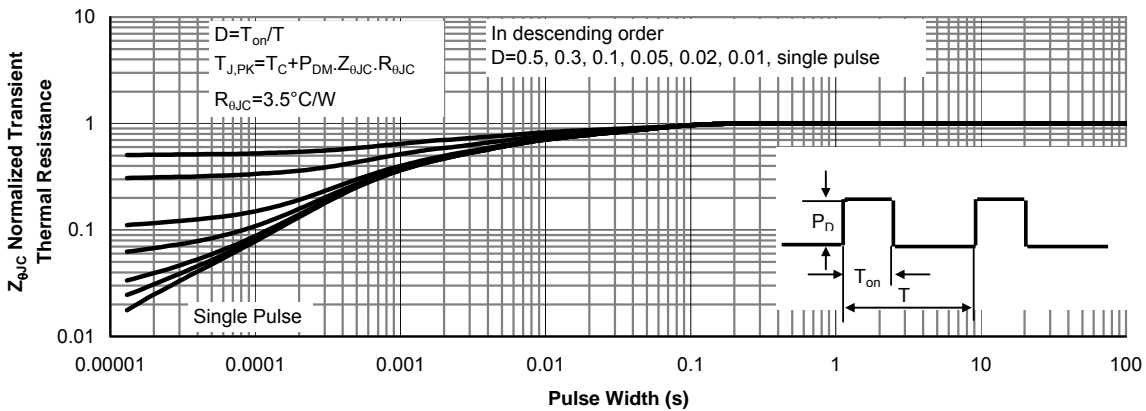


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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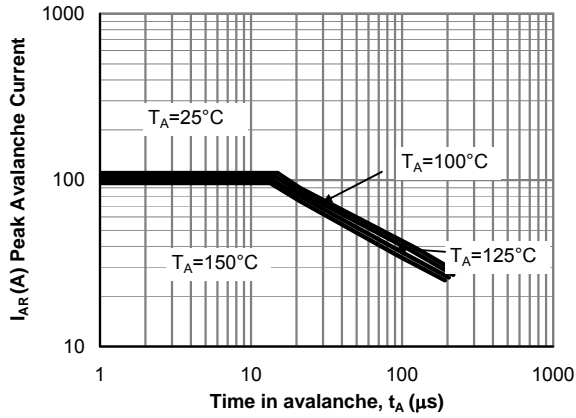


Figure 12: Single Pulse Avalanche capability (Note C)

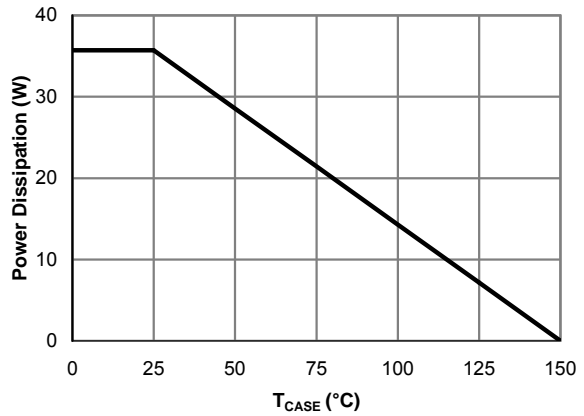


Figure 13: Power De-rating (Note F)

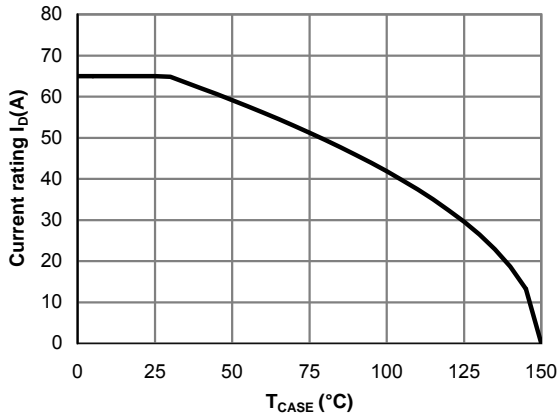


Figure 14: Current De-rating (Note F)

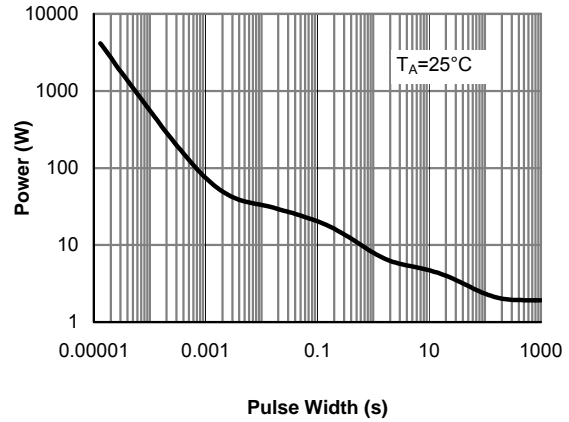


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

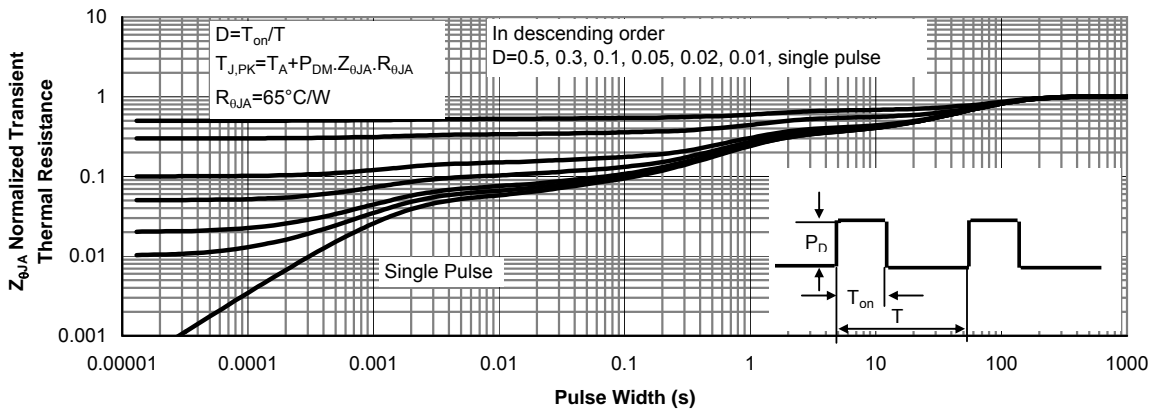
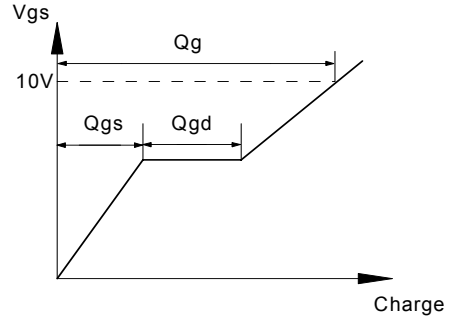
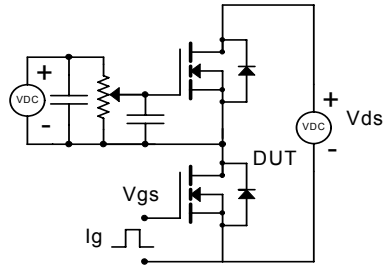
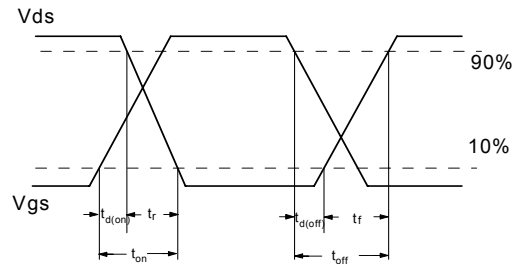
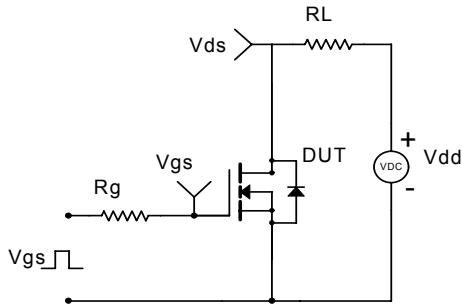


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

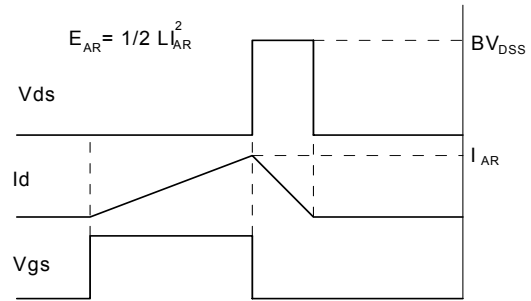
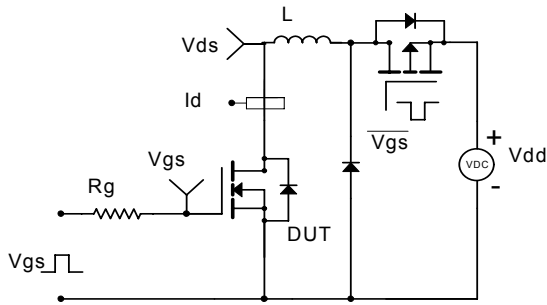
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

