

# PRELIMINARY

# OKI Semiconductor

REVISION-2 1996.11.2

## MSM54V16255A/SL

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

### DESCRIPTION

The MSM54V16255A/SL is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM54V16255A/SL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM54V16255A/SL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.

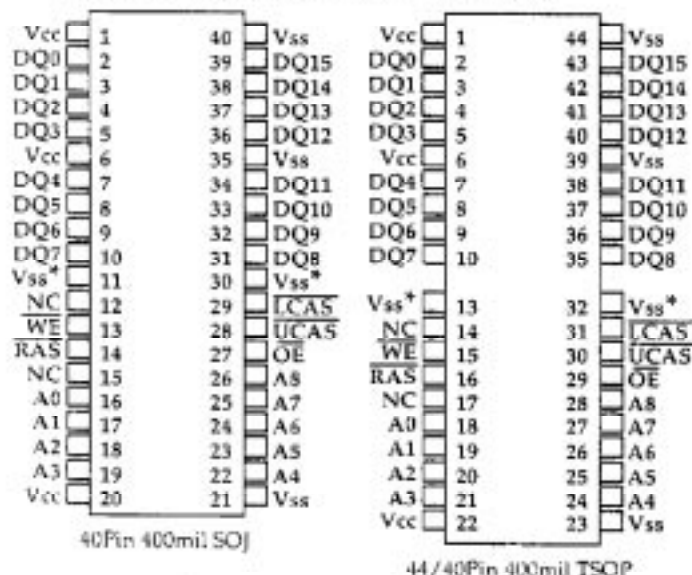
### FEATURES

- 262,144-word X 16-bit configuration
  - Single 3.3V power supply,  $\pm 0.3V$  tolerance
  - Input : LVTTTL compatible, low input capacitance
  - Output : LVTTTL compatible, 3-state
  - Refresh : 512 cycles/8ms
  - Fast page mode, read modify write capability
  - Byte wide control: 2  $\overline{CAS}$  control
  - $\overline{CAS}$  before  $\overline{RAS}$  refresh, Hidden refresh,  $\overline{RAS}$  only refresh capability
  - $\overline{CAS}$  before  $\overline{RAS}$  self-refresh capability (SL version)
  - Package options:
    - 40-Pin 400 mil plastic SOJ (SOJ40-P-400) (Product : MSM54V16255A/SL-xxJ5)
    - 44/40-Pin 400 mil plastic TSOP (TSOP44/40-P-400/0.8-K) (Product : MSM54V16255A/SL-xxTS-K)
- xx indicates speed rank.

### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t <sub>TRAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>	t <sub>RC</sub>	t <sub>PC</sub>	
MSM54V16255A/SL-40	40ns	22ns	10ns	10ns	80ns	25ns	504mW
MSM54V16255A/SL-45	45ns	24ns	12ns	12ns	90ns	27ns	450mW

### PIN CONFIGURATION ( TOP VIEW )

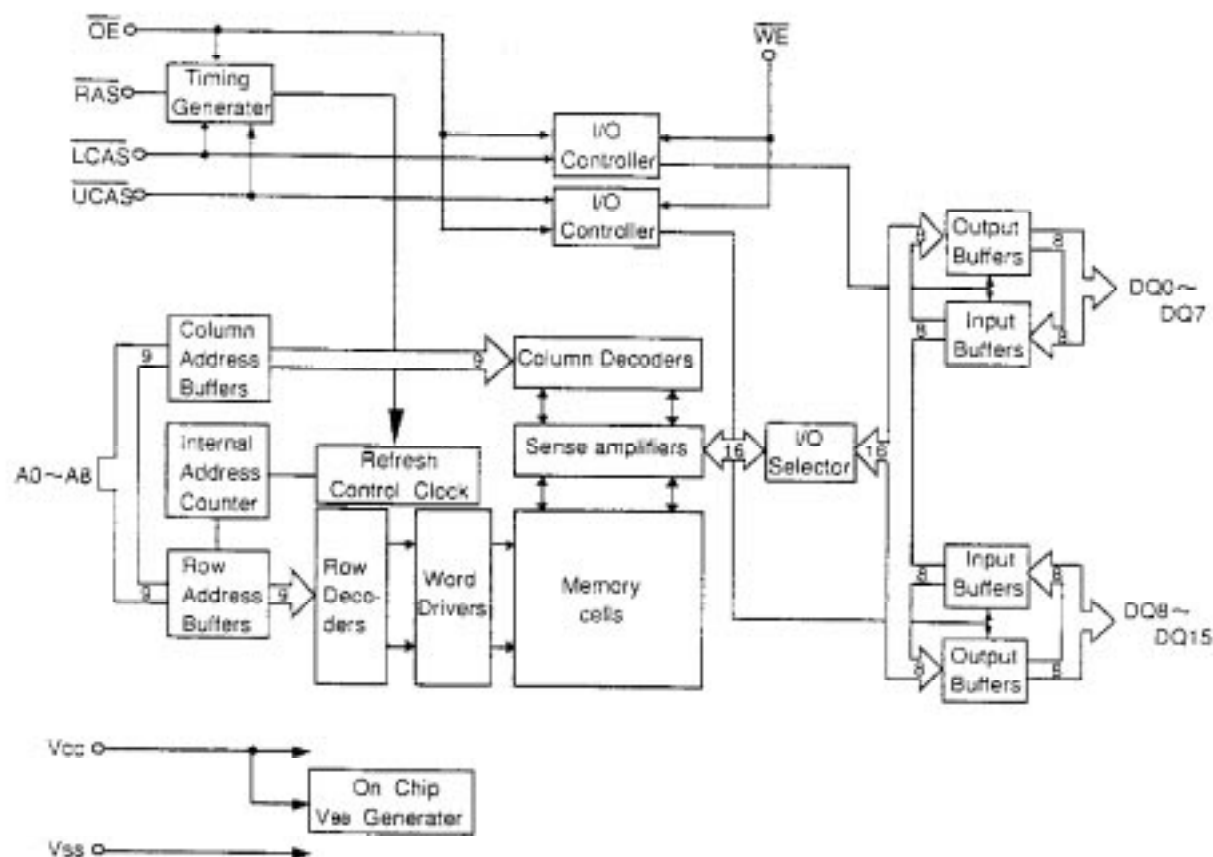


Pin Names	Function
A0-A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$ , $\overline{UCAS}$	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply ( 3.3V )
Vss	Ground ( 0V )
NC	No Connection
Vss*	Ground ( 0V ) : see Note2

Note1 :  
The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must be provided to every Vss pin.

Note2 :  
For improved signal integrity, it is recommended to connect the Vss\* pins, pin 11 and 31(SOJ) or pin 13 and 32(TSOP) to GND : the pins are electrically connected to internal GND.

## BLOCK DIAGRAM



## FUNCTION TABLE

Input Pin					DQPin		Functional Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	$DQ0 \sim DQ7$	$DQ8 \sim DQ15$	
H	.	.	.	.	High-Z	High-Z	Standby
L	H	H	.	.	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	Dout	Upper Byte Read
L	L	L	H	L	Dout	Dout	Word Read
L	L	H	L	H	Din	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	Din	Upper Byte Write
L	L	L	L	H	Din	Din	Word Write
L	L	L	H	H	High-Z	High-Z	—

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	V <sub>I</sub>	T <sub>a</sub> =25°C	-0.5~+4.6	V
Short circuit output current	I <sub>OS</sub>	T <sub>a</sub> =25°C	50	mA
Power dissipation	P <sub>D</sub>	T <sub>a</sub> =25°C	1	W
Operating temperature	T <sub>OP</sub>	—	0~+70	°C
Storage temperature	T <sub>STG</sub>	—	-55~+150	°C

### Recommended Operating Conditions

(T<sub>a</sub>=0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	—	3.0	3.3	3.6	V
	V <sub>SS</sub>	—	0	0	0	V
Input high voltage	V <sub>IH</sub>	—	2.0	—	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	—	0.8	V

### Capacitance

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=25°C, f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0~A8)	C <sub>IN1</sub>	—	—	8	pf
Input capacitance (RAS, LCAS, UCAS, WE, OE)	C <sub>IN2</sub>	—	—	8	pf
Input / output capacitance (DQ0~DQ15)	C <sub>I/O</sub>	—	—	9	pf

## DC CHARACTERISTICS

(V<sub>CC</sub>=3.3V±0.3V, T<sub>a</sub>=0 to 70°C)

Parameter	Symbol	Condition	MSM54V16255A /SL-40		MSM54V16255A /SL-45		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0mA	0	0.4	0	0.4	V	
Input Leakage Current	I <sub>I</sub>	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10	10	-10	10	μA	
Output Leakage Current	I <sub>IO</sub>	DO <sub>i</sub> Disable 0V ≤ V <sub>O</sub> ≤ 3.6V	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I <sub>CC1</sub>	$\overline{RAS}, \overline{CAS}$ Cycling t <sub>RC</sub> =Min.	-	140	-	125	mA	1,2
Power Supply Current (Standby)	I <sub>CC2</sub>	$\overline{RAS}, \overline{CAS} = V_{IH}$	-	3	-	3	mA	1
Average Power Supply Current (RAS only Refresh)	I <sub>CC3</sub>	$\overline{RAS}$ =Cycling $\overline{CAS}=V_{IH}$ t <sub>RC</sub> =Min.	-	140	-	125	mA	1,2
Average Power Supply Current (Fast Page Mode)	I <sub>CC4</sub>	$\overline{RAS}=V_{IL}$ $\overline{CAS}$ Cycling t <sub>RC</sub> =Min.	-	140	-	125	mA	1,3
Average Power Supply Current (CAS Before RAS Refresh)	I <sub>CC5</sub>	$\overline{RAS}$ =Cycling $\overline{CAS}$ Before $\overline{RAS}$	-	140	-	125	mA	1,2
Average Power Supply Current (Battery Backup)	I <sub>CC6</sub>	t <sub>RC</sub> = 125 μs $\overline{CAS}$ Before $\overline{RAS}$ t <sub>RAS</sub> ≤ 1 μs	-	300	-	300	μA	1,2,4,5
Average Power Supply Current (CAS Before RAS Self-refresh)	I <sub>CC7</sub>	$\overline{RAS} \leq 0.2V$ $\overline{CAS} \leq 0.2V$	-	200	-	200	μA	1,2,4,5

- Notes : 1. I<sub>CC</sub> Max. is specified as I<sub>CC</sub> for the output open condition.  
 2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .  
 3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .  
 4. V<sub>CC</sub> - 0.2V ≤ V<sub>IH</sub> ≤ 6.5V, -1.0V ≤ V<sub>IL</sub> ≤ 0.2V.  
 5. SL version.

## AC CHARACTERISTICS (1/2)

(V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>a</sub> = 0~70°C)

Parameter	Symbol	MSM54V16255A /SI-40		MSM54V16255A /SI-45		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t <sub>RC</sub>	80	—	90	—	ns	
Read/Write cycle time	t <sub>RMW</sub>	115	—	130	—	ns	
Hyper page mode cycle time	t <sub>PC</sub>	25	—	27	—	ns	
Fast page mode read/write cycle time	t <sub>PRMW</sub>	55	—	60	—	ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	40	—	45	ns	7,12,13
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	10	—	12	ns	7,12
Access time from column address	t <sub>AA</sub>	—	22	—	24	ns	7,13
Access time from $\overline{\text{OE}}$	t <sub>OA</sub>	—	10	—	12	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>	—	24	—	26	ns	7,12
Output buffer turn-off delay time	t <sub>OFF</sub>	3	8	3	8	ns	8
$\overline{\text{OE}}$ to data output buffer turn-off delay time	t <sub>OEZ</sub>	3	8	3	8	ns	8
Transition time	t <sub>r</sub>	2	35	2	35	ns	
Refresh period	t <sub>REF</sub>	—	8	—	8	ms	
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	30	—	35	—	ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	40	10,000	45	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t <sub>RASP</sub>	40	100,000	45	100,000	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	8	—	10	—	ns	
$\overline{\text{RAS}}$ hold time reference to $\overline{\text{OE}}$	t <sub>RCH</sub>	8	—	8	—	ns	
$\overline{\text{CAS}}$ precharge time	t <sub>CP</sub>	8	—	8	—	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	10	10,000	12	10,000	ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCO</sub>	18	30	18	33	ns	12
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAO</sub>	13	18	13	21	ns	
Row address set-up time	t <sub>ASR</sub>	0	—	0	—	ns	13
Row address hold time	t <sub>RAH</sub>	8	—	8	—	ns	
Column address set-up time	t <sub>ASC</sub>	0	—	0	—	ns	
Column address hold time	t <sub>CAH</sub>	5	—	6	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t <sub>AR</sub>	30	—	30	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	22	—	24	—	ns	
Read command set-up time	t <sub>RCB</sub>	0	—	0	—	ns	9
Read command hold time	t <sub>RCH</sub>	0	—	0	—	ns	
Read command hold time reference to $\overline{\text{RAS}}$	t <sub>RWH</sub>	0	—	0	—	ns	9

## AC CHARACTERISTICS (2/2)

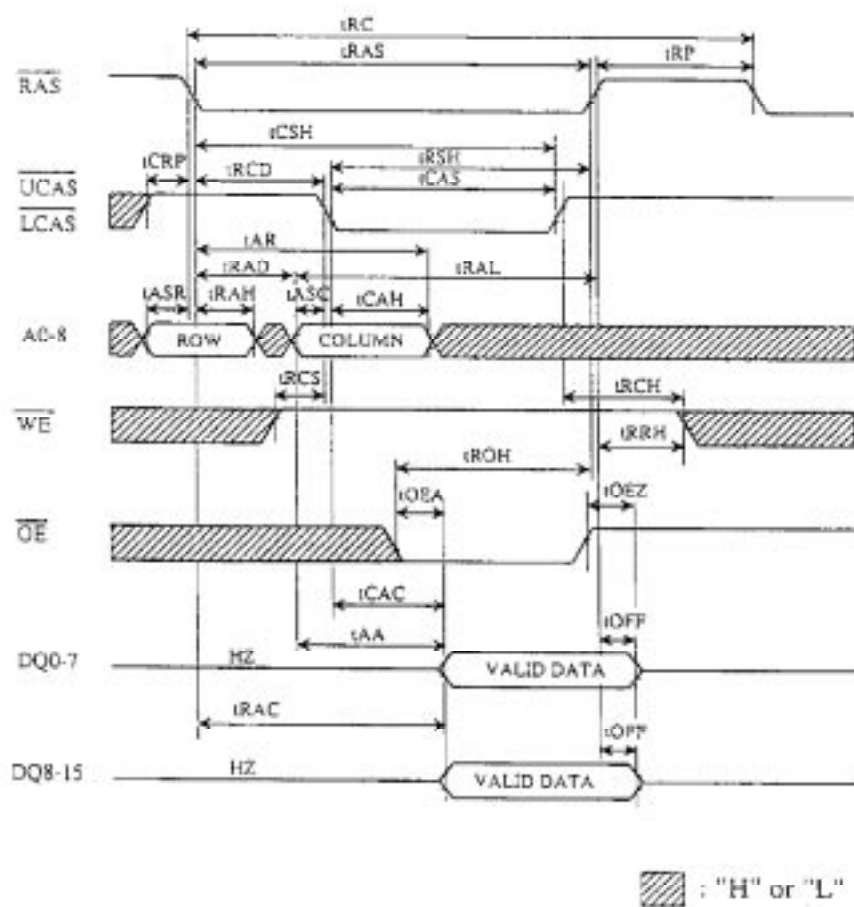
[V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>a</sub> = 0~70°C]

Parameter	Symbol	MSM54V16255A /SL-40		MSM54V16255A /SL-45		Unit	Note
		MIN	MAX	MIN	MAX		
Write command set-up time	t <sub>wcs</sub>	0	—	0	—	ns	
Write command hold time	t <sub>wch</sub>	7	—	8	—	ns	
Write command pulse width	t <sub>wp</sub>	7	—	8	—	ns	
Write command hold time from $\overline{\text{RAS}}$	t <sub>wcn</sub>	30	—	30	—	ns	
$\overline{\text{OE}}$ command hold time	t <sub>oeh</sub>	7	—	8	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t <sub>cwl</sub>	7	—	8	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t <sub>rwl</sub>	10	—	12	—	ns	
Data to $\overline{\text{CAS}}$ delay time	t <sub>ozc</sub>	0	—	0	—	ns	
Data to $\overline{\text{OE}}$ delay time	t <sub>ozo</sub>	0	—	0	—	ns	
Data-in set-up time	t <sub>os</sub>	0	—	0	—	ns	10
Data-in hold time	t <sub>oh</sub>	6	—	7	—	ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	t <sub>ohr</sub>	20	—	20	—	ns	
$\overline{\text{OE}}$ to Data-in delay time	t <sub>ozo</sub>	8	—	8	—	ns	
Hi-Z command pulse width	t <sub>oep</sub>	10	—	10	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t <sub>cwb</sub>	28	—	30	—	ns	11
Column address to $\overline{\text{WE}}$ delay time	t <sub>awb</sub>	38	—	40	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t <sub>rwb</sub>	60	—	65	—	ns	11
$\overline{\text{CAS}}$ active delay time from $\overline{\text{RAS}}$ precharge	t <sub>rpc</sub>	0	—	0	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ set-up time (CAS before $\overline{\text{RAS}}$ )	t <sub>csr</sub>	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time (CAS before $\overline{\text{RAS}}$ )	t <sub>chr</sub>	10	—	10	—	ns	
$\overline{\text{RAS}}$ Pulse Width (CAS before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>rass</sub>	100	—	100	—	ns	
$\overline{\text{RAS}}$ Precharge Time (CAS before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>rps</sub>	100	—	100	—	ns	
$\overline{\text{CAS}}$ Hold Time (CAS before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>chs</sub>	-40	—	-40	—	ns	

## Notes:

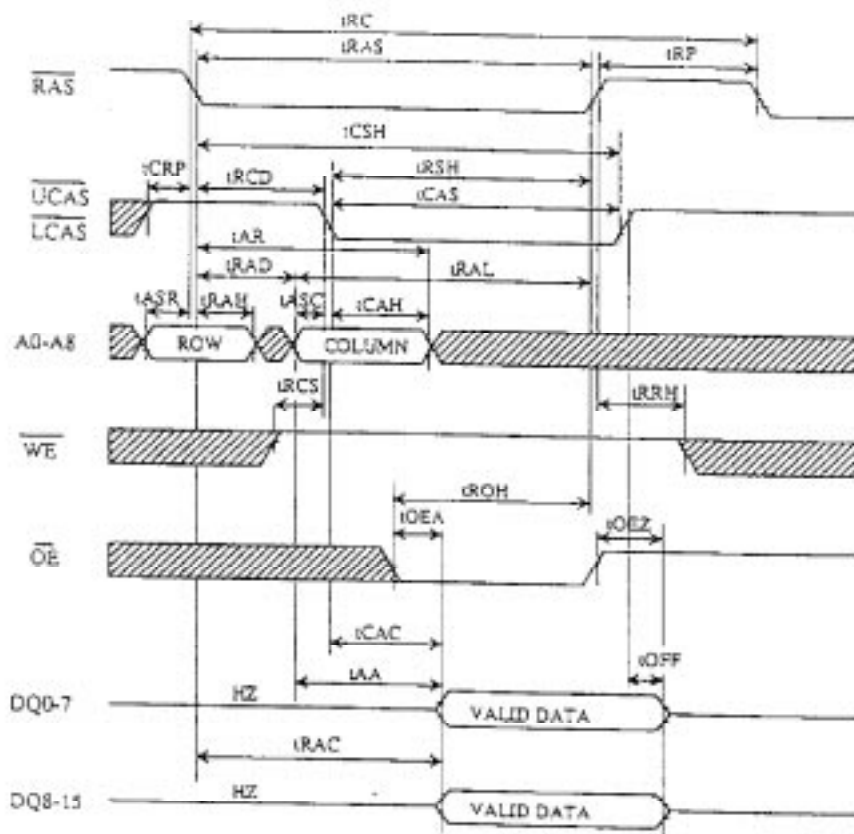
1. All voltages are referenced to  $V_{SS}$ .
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200  $\mu$ s is required after power-up, followed by any 8  $\overline{RAS}$  cycles. (Example:  $\overline{RAS}$ -only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  cycles instead of 8  $\overline{RAS}$  cycles are required.
5. The AC characteristics assume  $t_r=5$ ns.
6.  $V_{IH}$ (Min.) and  $V_{IL}$ (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
7. Data outputs are measured with a load of 50 pF. DOUT reference levels:  $V_{OH}/V_{OL}=2.0$  V/1.4V. Note that  $V_{OL}$  is defined as 1.4V when  $V_{SS}^*$  pins, pin 11 and pin 30, were open. The data output measurements under  $V_{OH}/V_{OL}=2.0$ V/0.8V are guaranteed when  $V_{SS}^*$  pins, pin 11 and 30(SO) or pin 13 and 32(TSOP) were connected to GND.
8.  $t_{OEZ}$ (Max.),  $t_{OH}$ (Max.),  $t_{WEZ}$ (Max.) and  $t_{OSZ}$ (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either  $t_{RCH}$  or  $t_{RHH}$  must be satisfied for a read cycle.
10. These parameters are referenced to  $\overline{CAS}$  leading edge of early write cycles and to  $\overline{WE}$  leading edge in  $\overline{OE}$ -controlled write cycles and read-modify-write cycles.
11.  $t_{WCS}$ ,  $t_{WOD}$ ,  $t_{WOW}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If  $t_{WOD} \geq t_{WOD}$ (Min.),  $t_{WOW} \geq t_{WOW}$ (Min.) and  $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indeterminate.
12. Operation within the  $t_{AC}$ (Max.) limit insures that  $t_{RAC}$ (Max.) can be met.  $t_{DC}$ (Max.) is specified as a reference point only. If  $t_{DC}$  is greater than the specified  $t_{AC}$ (Max.) limit, then access time is controlled by  $t_{DC}$ .
13. Operation within the  $t_{RAD}$ (Max.) limit ensures that  $t_{RAC}$ (Max.) can be met.  $t_{RAD}$ (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$ (Max.) limit, then access time is controlled by  $t_{AA}$ .
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while  $\overline{RAS}=V_{IL}$ .
16. Addresses (A0 - A8) may be changed once or less while  $\overline{CAS}=V_{IH}$  and  $\overline{RAS}=V_{IL}$ .
17. This is guaranteed by design. ( $t_{COH}=t_{CAC}$  - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

### READ CYCLE (RAS output control)



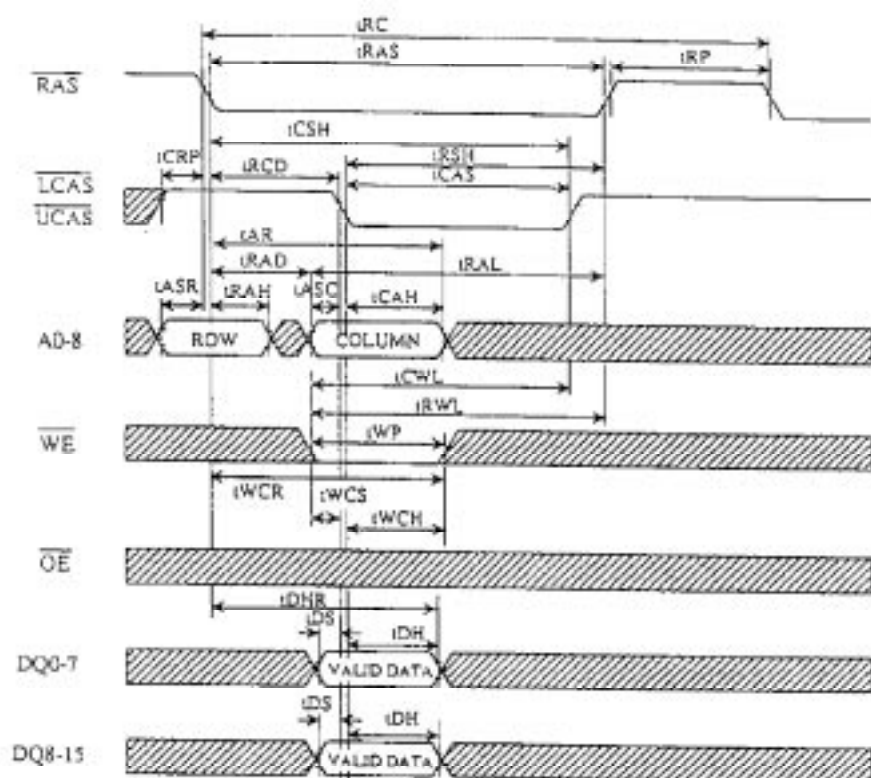


### READ CYCLE ( $\overline{\text{CAS}}$ output control)



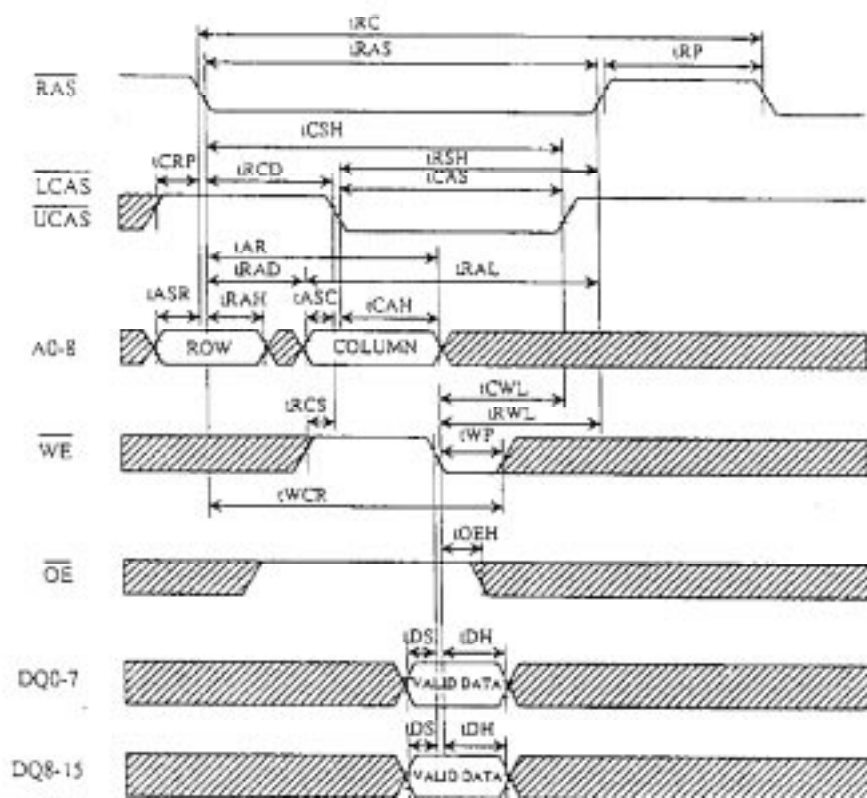
▨ : "H" or "L"

EARLY WRITE CYCLE (LCAS and UCAS active)



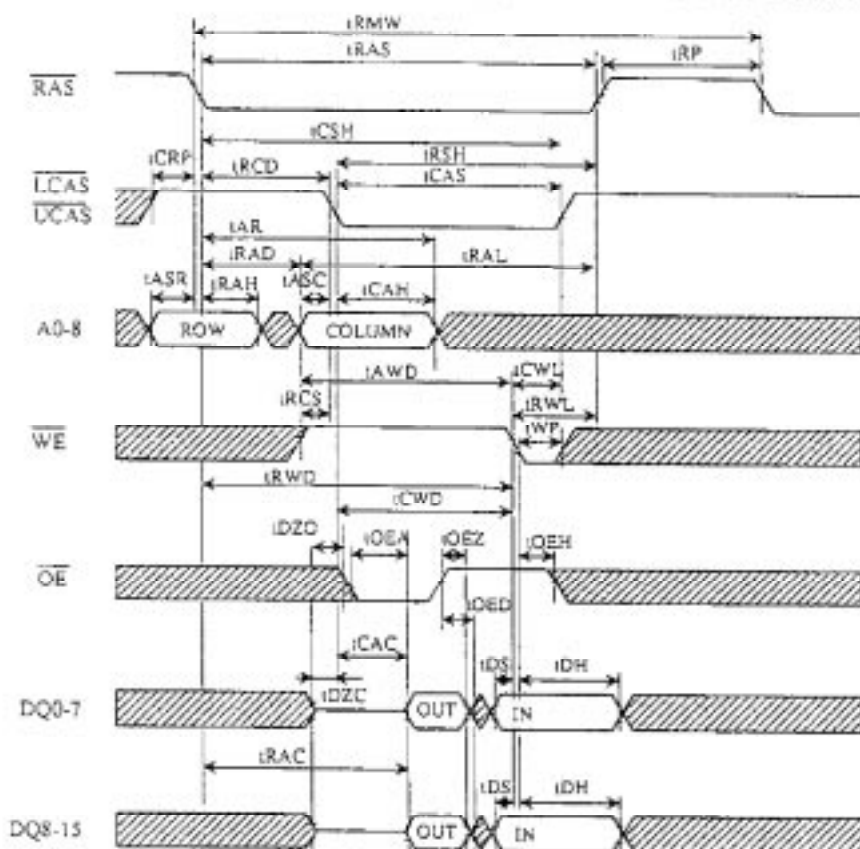
▨ : "H" or "L"

LATE WRITE CYCLE ( $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  active)



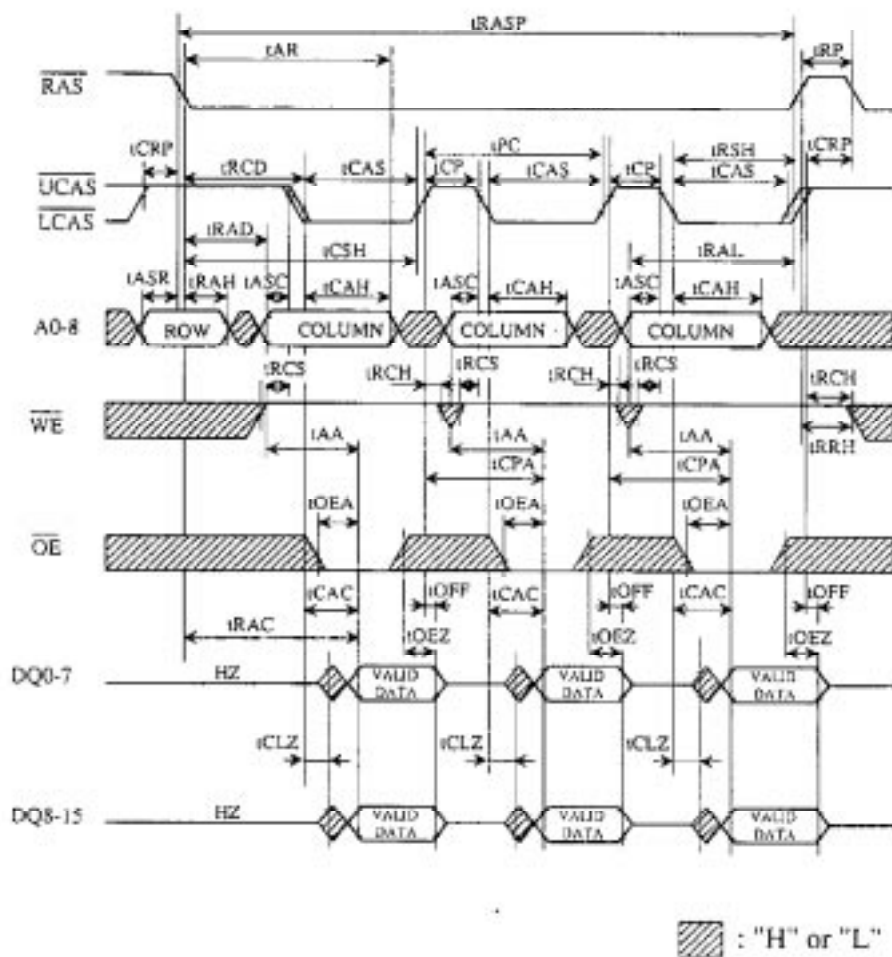
▨ : "H" or "L"

READ MODIFY WRITE CYCLE ( $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  active)

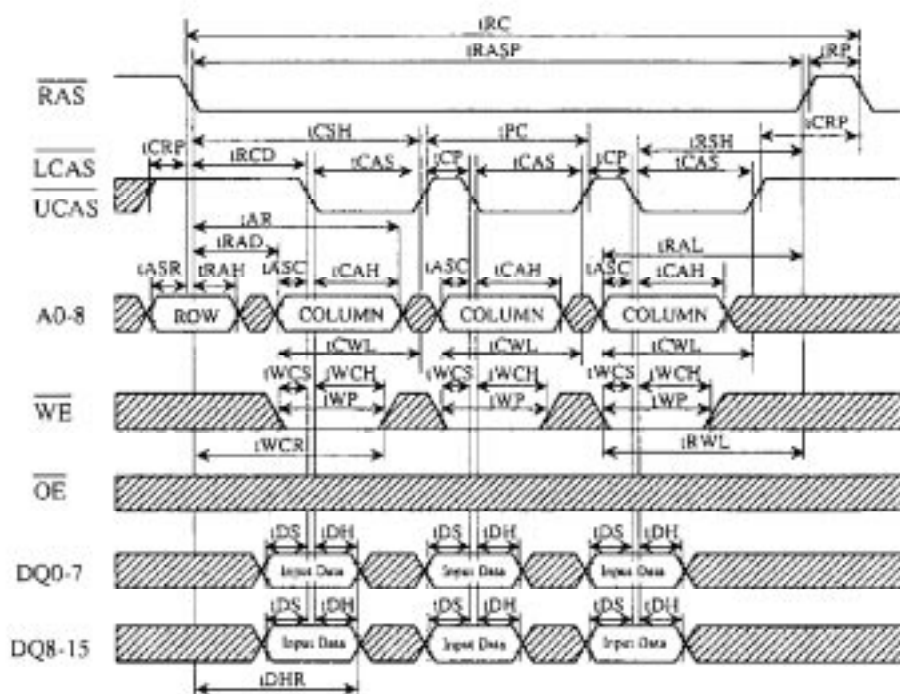


▨ : "H" or "L"

### FAST PAGE MODE READ CYCLE

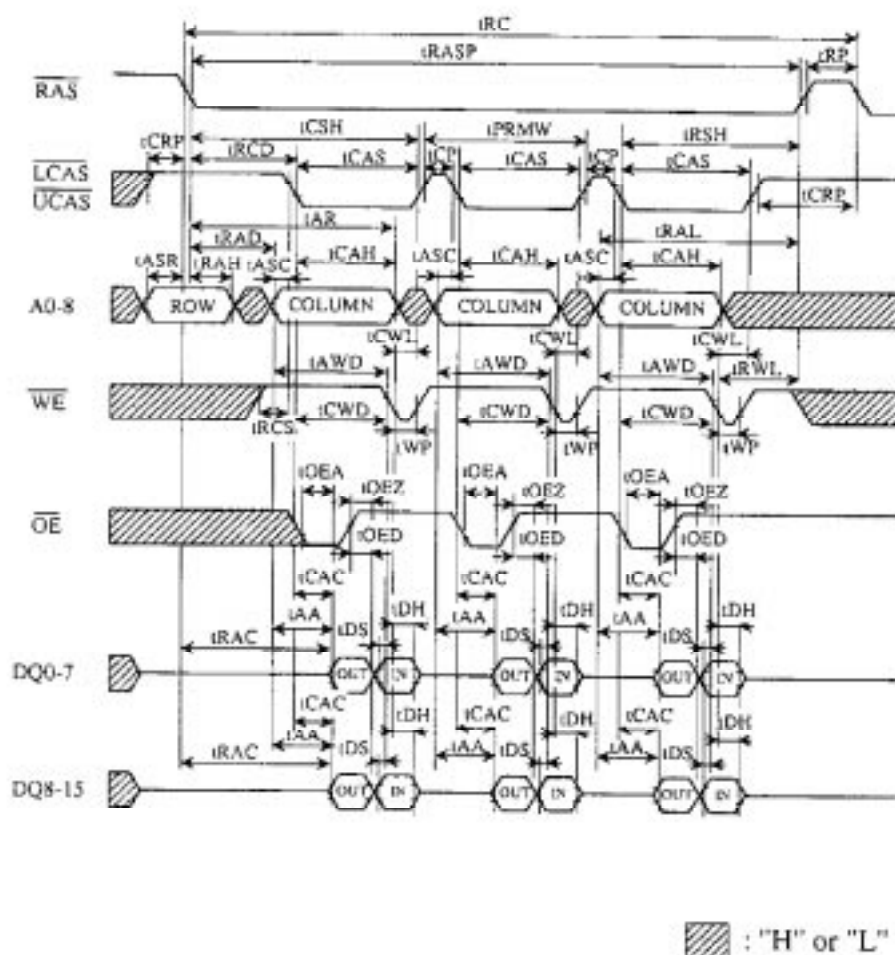


### FAST PAGE MODE EARLY WRITE CYCLE

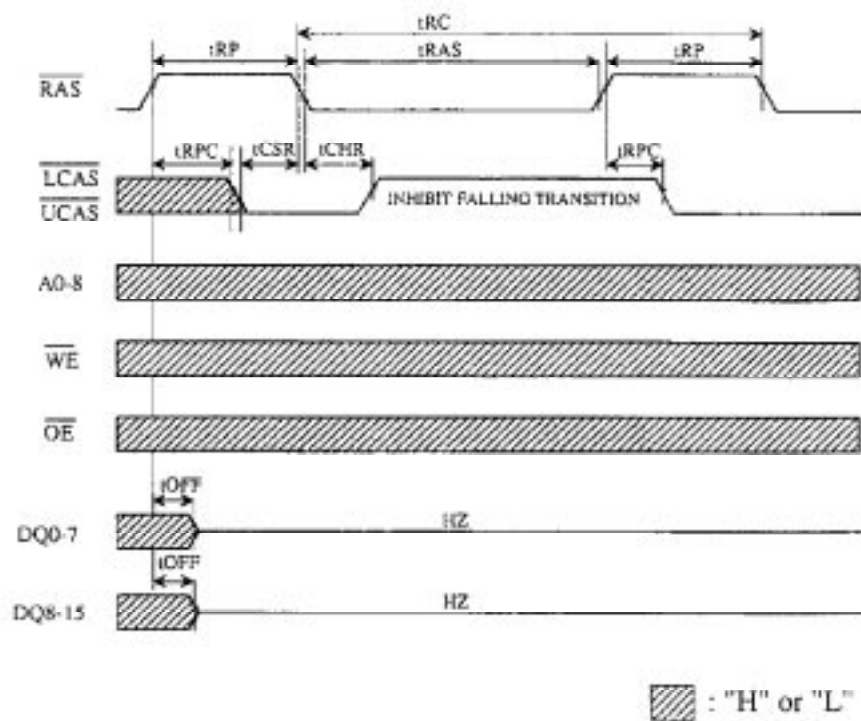


▨ : "H" or "L"

## FAST PAGE MODE READ MODIFY WRITE CYCLE

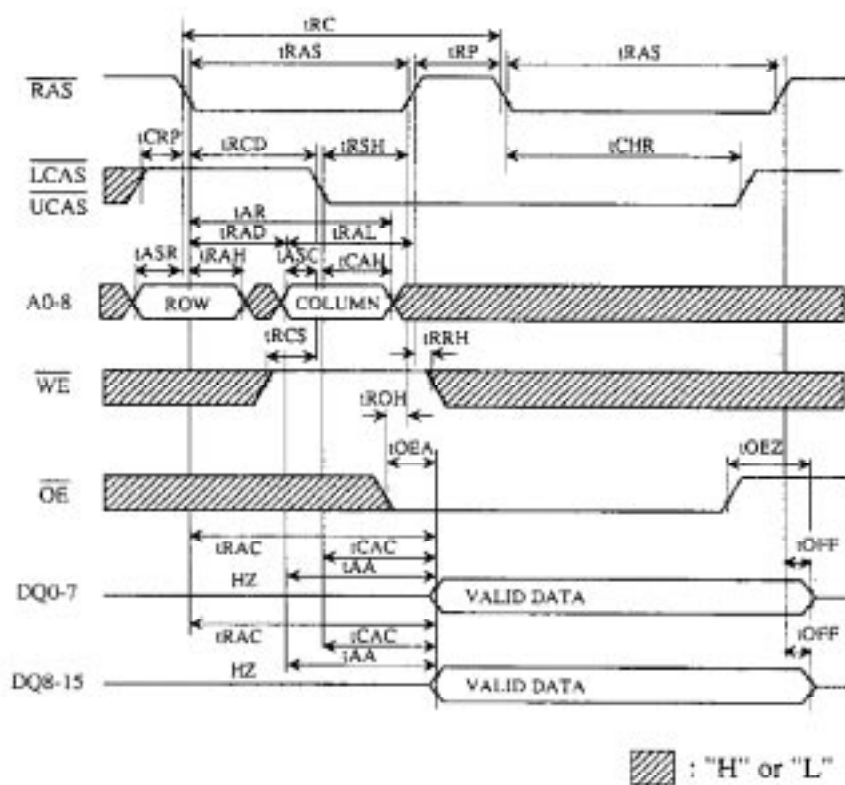


**CAS BEFORE RAS REFRESH CYCLE**

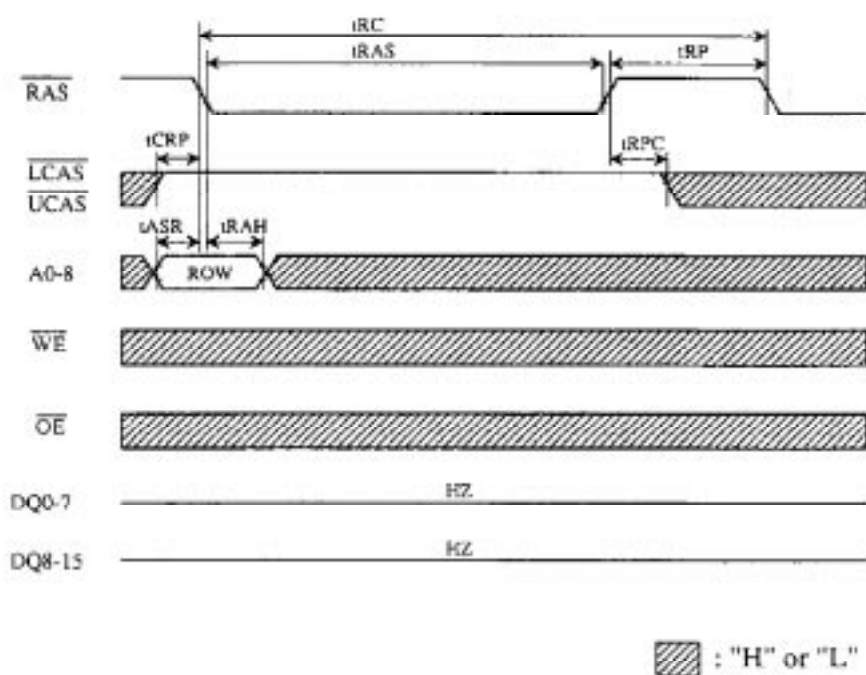




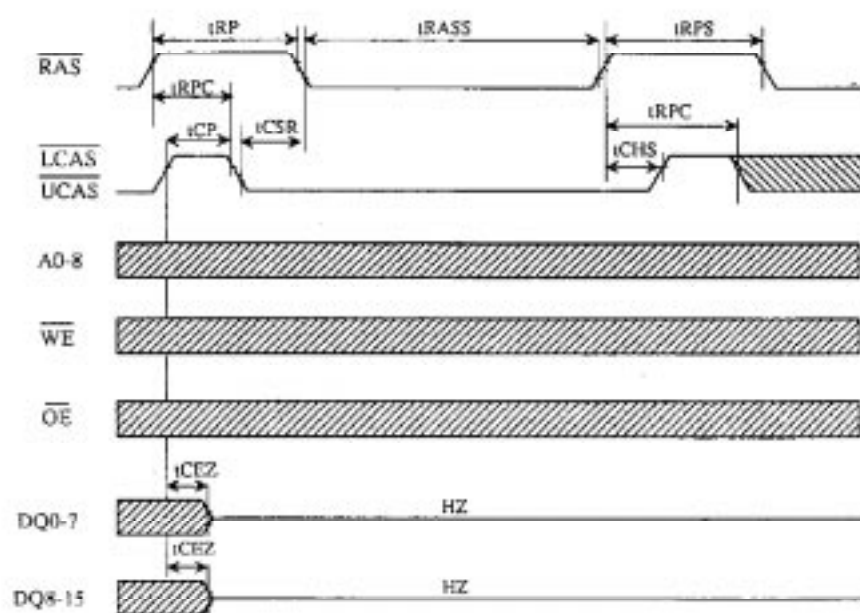
## HIDDEN REFRESH CYCLE



### RAS ONLY REFRESH CYCLE



### CAS BEFORE RAS SELFREFRESH CYCLE



▨ : "H" or "L"