ADC4340

**16-Bit 200 kHz
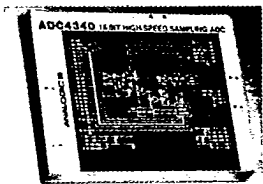Sampling A/D Converter**

Performance Features

The ADC4340 is a 16-bit 200 kHz sampling A/D converter featuring excellent differential linearity and low distortion. With a built-in sample-and-hold amplifier, the ADC4340 alleviates many of the design problems inherent in digitizing fast time-varying signals to the 16-bit level. For applications requiring only a 200 kHz sampling rate, the ADC4340 is an excellent alternative to the ADAM-826-1. Providing user-selectable unipolar and bipolar input ranges as well as TTL and CMOS compatible digital control signals and data, the ADC4340 is easy to use in various applications. The ADC4340 has a differential linearity of ±0.5 LSB and a maximum integral linearity error of ±0.003% of the full scale range, thus offering the time domain performance required in high speed, high resolution multiplexed data acquisition systems.

In addition, the ADC4340 offers the low distortion necessary for frequency domain applications, such as professional audio systems or digital telecommunications systems. At 1 kHz the ADC4340 exhibits a signal to noise ratio of 88 dB, peak distortion of −100 dB and total harmonic distortion of −92 dB.

With a 200 kHz throughput rate, the ADC4340 provides an economical solution for digitizing multiple audio channels since it can digitize four channels at 48 kHz per channel or two channels at 96 kHz per channel when used with a fast multiplexer. The ADC4340 is conveniently packaged in a 3.8" x 4.5" shielded module and consumes only 2.45 watts. This A/D converter offers a superb combination of speed, resolution, accuracy, and low distortion, making the ADC4340 ideal for a broad range of demanding, high performance applications.

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Features

■ 16 Bit Resolution

■ 200 kHz Throughput Rate

■ Signal to Noise Ratio 88 dB (1 kHz)

■ Peak Distortion −100 dB (1 kHz)

■ Total Harmonic Distortion −92 dB (1 kHz)

■ TTL/CMOS Compatibility

■ Excellent Differential Linearity (±0.5 LSB)

■ Integral Linearity ±0.003% FSR

■ No Missing Codes

■ Guaranteed Monotonicity

■ Low Power

■ Ease of Use

■ Low Cost

■ High Input Impedance (100 MΩ)

■ User-Selectable Unipolar and Bipolar Input Ranges

Applications

■ Digital Telecommunications

■ Professional Audio Systems

■ High Frequency Communications

■ Automatic Test Equipment

■ High Speed Data Acquisition

■ Satellite Communications

■ Seismic Instrumentation
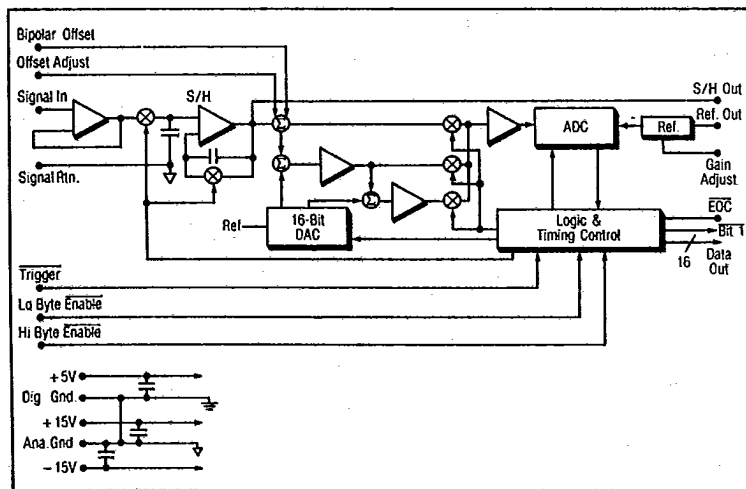
■ High Resolution Imaging

Figure 1. ADC4340 Functional Block Diagram.

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ANALOG INPUT
Input Range
0 to + 10V
±5V
Input Bias Current
100 pA Max., 500 nA Typ.
Input Capacitance
5 pF Typ.
Input Impedance
100 MΩ Min.

DIGITAL INPUTS
Logic Levels
LSTTL/CMOS Compatible
Logic "0"
0.8V Max.
Logic "1"
2.0V Min.
Trigger Input
Negative Edge Triggers Conversion
Trigger Pulse Width
50 ns Min.
Loading
1 LSTTL Load
High Byte Enable
Active Low
Low Byte Enable
Active Low

DIGITAL OUTPUTS
Output Coding
Binary
Offset Binary
Two's Complement
Data Outputs Fan-out
10 LSTTL Loads Max.
Logic Levels
Logic "0"
0.4V Max.
Logic "1"
2.4V Min.
End of Conversion (EOC)
Data Valid on High to Low Transition

REFERENCE OUTPUT
Voltage
+ 10.000V ± 20 mV
(2 mA Load Max.)[8]

DYNAMIC CHARACTERISTICS
Maximum Throughput Rate
200 kHz Min.
A/D Conversion Time
3.0 μs Typ.

Signal to Noise Ratio [2,5]
1 kHz 88 dB Typ., 86 dB Min.
10 kHz
88 dB Typ.
20 kHz
88 dB Typ.
Peak Distortion [3,5]
1 kHz
− 100 dB Typ., − 96 dB Min.
10 kHz
− 96 dB Typ.
20 kHz
− 96 dB Typ.
Total Harmonic Distortion [4,5]
1 kHz
− 92 dB Min.
10 kHz
− 92 dB Typ.
20 kHz
− 92 dB Typ.
Small-Signal Bandwidth
2 MHz Min.
S/H Acquisition Time
1.5 μs Typ., 2.0 μs Max.
S/H Aperture Delay
25 ns Typ.
S/H Aperture Jitter
± 400 ps Max.
S/H Feedthrough
− 90 dB Min.
Hold Mode Droop [6]
5 μV/μs
Dielectric Absorption
± 0.001% of input signal voltage change,
typical

TRANSFER CHARACTERISTICS
Resolution
16 Bits
Quantization Error
± 0.5 LSB
Integral Non-Linearity
± 0.003% FSR Max.
Differential Non-Linearity
± 0.5 LSB Typ.,
± 0.75 LSB Max.
Integral Non-Linearity
± 0.003% FSR Max.
Full Scale Range [7]
Factory Calibrated to ± 0.01%
Offset Error [7]
Factory Calibrated to ± 0.01%
Monotonicity
Guaranteed
No Missing Codes
Guaranteed from 0°C to 60°C

A/D Converter Noise[9]
50 μV rms Typ.,
70 μV rms Max.

STABILITY (0°C to 60°C)
Differential Non-Linearity
±0.5 ppm FSR/°C Max.

Offset Voltage
±25 μV/°C Typ.,
±50 μV/°C Max.

Gain
±5 ppm FSR/°C Max.

Warm-Up Time
15 Minutes

Supply Rejection
Gain
±10 ppm FSR/% Max.

Offset
±10 ppm FSR/% Max.

POWER REQUIREMENTS
Supply Range
±15V Supplies
14.5V Min., 15.5V Max.
+5V Supplies
4.75V Min., 5.25V Max.

Current Drain
+15V
80 mA Typ.
−15V
70 mA Typ.
+5V
40 mA Typ.

Power Consumption
2.45W Typ.

ENVIRONMENTAL & MECHANICAL
Temperature Range
Rated Performance
0°C to +60°C

Storage
−25°C to +75°C

Relative Humidity
0 to 85% Non-Condensing up to 40°C

Dimensions
3.8" x 4.5" x 0.55"

Shielding
Electromagnetic 6 Sides
Electrostatic 6 Sides

Case Potential
Ground

Mating Connector
J1: Amp 103183-7 or equiv. 16-pin
J2: Amp 1-103183-2 or equiv. 28-pin

Notes

1. Unless otherwise noted, all specifications apply at 25°C. Supplies are ±15V and +5V.

2. Signal to Noise Ratio represents the ratio between the rms value of the signal and the total rms noise below the Nyquist rate. The total rms noise is computed by: (1) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonic frequency bins; and (3) computing the rms noise from the sum of (1) and (2).

3. Peak Distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the signal. Note that in computing Peak Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 2.

4. Total Harmonic Distortion represents the ratio between the rms sum of all harmonics up to the 40th harmonic and the rms value of the signal. Note that in computing Total Harmonic Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 2.

5. ±5V input signal.

6. Doubles every 10°C.

7. Refer to "Output Coding and Trim Procedure" for field adjustable gain and offset procedures.

8. Load must remain constant during conversion.

9. Includes noise from the S/H and A/D converter.

Output Coding and Trim Procedure

To select the bipolar ±5V input range, jumper the Ref. Out pin to the Bipolar pin. To select the unipolar 0 to +10V input range, jumper the Sig. Rtn. pin to the Bipolar pin. To select two's complement output coding, use $\overline{B1}$ instead of B1.

To trim the offset of the ADC4340, apply 0V to the analog input and adjust the offset trim potentiometer until the correct output code (see Figure 2) is produced. Increase the applied voltage by +76 μV and adjust the potentiometer so the LSB undergoes a code transition, alternating equally between 0 and 1.

To trim the gain of the ADC4340, apply positive full scale (see Figure 2) to the analog input and adjust the gain trim potentiometer until the correct output code (see Figure 2) is produced. Reduce the applied voltage by −76 μV and adjust the potentiometer so the LSB undergoes a code transition, alternating equally between 0 and 1.

Layout Considerations

To maintain the 16-bit performance of the ADC4340 requires a careful layout of the printed-circuit board. For example, the analog input should be separated from the digital control lines to reduce glitches induced during

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digital switching. It is also important to con-figure a low impedance ground plane on the printed-circuit board. Provide separate analog and digital grounds and return them separately to the system power supply, which should be a well-regulated linear supply.

If the ADC4340 is driving more than two TTL loads or if the digital bus consists of more than 6" of etch, then a buffer should be used as shown in Figure 11.

TRUTH TABLE	
INPUT VOLTAGE	DIGITAL OUTPUT
BINARY	MSB LSB
+9.999847V	1111111111111111
+9.999771V	1111111111111110/1
+5.000000V	1000000000000000
+0.000076V	0000000000000000/1
+0.000000V	0000000000000000
OFFSET BINARY	MSB LSB
+4.999847V	1111111111111111
+4.999771V	1111111111111110/1
+0.000076V	1000000000000000/1
+0.000000V	1000000000000000
−5.000000V	0000000000000000
TWO'S COMPLEMENT	MSB LSB
+4.999847V	0111111111111111
+4.999771V	0111111111111110/1
+0.000076V	0000000000000000/1
+0.000000V	0000000000000000
−4.999847V	1000000000000001
−5.000000V	1000000000000000

Figure 2. Output Coding for ADC4340.

Timing Considerations

In most cases, the ADC4340 will be connected such that a single trigger command will cause the S/H to go into the hold mode. Under control of the internal timing logic, the A/D Converter will then begin the conversion while hold mode settling takes place. At the completion of the
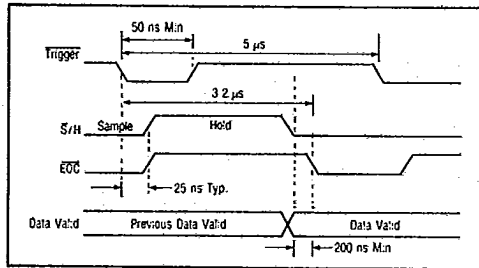

Figure 3. ADC4340 Timing Diagram.

conversion process, the S/H will automatically be returned to the sample mode to await the next trigger command. Data is valid 15 ns before the falling edge of $\overline{EOC}$. It is important to note that the connection to the $\overline{EOC}$ and Data lines must be kept as short as possible, or alternatively, buffered prior to connection to external circuitry.

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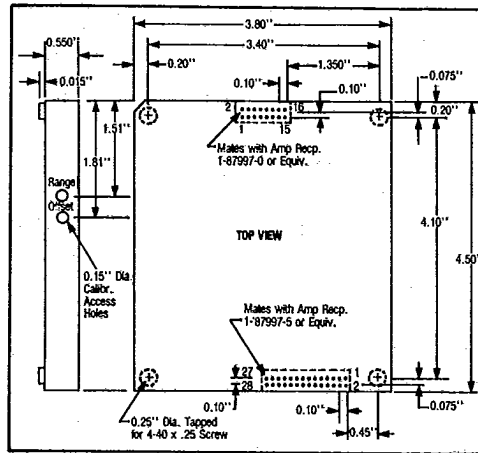Figure 4. ADC4340 Mechanical Outline.

J1 Pin Assignments		J2 Pin Assignments	
1. Offset Adj.	9. Bipolar	1. Trigger	15. Bit 11
2. Gain Adj.	10. Ref. Out	2. EOC	16. Bit 12
3. −15V	11. S/H Out	3. N/C	17. Bit 9
4. −15V	12. Ref. Rtn.	4. N/C	18. Bit 10
5. Analog Rtn.	13. Sig. Rtn.	5. +5V	19. Lo Byte Enable
6. Analog Rtn.	14. Sig. Rtn.	6. +5V	20. Hi Byte Enable
7. +15V	15. Sig. In	7. Digital Rtn.	21. Bit 7
8. +15V	16. Sig. Rtn.	8. Digital Rtn.	22. Bit 8
		9. Bit 1 MSB	23. Bit 5
		10. Digital Rtn.	24. Bit 6
		11. Bit 15	25. Bit 3
		12. Bit 16 LSB	26. Bit 4
		13. Bit 13	27. Bit 1 MSB
		14. Bit 14	28. Bit 2

Figure 5. ADC4340 Pinouts.

Principles Of Operation

To understand the operating principles of the ADC4340 A/D converter, refer to Figure 6. The simplified block diagrams in paths a, b, and c in Figure 6 illustrate the three successive passes in the sub-ranging conversion scheme of the ADC4340. For all three passes, the lines labeled "From S/H" come from the output of the internal sample-and-hold amplifier. In the first pass (a), the input signal is attenuated by a factor of 4. It thus converts the 10V full-scale range of the input to the 2.5V full-scale range of the 6-bit flash A/D converter. The 6-bit A/D

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converter then performs a 6-bit approximation of the input signal. The outputs of the A/D converter, via latches in a specialized gate array, drive the six MSBs of the 16-bit D/A converter.

In the second pass (b), a difference amplifier subtracts the D/A converter's output voltage from the input voltage then amplifies this difference by a factor of 8. The ±5V output range of the D/A converter matches the ±5V full-scale range of the input voltage. The output of the difference amplifier provides the input signal for the 6-bit flash A/D converter. The A/D converter's outputs are latched into the gate array, which supplies the next five lower-order bits of the D/A converter. The gain factor in this second pass is such that the difference signal cannot exceed half-scale in the 6-bit A/D converter. Since the MSB of this conversion overlaps the previous conversion, the resolution of the A/D conversion in the second pass is five bits (not six).

In the third pass (c), the gain-of-256 difference amplifier subtracts the D/A converter's output voltage from the input voltage. The outputs of the flash A/D converter are latched into the gate array. The effective resolution of the conversion is thus 6 + 5 + 5, or 16 bits. Using the error signals generated by the D/A converter in the multiple passes, logic circuitry in the gate array performs an error correction on the converted output.

The ADC4340 has a 3-state output structure. Users can enable the eight MSBs, eight LSBs, or both, by using the HI BYTE ENABLE and LO BYTE ENABLE pins. This feature makes it possible to transfer data from the ADC4340 to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered; see Figure 11.

The digital error-correction technique used in the ADC4340 provides an output word that is accurate and linear to within the full 16-bit resolution of the A/D converter. The method corrects for any gain and linearity errors in the amplifying circuitry, as well as in the 6-bit flash A/D converter. Without the error-correction technique, it would be necessary that all the components in the ADC4340 — the difference amplifier, the switched gain amplifier, and the 6-bit flash A/D converter — be accurate and linear to a 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve on a production basis. The key to the conversion technique used in the ADC4340 is the 16-bit-accurate and 16-bit-linear D/A converter, which serves as the reference element for the conversion passes as well as for the error-correction mechanism. The use of the sub-ranging architecture in the ADC4340 results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 16-bit level.
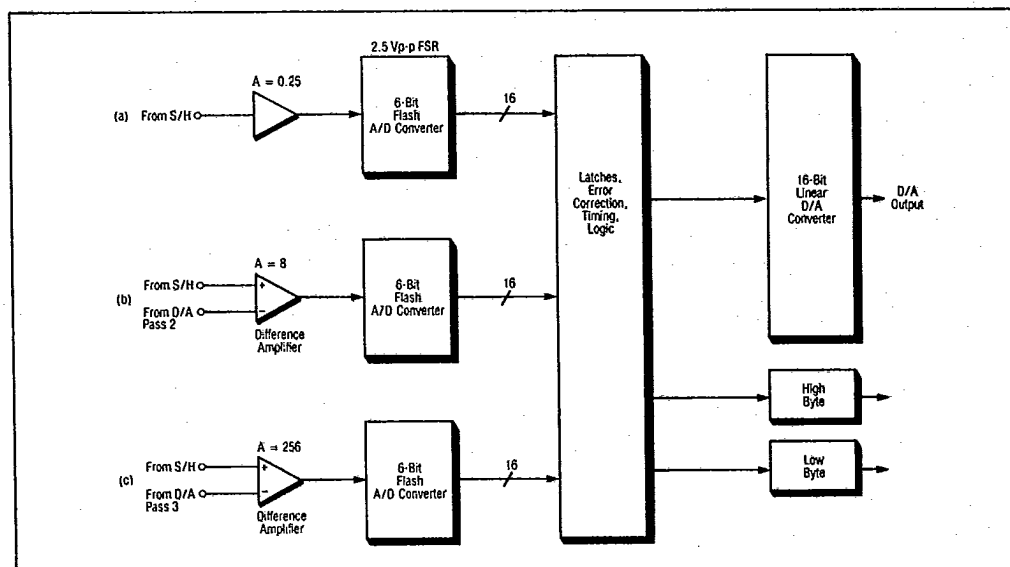

Figure 6. Operating Principle of the ADC4340.

Performance Testing   T-51-10-16

The customer is assured that all ADC4340's shipped meet published specifications since each module is exhaustively tested prior to shipment. The customer receives with the module the results of these tests in the form of a computer-printed data sheet detailing the performance of that particular unit. Each ADC4340 is exercised both in the "Amplitude Domain" and the "Frequency Domain".

Amplitude Domain Testing

Analogic's Amplitude Domain automatic test equipment includes a 22-bit digital-to-analog converter with a reference traceable to the National Bureau of Standards. A simplified block diagram of this test system is shown in Figure 7. The data sheet generated provides the customer with detailed results on integral linearity, A/D converter noise, absolute accuracy, conversion time, power supply current, and power supply rejection. A typical amplitude domain data sheet for the ADC4340 is shown in Figure 8.

Frequency Domain Testing

The performance of the ADC4340 in the frequency domain is critical in many applications; therefore, Analogic is thorough in specifying and testing the module in the frequency domain. A simplified block diagram of the Frequency Domain Test System is shown in Figure 9. This automatic test system consists of a host computer, a floating point array processor manufactured by Analogic, a low noise, low distortion sine wave generator, and a timebase for adjusting the sampling rate of the A/D converter under test. A typical frequency domain data sheet produced by this system is shown in Figure 10.

It is important that the user thoroughly understand Analogic's definitions of these frequency domain parameters, which are summarized below.

Peak Distortion: Ratio, expressed in dB, between the rms value of the highest spurious spectral component below the Nyquist rate and the rms value of the input signal.

$$\text{Peak Distortion} = 20 \log \frac{\text{rms value of max. spurious component}}{\text{rms value of input signal}}$$

Signal to Noise Ratio: Ratio, expressed in dB, between the rms value of the signal and the total rms noise below the Nyquist rate.

Total Harmonic Distortion: Ratio, expressed in dB, between the rms sum of all harmonics up to the 40th harmonic and the rms value of the signal.

Direct Harmonic Distortion: Ratio, expressed in dB, between the rms sum of all the components below the Nyquist rate that are harmonically related to the signal and the rms value of the signal.

Reflected Harmonic Distortion: Ratio, expressed in dB, between the rms sum of all aliased harmonics and the rms value of the signal.

Note that the estimated noise, based on those frequency bins not correlated with the test signal, is first removed from the harmonic frequency bins before the above distortion values are calculated.
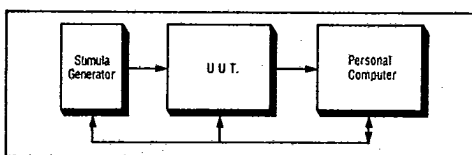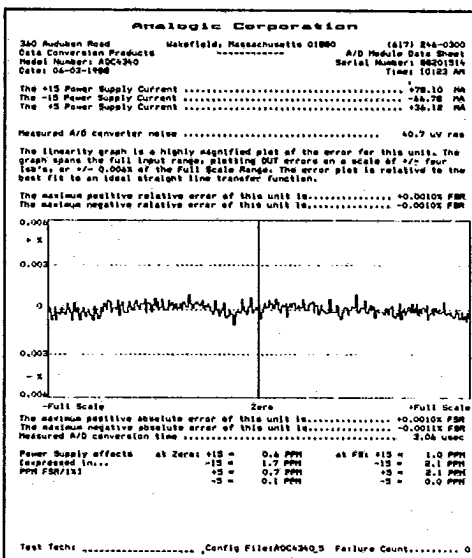

Figure 7. "Amplitude Domain" Test System.
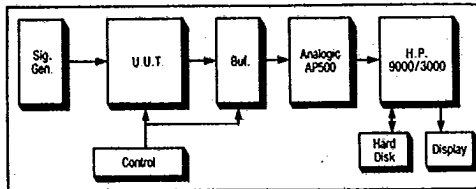

Figure 8. "Amplitude Domain" Data Sheet.

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Figure 9. "Frequency Domain" Test System.

Figure 10. "Frequency Domain" Data Sheet.

Typical Application

The circuit in Figure 11 illustrates a typical application of the ADC4340 A/D converter. This circuit is used in computer tomography, although it could be generalized for any high speed, multiplexed data acquisition application.

In the circuit, the X-ray Detector emits a signal that is related to the intensity of the x-rays that have passed through a patient. There are 256 such signals that are multiplexed to an auto-ranging PGA and ultimately sampled by the ADC4340 A/D converter and processed by the minicomputer. The auto-ranging PGA, with gains of 1, 8, and 64, in conjunction with the 16-bit A/D converter, provides an equivalent dynamic range of 20 bits. Typically, four such circuits are combined such that 1024 channels
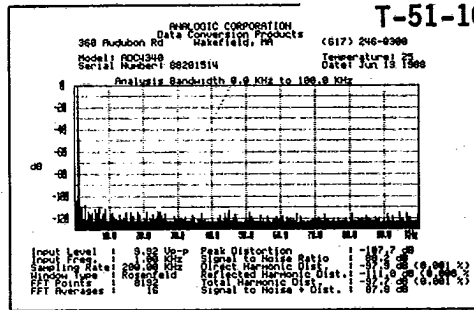
can be sampled. However, for simplicity, only one of the four A/D converters is shown.

The 200 kHz sampling rate of the ADC4340 is required to handle such a large number of channels, since the 1024 channels must be sampled every 2 ms. After an image consisting of 1024 signals has been processed, the x-ray source is rotated by a fraction of a degree and another image of 1024 signals is processed. In this way, an image of a slice of tissue can be reconstructed by the computer. The 16-bit resolution of the ADC4340 makes it ideal for this critical application.
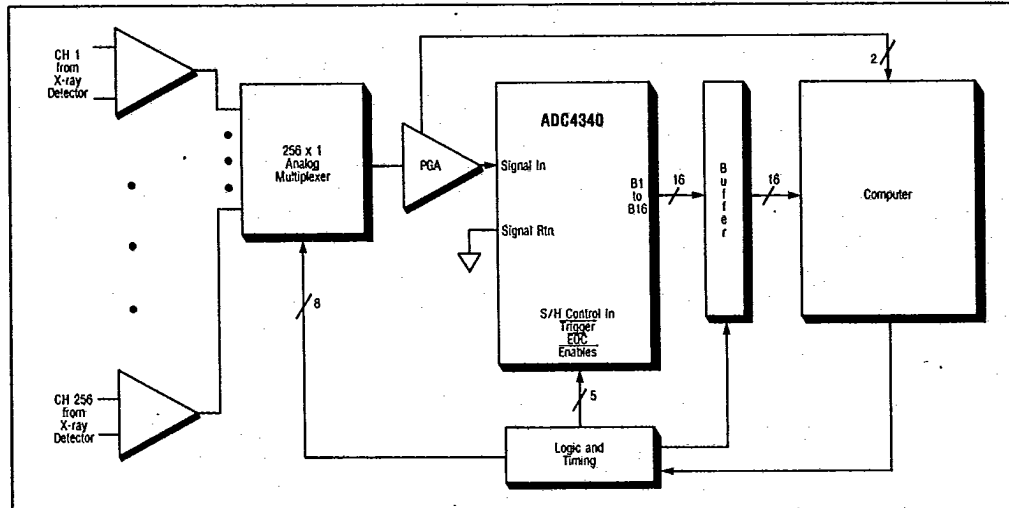

Figure 11. Typical Application Circuit for ADC4340.

Ordering Guide

Specify **ADC4340**

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