

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator type

Description

The CXP87800 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP87852/87860.

Features

- A wide instruction set (213 instructions) which cover various types of data.
 - 16-bit operation/multiplication and division/boolean bit operation instructions

- Minimum instruction cycle
- Applicable EPROM

- Incorporated RAM capacity
- Peripheral functions
 - A/D converter

— Serial interface

— Timer

— High precision timing pattern generator

— PWM/DA gate output

— Servo input control

— VSYNC separator

— FRC capture unit

— PWM output

— VISS/VASS circuit

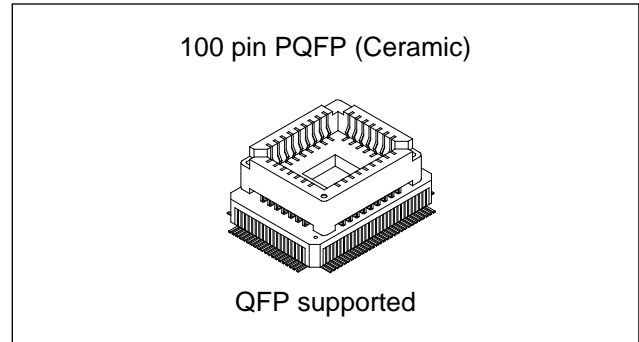
— Remote control receiving circuit

— General purpose prescaler

— HSYNC counter

- Interruption
- Standby mode
- Package

Note) Mask option depends on the type of the CXP87800. Refer to the Products List for details.



250ns at 16MHz operation (4.5 to 5.5V)

LCC type 27C512

(Maximum 60K bytes are available.)

2048 bytes

8-bit, 12-channel, successive approximation method
(Conversion time of 20 μ s/16MHz)

Buffer RAM 1 channel

(Auto transfer for 1 to 32 bytes)

8-bit and 8-stage FIFO 1 channel

(Auto transfer for 1 to 8 bytes)

Incorporated two-wire 8-bit and 8-stage FIFO 1 channel

(Auto transfer for 1 to 8 bytes)

8-bit timer, 8-bit timer/counter

19-bit time base timer, 32kHz timer/counter

PPG 19-pin, 32-stage programmable

RTG 5 pins, 2 channels

PWM output 12 bits, 2 channels

(Repetitive frequency of 62.5kHz/16MHz)

DA gate pulse output 13 bits, 4channels

Capstan FG, drum FG/PG, CTL input

Incorporated 26-bit and 8-stage FIFO

14 bits

Pulse duty auto detection circuit

8-bit pulse measurement counter with on-chip 6-stage FIFO

7 bits (SYNC1 input frequency division, FRC capture possible.)

12-bit event counter (SYNC1 input count)

23 factors, 15 vectors, multi-interruption possible

SLEEP/STOP

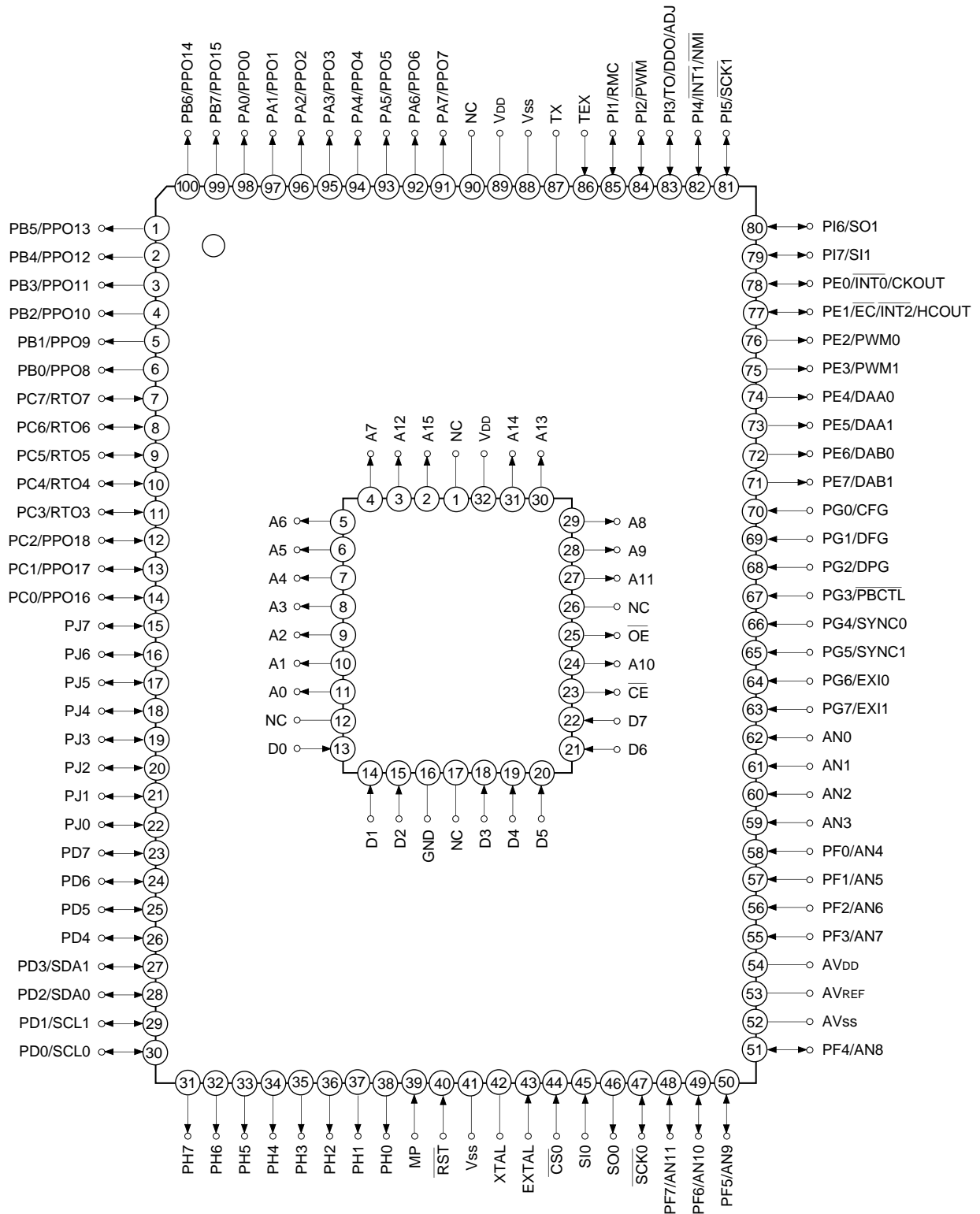
100-pin ceramic PQFP

Structure

Silicon gate CMOS IC

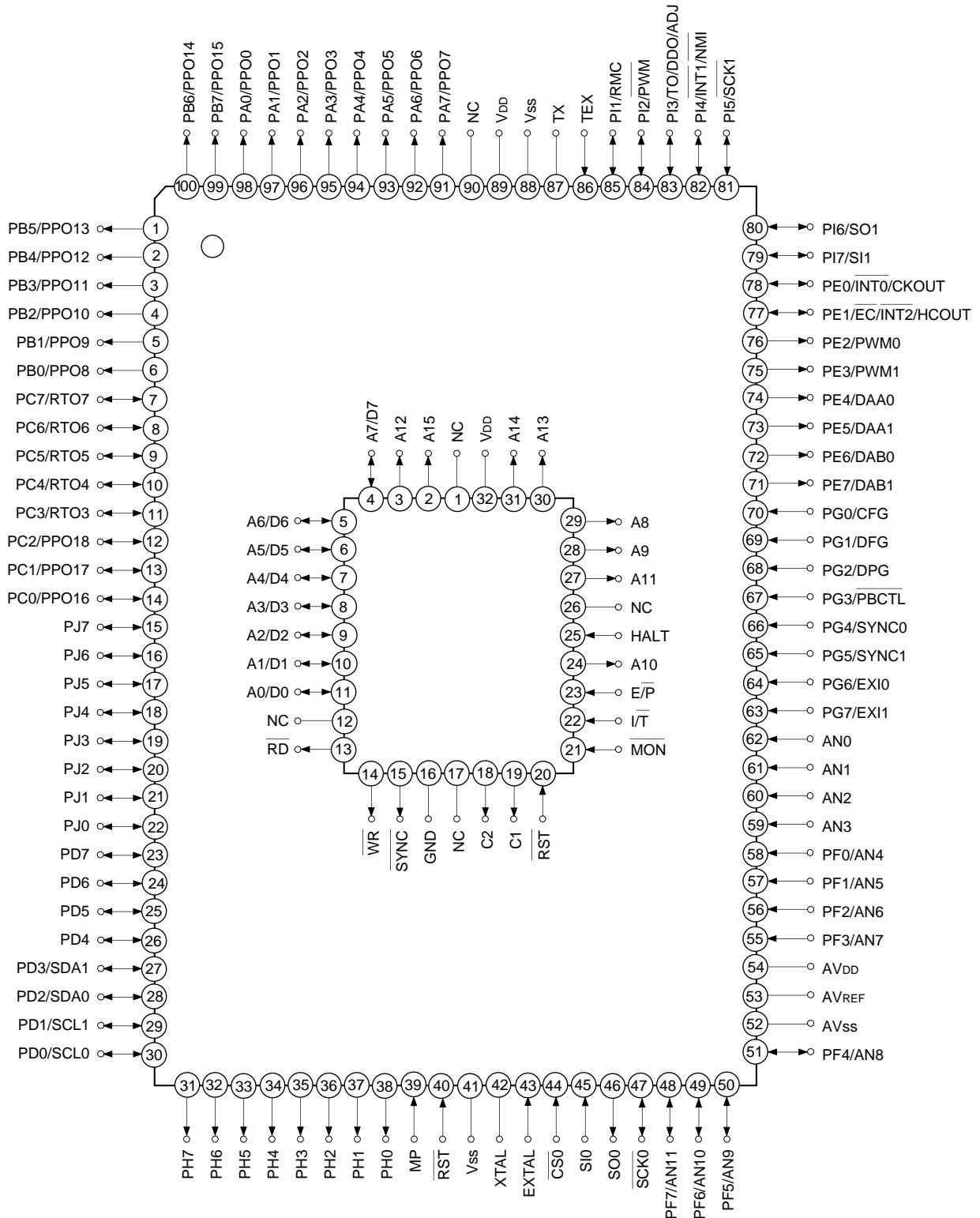
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Pin Assignment in Piggyback Mode (QFP package)



- Note)**
1. NC (Pin 90) is always connected to V_{DD}.
 2. V_{SS} (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) is always connected to GND.

Pin Assignment in Evaluator Mode (QFP package)



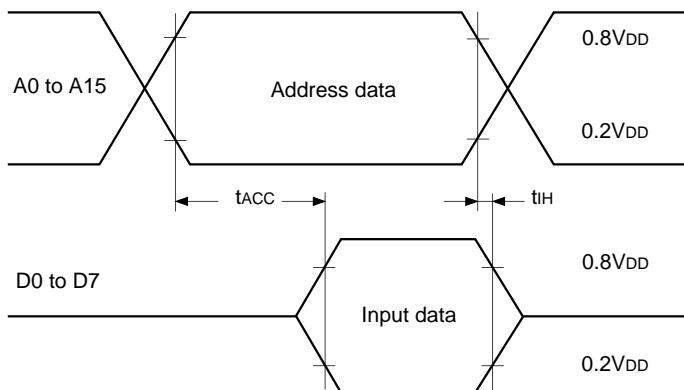
- Note)**
1. NC (Pin 90) is always connected to V_{DD}.
 2. V_{SS} (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) is always connected to GND.

EPROM Read Timing ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100*1	ns
				75*2	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

*1 At 12MHz operation ($V_{DD} = 4.5$ to 5.5V)

*2 At 16MHz operation ($V_{DD} = 4.5$ to 5.5V)



Products List

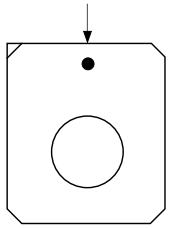
Option item	Products		
	Mask product		Piggyback/evaluator product
	CXP87852	CXP87860	CXP87800-U01Q
Package	100-pin plastic QFP		100-pin ceramic PQFP
ROM capacity	52K bytes	60K bytes	EPROM 60K bytes
			27C512 × 1
Pull-up resistor for reset pin	Existent/Non-existent		Existent
Input circuit format*1	CMOS schmitt/TTL schmitt		TTL schmitt

*1 The input circuit format can be selected to PG4/SYNC0 and PG5/SYNC1, respectively.

Piggyback mode/evaluator mode can be switched as shown below.

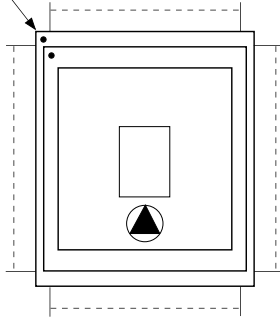
Piggyback mode

LCC type EPROM
Pin 1 marking



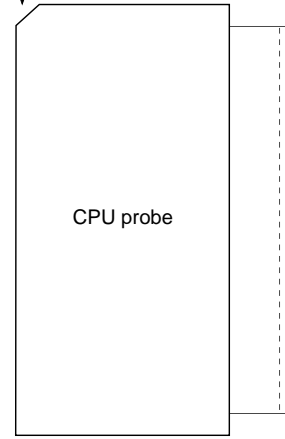
Piggyback/evaluator product

Pin 1 index



Evaluator mode

Pin 1 marking



Note)

Note) Evaluation cap should be connected to CPU probe.

