Am2906

Quad Two-Input OC Bus Transceiver with Parity

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver output can sink 100mA at 0.8V max.
- Two-port input to D-type register on driver.
- Internal 4-bit odd parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.

GENERAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

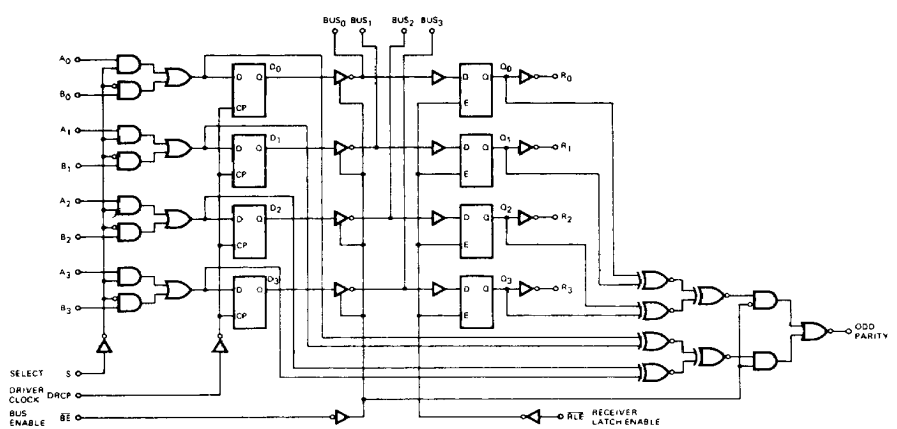
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

BLOCK DIAGRAM



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CONNECTION DIAGRAM
Top View

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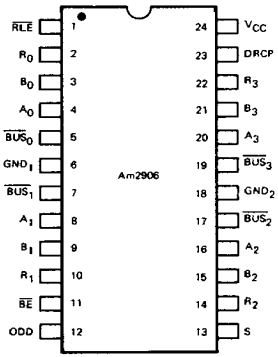

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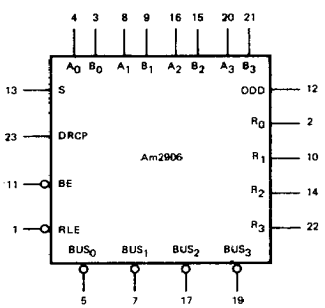
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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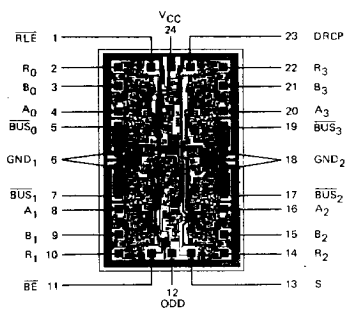
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.080" x 0.130"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2906 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin CERDIP
  - F– 24-pin flatpak
  - P– 24-pin plastic DIP
  - X– Dice
- **Am2906** — Device type
  - OC Bus Transceiver

Valid Combinations	
Am2906	PC DC, DCB, DM, DMB FM, FMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 8 16, 20	A_0, A_1, A_2, A_3	I	The "A" word data input into the two input multiplexer of the driver register.
3, 9 15, 21	B_0, B_1, B_2, B_3	I	The "B" word data input into the two input multiplexers of the driver register.
13	S	I	Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.
23	DRCP		Driver Clock Pulse. Clock pulse for the driver register.
11	$\overline{BE}$		Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.
5 7 17, 19	$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$	O	The four driver outputs and receiver inputs (data is inverted).
2, 10 14, 22	R_0, R_1, R_2, R_3	O	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
1	$\overline{RLE}$	O	Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
12	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in high-impedance state.

FUNCTION TABLE

INPUTS						INTERNAL TO DEVICE		BUS	OUTPUTS		
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	ODD	FUNCTION
X	X	X	X	H	X	X	X	Z	X	PQ	Driver output disable
X	X	X	X	L	X	X	X	X	X	PD	Driver output enable
X	X	X	X	H	L	X	L	L	H	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	X	H	H	L	H	
X	X	X	X	X	H	X	NC	X	NC	X	Latch received data
L	L	X	↑	X	X	L	X	X	X	X	Load driver register
L	H	X	↑	X	X	H	X	X	X	X	
H	X	L	↑	X	X	L	X	X	X	X	
H	X	H	↑	X	X	H	X	X	X	X	
X	X	X	L	X	X	NC	X	X	X	X	No driver clock restrictions
X	X	X	H	X	X	NC	X	X	X	X	
X	X	X	X	L	X	L	X	H	X	H	Drive Bus
X	X	X	X	L	X	H	X	L	X	H	

H = HIGH
L = LOW
Z = HIGH Impedance

X = Don't care
i = 0, 1, 2, 3
↑ = LOW to HIGH transition

NC = No change
PD = Parity of D flip flops
PQ = Parity of Q latches

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $I_0 \oplus I_1 \oplus I_2 \oplus I_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

I_i = Selected input A_i or B_i

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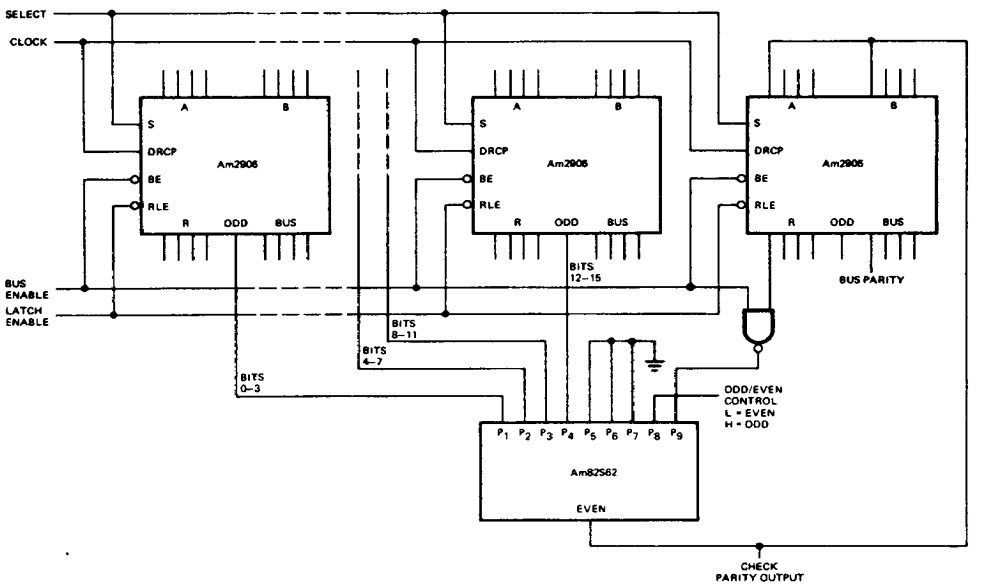
APPLICATIONS



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Generating or checking parity for 16 data bits.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs for
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Bus 200mA
DC Output Current, Into Outputs
(Except Bus) 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	MIL	I_{OH} = −1.0mA	2.4	3.4		Volts
			COM'L	I_{OH} = −2.6mA	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −660µA, V_{IN} = V_{IH} or V_{IL}	MIL		2.5	3.4		
			COM'L		2.7	3.4		
V_{OL}	Output LOW voltage (Except Bus)	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL				0.7	Volts
			COM'L				0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 2.7V					20	µA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX, V_{IN} = 5.5V					100	µA
I_{SC}	Output Short Circuit Current (Except Bus) (Note 3)	V_{CC} = MAX			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX, All inputs = GND				72	105	mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

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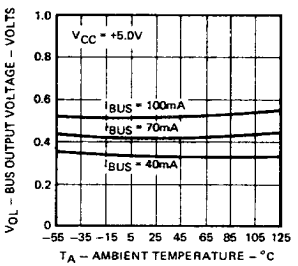
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



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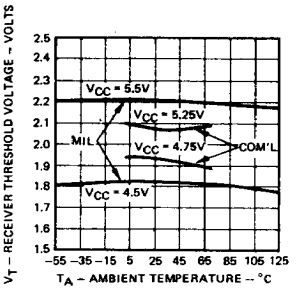
Receiver Threshold Variation Versus Ambient Temperature



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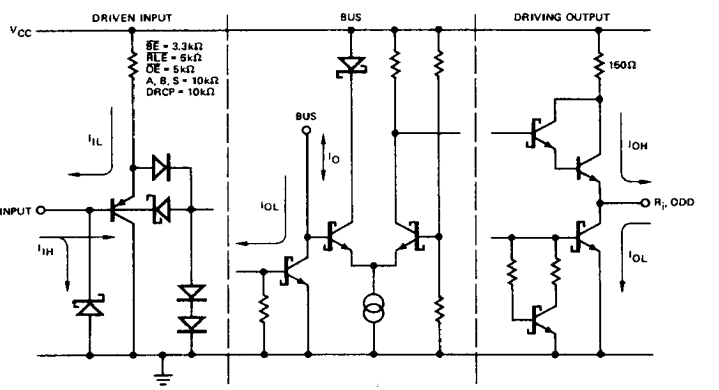
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



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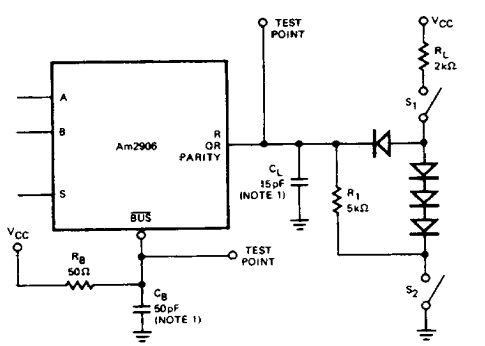
Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL Am2906 Min	COMMERCIAL Am2906 Typ (Note 1)	COMMERCIAL Am2906 Max	MILITARY Am2906 Min	MILITARY Am2906 Typ (Note 1)	MILITARY Am2906 Max	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 50 Ω		21	36		21	40	ns
t_{PLH}				21	36		21	40	
t_{PHL}	Bus Enable ($\overline{BE}$) to BUS			13	23		13	26	ns
t_{PLH}				13	23		13	26	
t_s	Data Inputs (A or B)	C_L = 15 pF, R_L = 2.0 kΩ	23			25			ns
t_h			7.0			8.0			
t_s	Select Inputs (S)		30			33			ns
t_h			7.0			8.0			
t_{PW}	Clock Pulse Width (HIGH)		25			28			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	34		18	37	ns
t_{PHL}				18	34		18	37	
t_{PLH}	Latch Enable to Receiver Output			21	34		21	37	ns
t_{PHL}				21	34		21	37	
t_s	Bus to Latch Enable ($\overline{RLE}$)		18			21			ns
t_h			5.0			7.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	40	ns
t_{PHL}				21	36		21	40	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	40	ns
t_{PHL}				21	36		21	40	

Notes:
1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING TEST CIRCUIT



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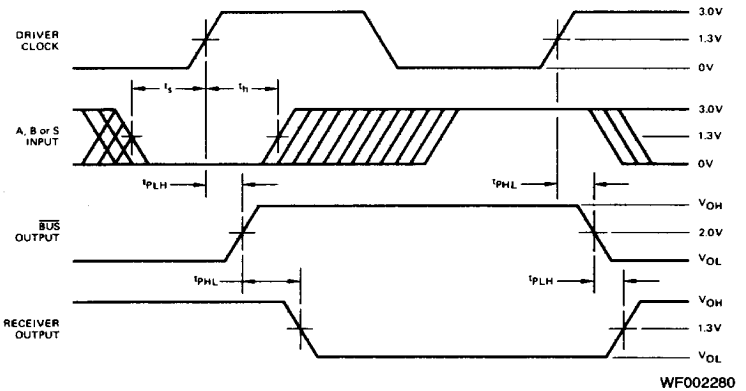
SWITCHING WAVEFORMS



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Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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