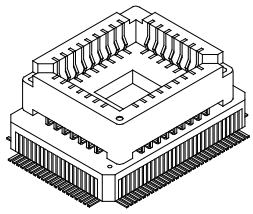
SONY

CXP82200

CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

100 pin PQFP (Ceramic)



Description

The CXP82200 is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP82220/82224.

Features

- Wide-range instruction system (213 instructions) to cover various types of data
  - — 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
  122µs at 32kHz operation
- Applicable EPROM LCC type 27C128, LCC type 27C256
  (Maximum 24K bytes are available.)
- Incorporated RAM capacity 704 bytes (Including fluorescent display data area)
- Peripheral functions
  - — A/D converter 8-bit, 8-channel, successive approximation method
    (Conversion time of 32µs/10MHz)
  - — Serial interface Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
    8-bit clock sync type, 1 channel
  - — Timer 8-bit timer
    8-bit timer/counter
    19-bit time base timer
    16-bit capture timer/counter
    32kHz timer/counter
  - — Fluorescent display panel controller/driver
    Maximum 384 segment display possible
    1 to 16-digit dynamic display
    Dimmer function
    High voltage drive output (40V)
    On-chip pull-down resistor (Mask option)
    Hardware key scan function (Maximum 16 × 8 key matrix compatible)
  - — Remote control reception circuit 8-bit pulse measurement counter with on-chip 6-stage FIFO
  - — PWM output 14 bits, 1 channel
  - — CTL duty detection circuit
  - — High-speed output circuit Four RTG outputs
- Interruption 19 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 100-pin ceramic QFP

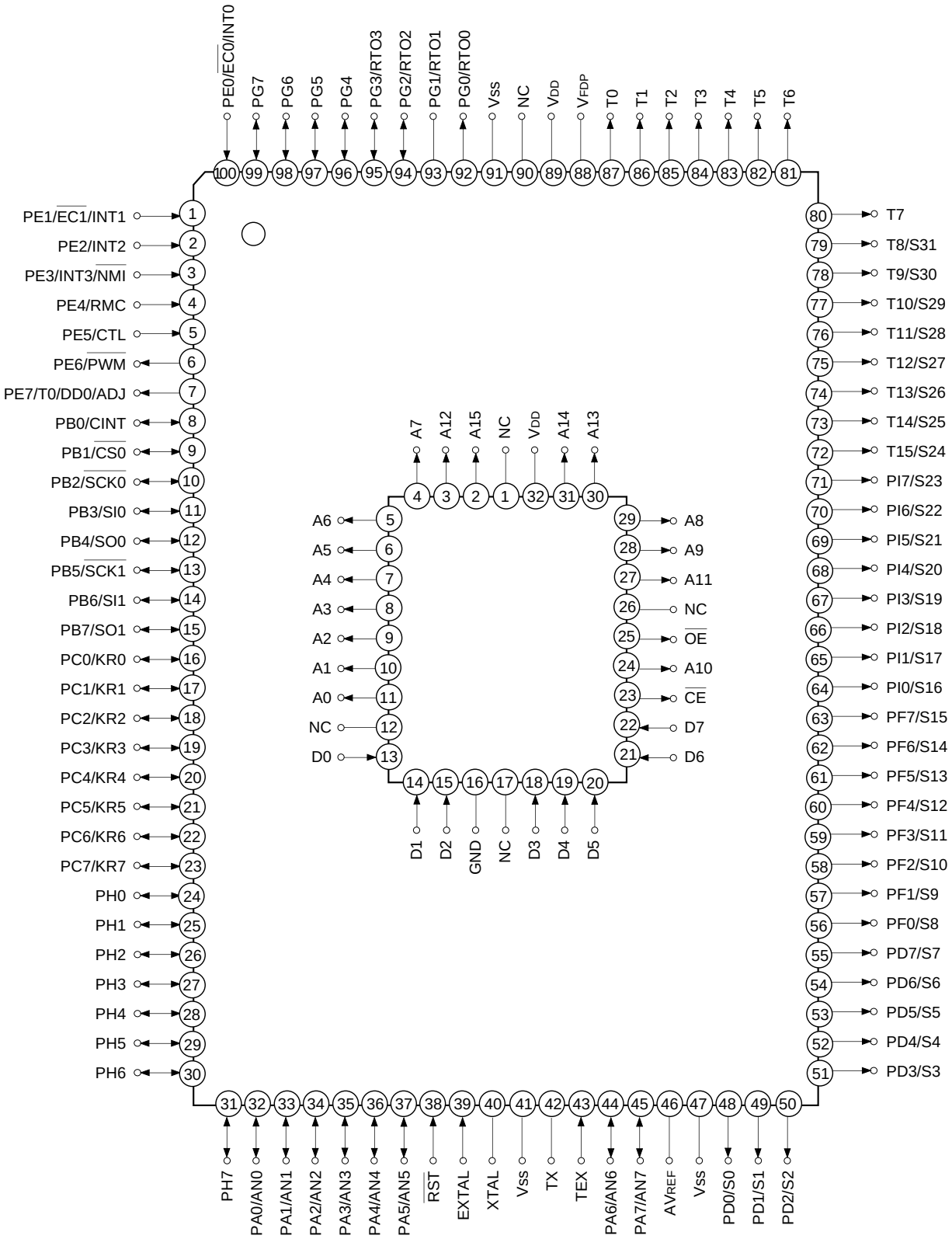
Note) Mask option depends on the type of the CXP82200. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

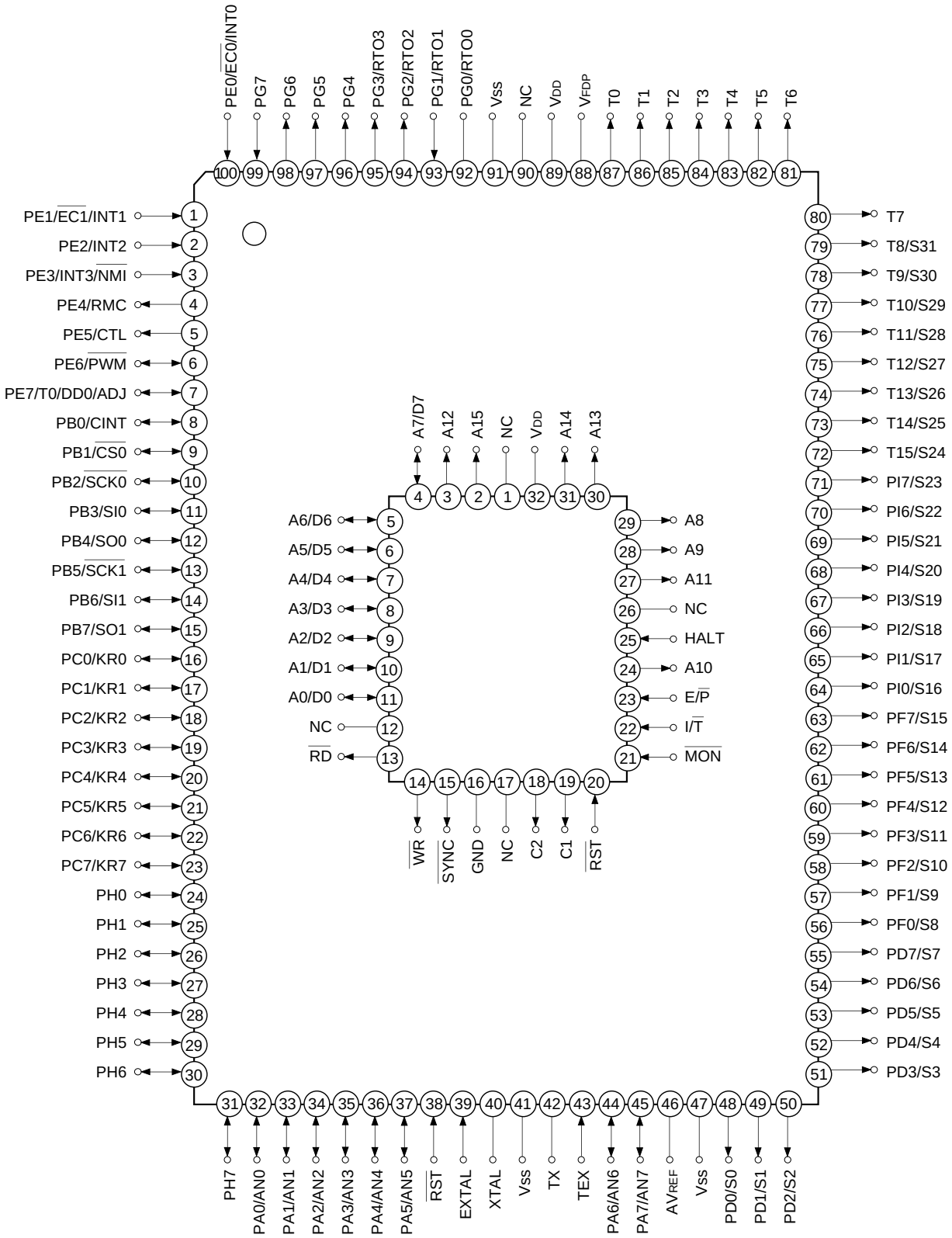
E93847A78-PS

Pin Assignment in Piggyback Mode



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. Vss (Pins 41 and 91) are both connected to GND.

Pin Assignment in Evaluator Mode

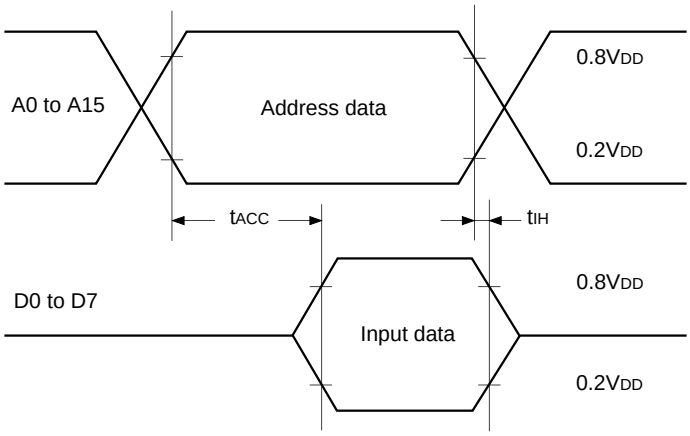


Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. Vss (Pins 41 and 91) are both connected to GND.

EPROM Read Timing

(Ta = –20 to +75°C, Vcc = 4.5 to 5.5V, Vss = 0V reference)

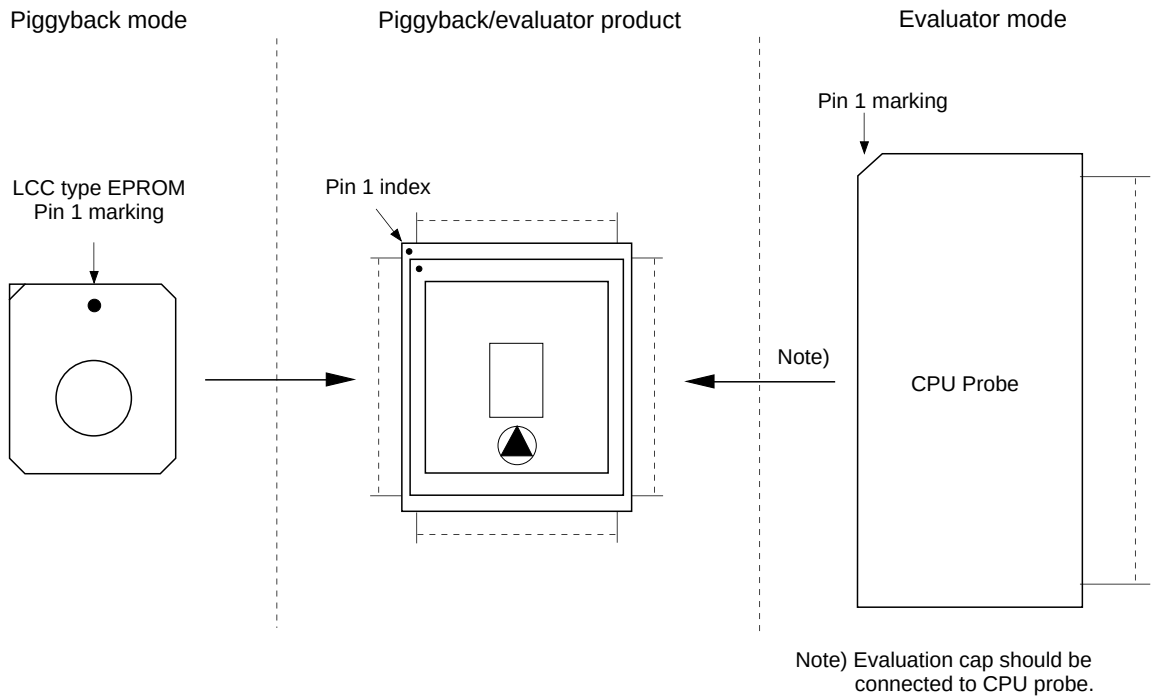
Item	Symbol	Pins	Min.	Max.	Unit
Address → Data Input delay time	t_{ACC}	A0 to A15 D0 to D7		120	ns
Address → Data Hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Products List

Option item	Products		
	Mask		Piggyback/evaluator
	CXP82220	CXP82224	CXP82200-U01Q
Package	100-pin plastic QFP		100-pin ceramic PQFP
ROM capacitance	20K bytes	24K bytes	EPROM 24K bytes
Pull-up resistance for reset pin	Existent/Non-existent		Existent
Power-on reset circuit	Non-existent		Non-existent
Pull-down resistance for high voltage drive pin	Existent/Non-existent		Only port for display

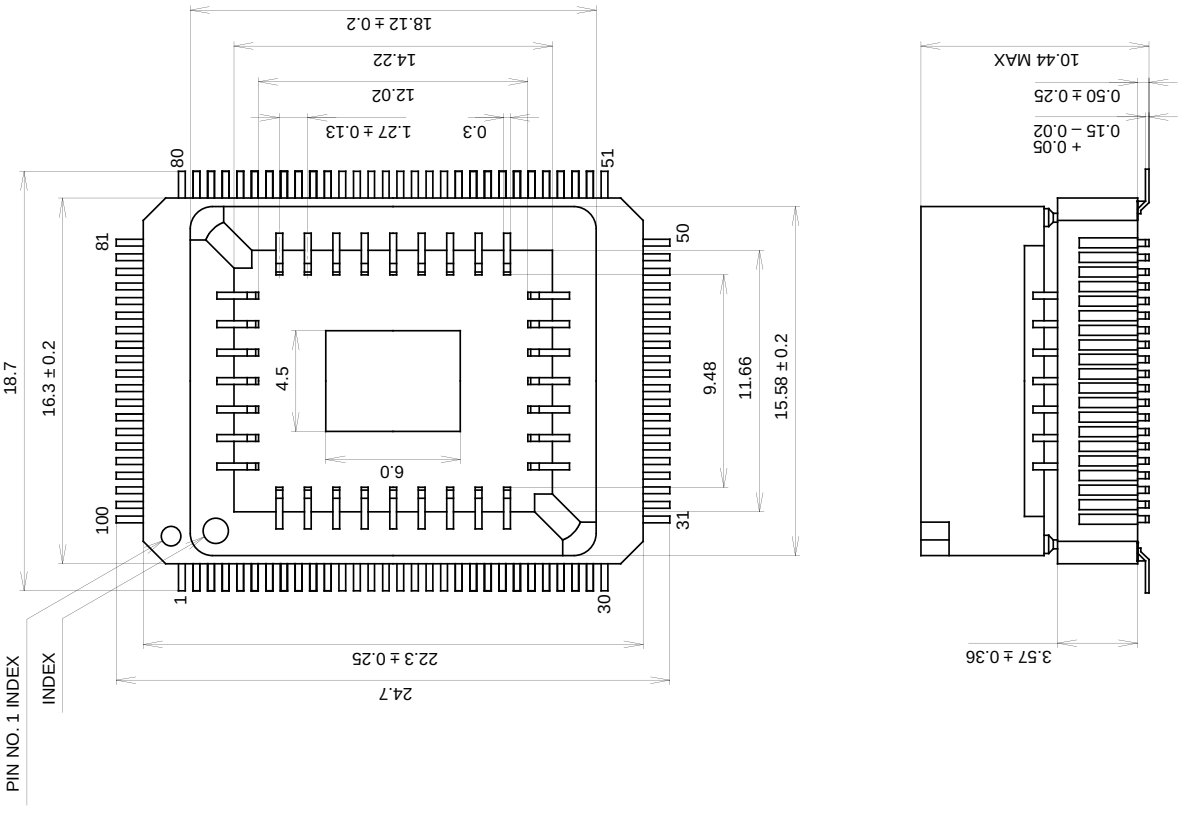
Piggyback mode/evaluator mode can be switched as shown below.

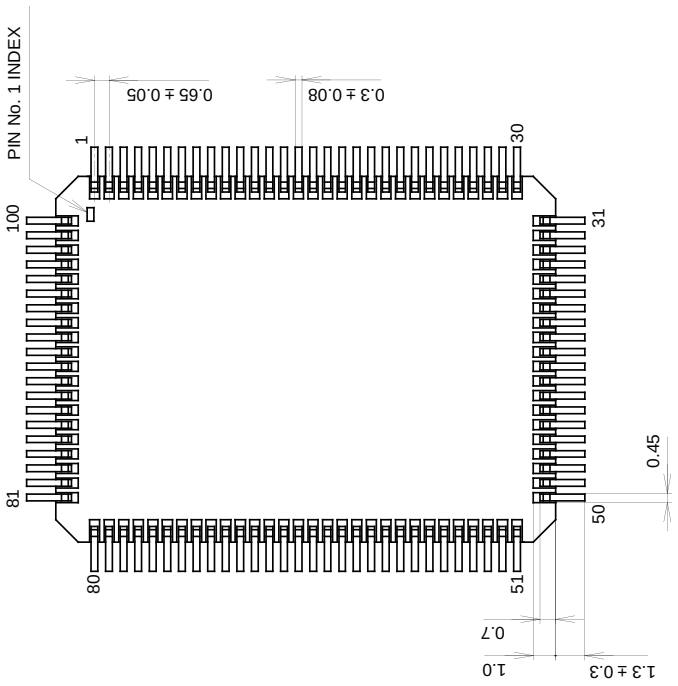


Note) Evaluation cap should be connected to CPU probe.

Package Outline Unit: mm

100PIN PQFP (CERAMIC)





PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	————