N- and P-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

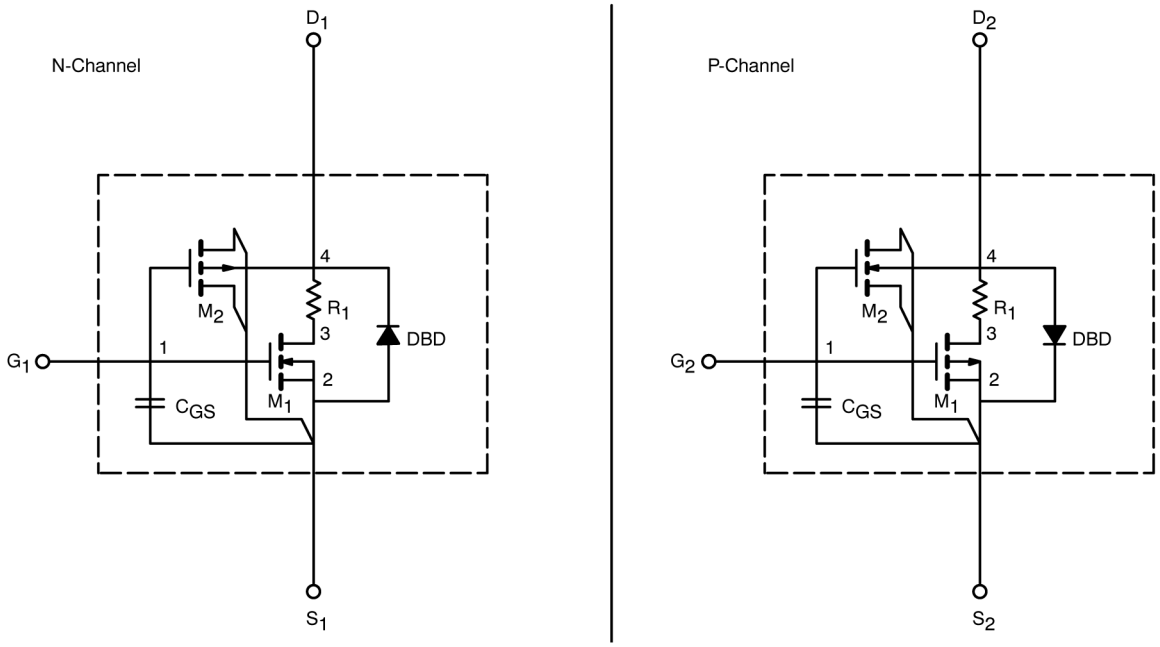
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The model subcircuit schematic is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



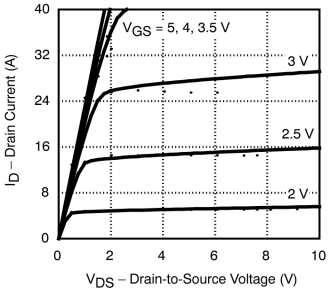
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

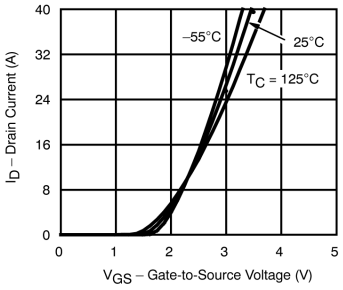
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**		**Typical[a]**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V, V_{GS}, I_D = 250 µA	N-Ch		
		V_{DS} = V, V_{GS}, I_D = –250 µA	P-Ch		
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} V, V_{GS} = V	N-Ch		A
		V_{DS} = – V, V_{GS} = – V	P-Ch		
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 5 A	N-Ch	0.044	Ω
		V_{GS} = –4.5 V, I_D = –3.2 A	P-Ch	.056	
		V_{GS} = 3.0 V, I_D = 3.9 A	N-Ch	0.051	
		V_{GS} = –3.0 V, I_D = –2.0 A	P-Ch	0.084	
		V_{GS} = 2.5 V, I_D = 1 A	P-Ch	0.056	
		V_{GS} = –2.7V, I_D = –1 A	P-Ch	0.096	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 5 A	N-Ch	15	S
		V_{DS} = –9 V, I_D = –3.4 A	P-Ch	9.3	
Diode Forward Voltage[b]	V_{SD}	I_S = 5 A, V_{GS} = 0 V	N-Ch	0.84	V
		I_S = –2 V, V_{GS} = 0 V	P-Ch	–0.74	
Dynamic[a]					
Total Gate Charge	Q_g	N-Channel V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 5 A P-Channel V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –3.2 A	N-Ch	8	nC
			P-Ch	8.9	
Gate-Source Charge	Q_{gs}		N-Ch	2	
			P-Ch	2.1	
Gate-Drain Charge	Q_{gd}		N-Ch	2.4	
			P-Ch	3.3	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} =6 V, R_L = 6 Ω $I_D \cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω P-Channel V_{DD} = –6 V, R_L = 6 Ω $I_D \cong$ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω	N-Ch	24	ns
			P-Ch	12	
Rise Time	t_r		N-Ch	19	
			P-Ch	19	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	30	
			P-Ch	46	
Fall Time	t_f		N-Ch	13	
			P-Ch	60	
			N-Ch	64	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = A, I_S = 1.25A, di/dt = 100 A/µs	P-Ch	53	

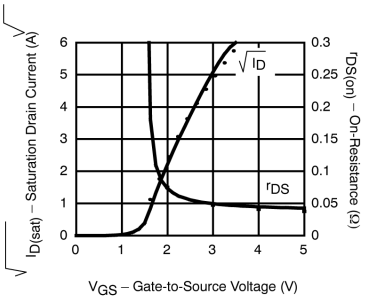
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

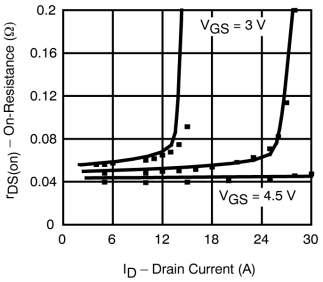
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

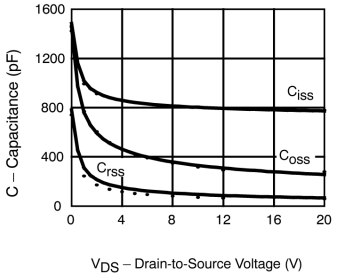
N-Channel

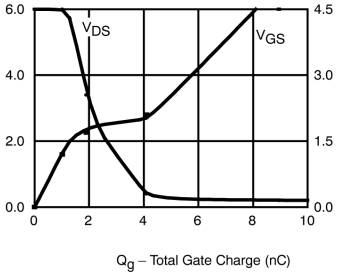






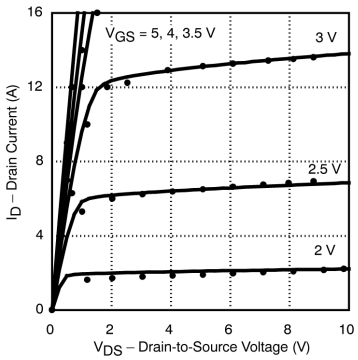


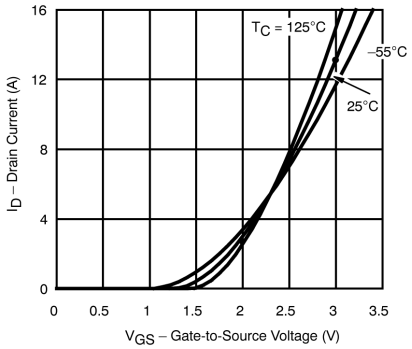


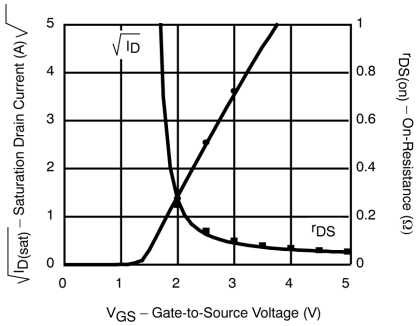


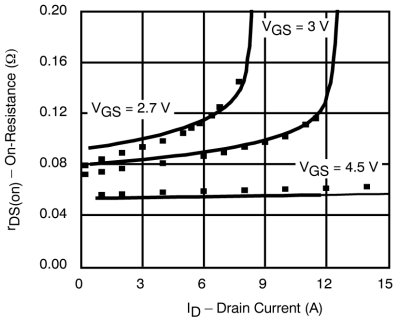
Note: Dots and squares represent measured data.

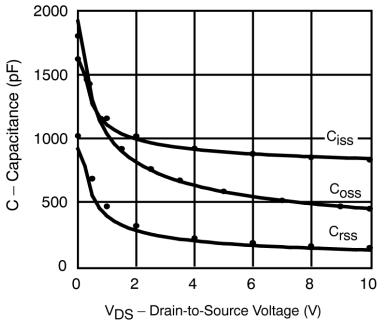
P-Channel

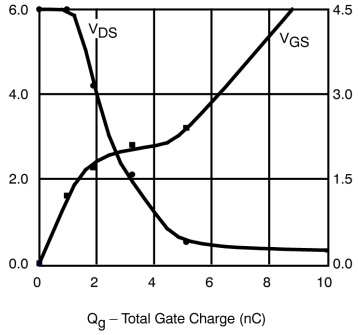












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