Am54S/74S160 • Am54S/74S161 • Am54S/74S163

BCD Decade/Four-Bit Binary Counters

Distinctive Characteristics

- Fully synchronous counting
- Fully synchronous parallel loading
- Edge-triggered clock action
- Advanced Schottky technology
- 100% MIL-STD-883 reliability assurance testi

FUNCTIONAL DESCRIPTION

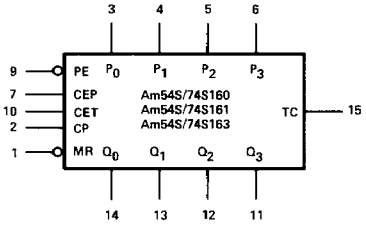
The Am54S/74S160 is a fully synchronous 4-bit decimal counter. The Am54S/74S161 and Am54S/74S163 are fully synchronous 4-bit binary counters. With the parallel enable ($\overline{PE}$) LOW, data on the P_0-P_3 inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is HIGH and both count enables CEP and CET are also HIGH, counting will occur on the LOW-to-HIGH clock transition.

The terminal count state (1001 for the Am54S/74S160 and 1111 for both the Am54S/74S161 and Am54S/74S163) is decoded and ANDed with CET in the terminal count (TC) output. If CET is HIGH and the counter is in its terminal count state, then TC is HIGH.

Both the Am54S/74S160 and Am54S/74S161 have an asynchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW independent of all other inputs.

The Am54S/74S163 has a synchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW after the next clock pulse independent of all other inputs. The only requirements on the $\overline{PE}$, CEP, CET and P_0-P_3 inputs is that they meet the set-up time requirements before the clock LOW-to-HIGH transition.

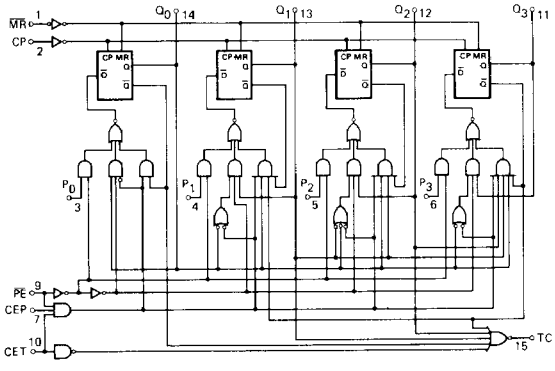
LOGIC SYMBOL



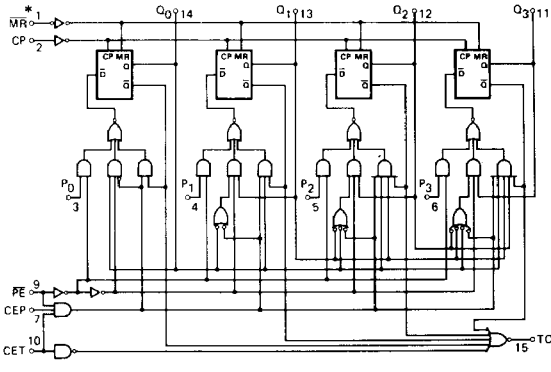
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54S/74S160



Am54S/74S161/S163

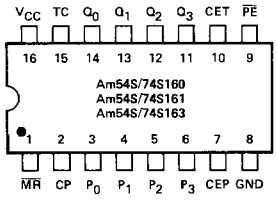


*$\overline{MR}$ is asynchronous on the Am54S/74S161 and synchronous on the Am54S/74S163

ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S160 Order Number	Am54S/74S161 Order Number	Am54S/74S163 Order Number
Molded DIP	0 to +75°C	SN74S160N	SN74S161N	SN74S163N
Hermetic DIP	0 to +75°C	SN74S160J	SN74S161J	SN74S163J
Dice	0 to +75°C	SN74S160X	SN74S161X	SN74S163X
Hermetic DIP	−55 to +125°C	SN54S160J	SN54S161J	SN54S163J
Hermetic Flat Pak	−55 to +125°C	SN54S160W	SN54S161W	SN54S163W
Dice	−55 to +125°C	SN54S160X	SN54S161X	SN54S163X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

AXIMUM RATINGS (Above which the useful life may be impaired)

ɔrage Temperature	−65°C to +150°C
mperature (Ambient) Under Bias	−55°C to +125°C
pply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
ɔ Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
ɔ Input Voltage	−0.5V to +5.5V
ɔ Output Current, Into Outputs	30mA
ɔ Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

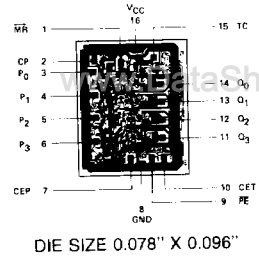
Am74S160X, Am74S161X, Am74S163 T_A = 0 to +75°C V_{CC} = 5.0V ± 5% (COM'L) MIN = 4.75V MAX = 5.25V
Am54S160X, Am54S161X, Am54S163 T_A = −55 to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN = 4.5V MAX = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}			0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	P; MR; CEP			−2.0	mA
			CET			−3.0	
			$\overline{PE}$			−4.0	
			CP			−5.0	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	P; $\overline{MR}$; CEP			50	μA
			CET			75	
			$\overline{PE}$			100	
			CP			125	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX		−40	−65	−100	mA
I_{CC}	Power Supply Current Am54S/74S160/161 only	V_{CC} = MAX (Note 5)			82	127	mA
	Am54S/74S163 only	V_{CC} = MAX (Note 6)			96	150	mA

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; $\overline{MR}$ = 0V; all other inputs HIGH.
6. Outputs open; $\overline{MR}$, CP, CET = HIGH; all other inputs LOW.

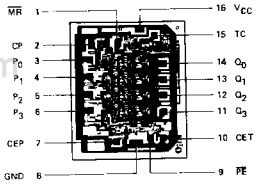
Metallization and Pad Layouts

Am54S/74S160



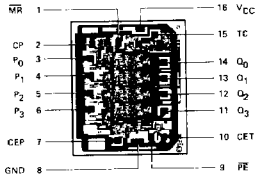
DIE SIZE 0.078" X 0.096"

Am54S/74S161



DIE SIZE 0.092" X 0.076"

Am54S/74S163



DIE SIZE 0.092" X 0.076"

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DEFINITION OF FUNCTIONAL TERMS

$\overline{PE}$ Parallel Enable. When $\overline{PE}$ is LOW, the parallel inputs, P_0 through P_3, are enabled. When $\overline{PE}$ is HIGH, the count function is possible.

CEP Count Enable Parallel. CEP is one of the count enable inputs that must be HIGH for the counter to count.

CET Count Enable Trickle. CET is one of the count enable inputs that must be HIGH for the counter to count. In addition, CET is included in the TC output gate and must be HIGH for TC to be HIGH.

CP Clock Pulse. Causes the required output change on the LOW-to-HIGH transition (Edge-triggered).

$\overline{MR}$ Master Reset (Am54S/74S160/S161). When the asynchronous master reset is LOW, the Q_0 through Q_3 outputs will be LOW regardless of the other inputs.

$\overline{MR}$ Master Reset (Am54S/74S163). When the synchronous master reset is LOW the Q_0 through Q_3 outputs will be LOW following the next clock pulse regardless of the other inputs.

P_0, P_1, P_2, P_3 The parallel data inputs for the four internal flip-flops.

Q_0, Q_1, Q_2, Q_3 The four parallel outputs from the counter.

TC Terminal Count. The terminal count output will be HIGH for CET HIGH and binary nine on the Am54S/74S160 or CET HIGH and binary 15 on the Am54S/74S161.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{MR}$	1	1	–	–
CP	2	2.5	–	–
P_0	3	1	–	–
P_1	4	1	–	–
P_2	5	1	–	–
P_3	6	1	–	–
CEP	7	1	–	–
GND	8	–	–	–
$\overline{PE}$	9	2	–	–
CET	10	1.5	–	–
Q_3	11	–	20	10
Q_2	12	–	20	10
Q_1	13	–	20	10
Q_0	14	–	20	10
TC	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

FUNCTION TABLE

DEVICE TYPE	INPUTS									OUTPUTS			
	CP	$\overline{MR}$	$\overline{PE}$	CEP	CET	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3
Am54S/74S160/S161	X	L	X	X	X	X	X	X	X	L	L	L	L
Am54S/74S163	↑	L	X	X	X	X	X	X	X	L	L	L	L
Am54S/74S160/S161/S163	↑	H	L	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
	↑	H	H	L	L	X	X	X	X	NC	NC	NC	NC
	↑	H	H	L	H	X	X	X	X	NC	NC	NC	NC
	↑	H	H	H	L	X	X	X	X	NC	NC	NC	NC
	↑	H	H	H	H	X	X	X	X	COUNT			

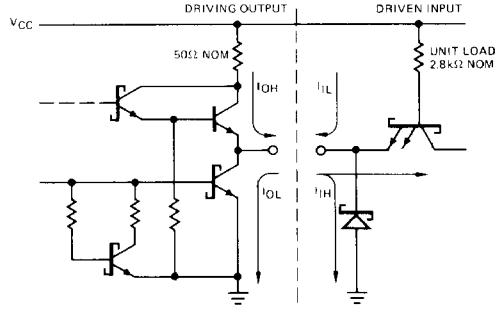
H = HIGH X = Don't Care D_i may be either HIGH or LOW
L = LOW NC = No Change ↑ LOW-to-HIGH Transition

TERMINAL COUNT (TC) TRUTH TABLE

Am54S/74S160					Am54S/74S161/163					TC
CET	Q_0	Q_1	Q_2	Q_3	CET	Q_0	Q_1	Q_2	Q_3	
H	H	L	L	H	H	H	H	H	H	H
L	X	X	X	X	L	X	X	X	X	L
X	L	X	X	X	X	L	X	X	X	L
X	X	H	X	X	X	X	L	X	X	L
X	X	X	H	X	X	X	X	L	X	L
X	X	X	X	L	X	X	X	X	L	L

H = HIGH L = LOW X = Don't Care

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



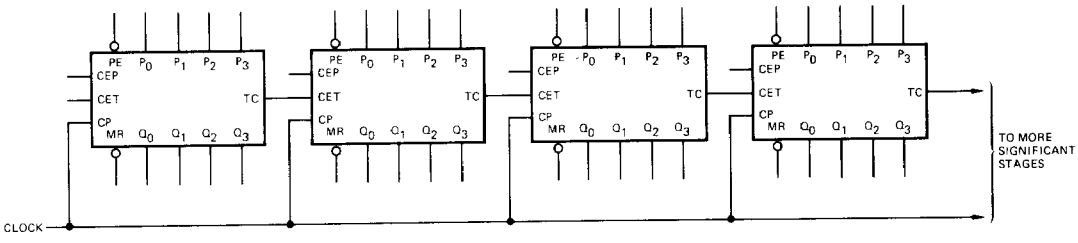
Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS (T_A = +25°)

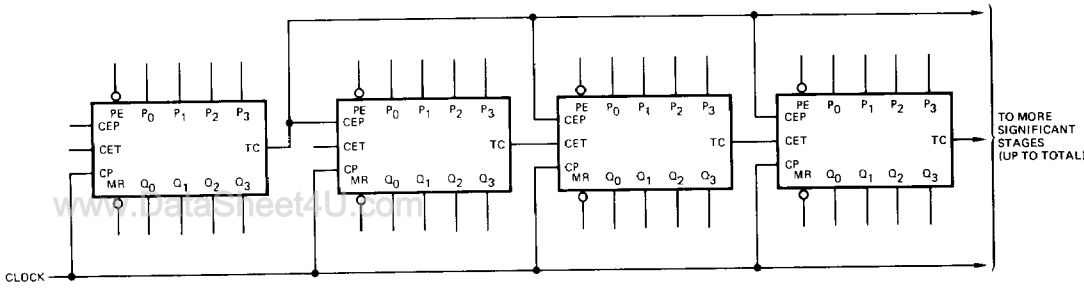
Parameters	Description	Test Conditions	Min	Typ	Max	Units
f_{MAX}	Count Frequency	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω	70	100		MHz
t_{PLH}	Clock to Q			6	9	ns
t_{PHL}				8.5	13	
t_{PLH}	Clock to TC			12	18	ns
t_{PHL}				8	12	
t_{PLH}	CET to TC			6.5	10	ns
t_{PHL}				6.5	10	
t_{PHL}	$\overline{MR}$ to Q (Am54S/74S160/161 only)			14	20	ns
t_s	Recovery Time for MR (inactive) Am54S/74S160 and Am54S/74S161 only		6			ns
t_{pw}	Master Reset Pulse Width		13			ns
t_{pw}	Clock Pulse Width HIGH		6			ns
	Clock Pulse Width LOW		10			
t_s	Data to Clock		8			ns
t_h			0			
t_s	$\overline{PE}$ to Clock		16			ns
t_h			0			
t_s	CEP or CET to Clock		12			ns
t_h			0			
t_s	$\overline{MR}$ to Clock Am54S/74S163 only		14			ns
t_h			0			

APPLICATIONS

SYNCHRONOUS MULTISTAGE COUNTING USING CET INPUT ONLY



FASTER SYNCHRONOUS MULTISTAGE COUNTING USING CET AND CEP INPUTS



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