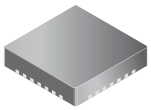
LED Backlight Driver for LCD Monitors and Televisions

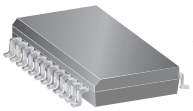
Features and Benefits

- Six integrated high current sinks
- Fixed frequency current mode control with integrated gate driver
- 300 kHz to 1 MHz adjustable switching frequency
- Controlled startup using options of Enable, PWM signal, or battery voltage ramp
- Parallel operation with one boost controller (master) and up to five slave controllers
- Active current sharing between LED strings for ±0.6% accuracy and matching
- No audible MLCC noise during PWM dimming
- Adjustable overvoltage protection (OVP)
- Open or shorted LED string protection
- Overtemperature, cycle-by-cycle current limit, and undervoltage protection
- SOIC 24-pin package for easy single-side PCB manufacturing, or TSSOP 24-pin and QFN 28-contact packages with exposed thermal pad for better thermal performance

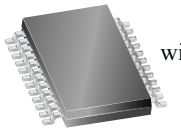
Packages:



28-contact QFN
with exposed thermal pad
(ET Package)



24-pin SOICW
with internally fused pins
(LB package)



24-pin TSSOP
with exposed thermal pad
(LP package)

Not to scale

Description

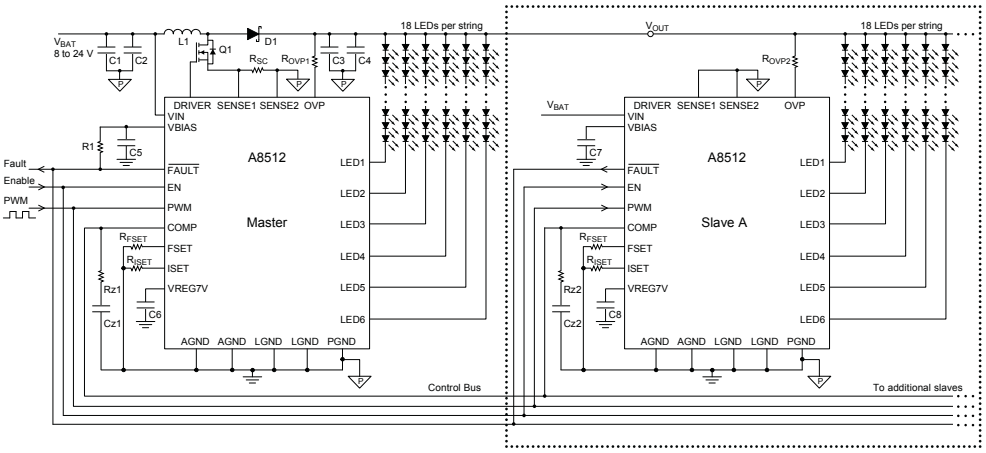
The A8512 is a multi-output WLED/RGB driver for backlighting LCD monitors and televisions. It integrates a boost controller to drive external MOSFET, and six internal current-sinks. The boost converter operates in constant frequency (programmable) current mode control.

PWM dimming allows LED currents to be controlled in 500:1 ratio. The LED sink current is set by an external R_ISET resistor (see chart below). More than one LED sinks can be combined together to achieve even higher current per LED string. Multiple A8512s can be connected in parallel, with one master controller controlling the boost stage, and up to five slave controllers, which act as LED sinks. This allows up to 36 LED strings to be powered by just one boost converter.

The A8512 operates from a single supply of 8 to 24 V. It provides protection against overvoltage, open or shorted LED string, and overtemperature. A dual level cycle-by-cycle current limit function provides soft start and protects against overloads.

The device is provided in a 24-pin SOICW package (LB), with internally fused pins for enhanced thermal dissipation, and a 28-contact 5 mm × 5 mm QFN package (ET) and a 24-pin TSSOP package (LP), both with an exposed thermal pad for enhanced thermal dissipation. All packages are lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application Circuit



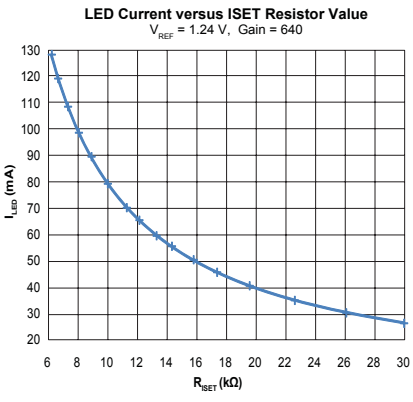


Figure 1. Typical application circuit for single IC operation, and (in dotted box) master/slave multiple IC operation.

Selection Guide

Part Number	Packing	Package
A8512ELBTR-T	1000 pieces per 13-in. reel	24-pin SOICW, with internally fused pins for enhanced thermal dissipation
A8512ELPTR-T	4000 pieces per 13-in. reel	24-pin TSSOP, with exposed thermal pad for enhanced thermal dissipation
A8512EETTR-T	1500 pieces per 7-in. reel	28-contact QFN, with exposed thermal pad for enhanced thermal dissipation

Absolute Maximum Ratings

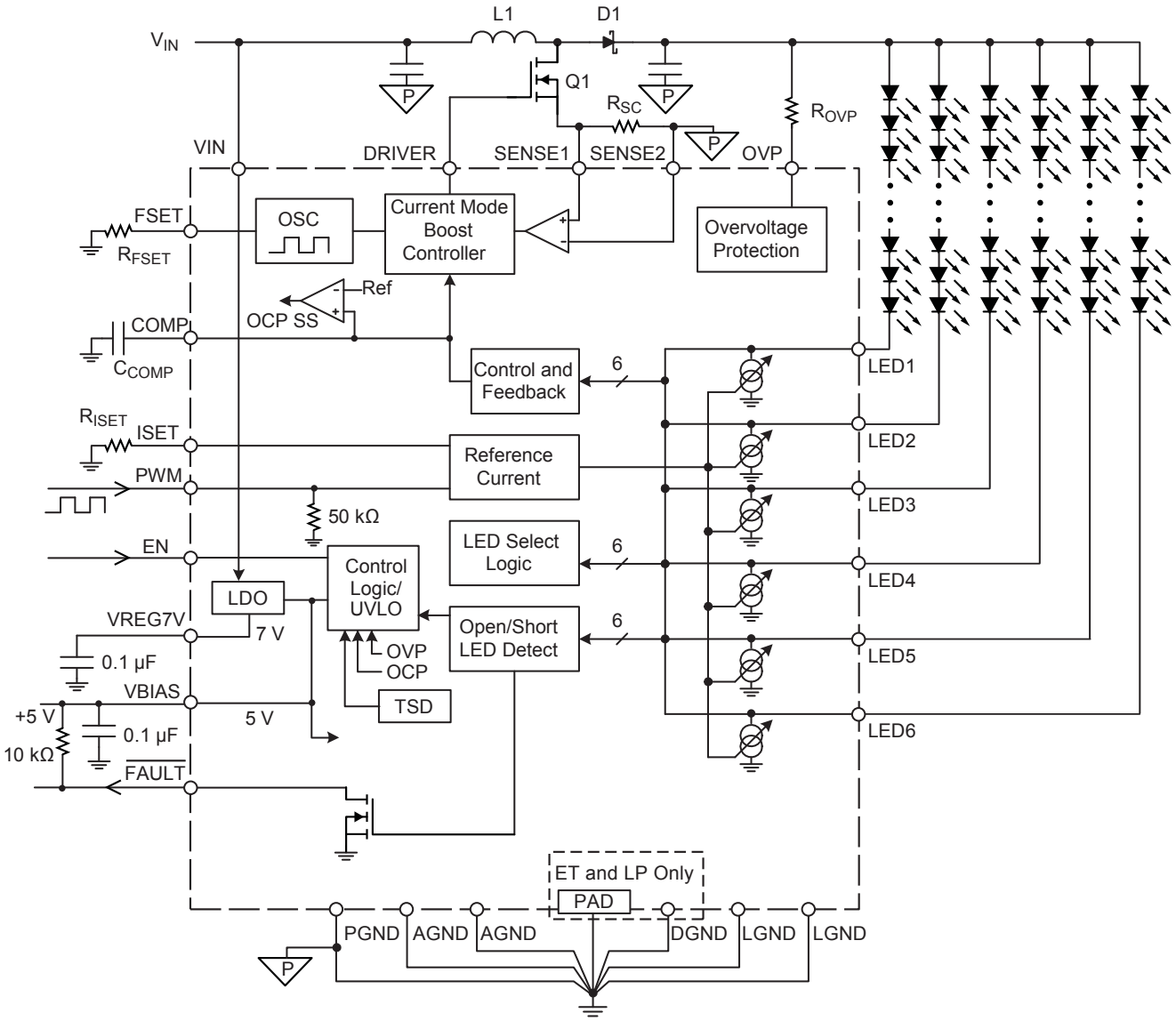
Characteristic	Symbol	Notes	Rating	Unit
VIN Pin Input Voltage	V_{IN}		–0.3 to 34	V
LED1-LED6 Pin Voltage	V_{LEDx}		–0.3 to 40	V
OVP Pin Input Voltage	V_{OVP}		–0.3 to 50	V
SENSE1 and SENSE2 Pin Input Voltage	V_{SENx}		–0.3 to 1	V
VBIAS, VREG7V, and DRIVER Pins			–0.3 to 10	V
Remaining Pins Input Voltage			–0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

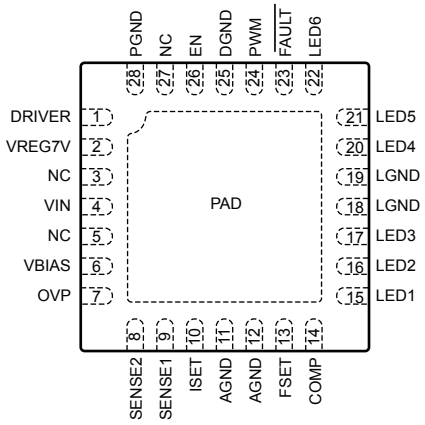
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package ET, 4-layer PCB, based on JEDEC standard	32	ºC/W
		Package LB, on 2-layer PCB, 1-in² 2-oz copper exposed area	51	ºC/W
		Package LB, on 4-layer PCB, based on JEDEC standard	35	ºC/W
		Package LP, on 4-layer PCB, based on JEDEC standard	28	ºC/W

*Additional thermal information available on the Allegro website

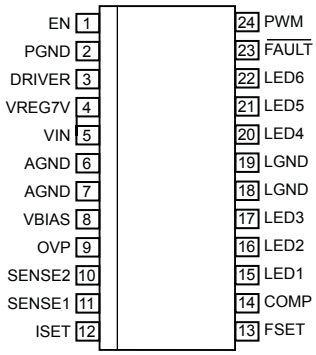
Functional Block Diagram



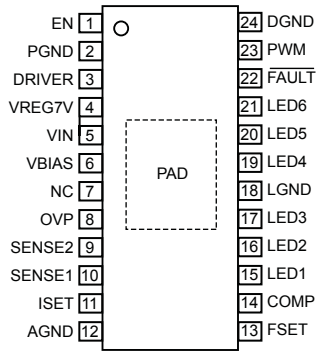
Pin-out Diagrams



Package ET



Package LB



Package LP

Terminal List Table

Number			Name	Function
ET	LB	LP		
26	1	1	EN	Device Enable. Apply logic-high signal to enable, low to shut down.
28	2	2	PGND	Power ground for external FET gate driver. Connect directly to R_{SC} ground and to common star ground.
1	3	3	DRIVER	Gate driver terminal to drive external MOSFET.
2	4	4	VREG7V	Gate driver supply from internal voltage regulator. Bypass with 0.1 to 1 µF ceramic capacitor to PGND.
4	5	5	VIN	Input supply voltage for the IC.
11, 12	6, 7	12	AGND	Analog (signal) GND for the IC. Connect to common star ground.
6	8	6	VBIAS	Bias supply voltage from internal regulator. Bypass with 0.1 to 1 µF ceramic capacitor to AGND
7	9	8	OVP	Overvoltage Protection terminal. Connect this pin to output capacitor through a resistor R_{OVP} to set the OVP threshold.
8	10	9	SENSE2	Connect to ground side of current sense resistor R_{SC}.
9	11	10	SENSE1	Connect to high side of current sense resistor R_{SC}.
10	12	11	ISET	Sets 100% Current through LED strings; connect R_{ISET} from ISET to AGND.
13	13	13	FSET	Sets switching frequency; connect R_{FSET} from FSET to AGND.
14	14	14	COMP	Compensation pin; connect C_{COMP} (1 µF typical) capacitor to AGND.
15,16,17	15,16,17	15,16,17	LED1-3	LED current sinks; connect unused LEDx pins to ground to disable.
18,19	18,19	18	LGND	LED current sink ground; connect to common star ground.
20,21,22	20,21,22	19,20,21	LED4-6	LED current sinks; connect unused LEDx pins to ground to disable.
23	23	22	$\overline{\text{FAULT}}$	This open-drain output is pulled low when fault condition occurs; connect to external pull-up resistor.
24	24	23	PWM	Pulse width modulation LED-current control; apply logic level PWM for dimming.
25	–	24	DGND	Digital ground for input control signals (EN and PWM); connect to common star ground.
3,5,27	–	7	NC	Not connected electrically.
PAD	–	PAD	PAD	Exposed pad. Solder to GND plane for enhanced thermal dissipation.

ELECTRICAL CHARACTERISTICS Valid at V_{IN} = 12 V; T_A = 25°C, R_{FSET} = 52 kΩ, R_{ISET} = 12.4 kΩ, except • indicates specifications guaranteed over the full operating temperature range with $T_A = T_J$, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit
Input Voltage Range	V_{IN}		•	8	–	24	V
Internal Bias Voltage Range	V_{BIAS}			4.75	–	5.5	V
Internal Gate Driver Voltage	V_{DRIVER}	V_{IN} ≥ 10 V		6.5	–	8	V
Undervoltage Lockout Threshold for V_{IN}	V_{UVLO}	V_{IN} falling	•	5.7	6.5	6.8	V
Undervoltage Lockout Hysteresis for V_{IN}	$V_{UVLOHYS}$			–	0.55	–	V
Supply Current[2]	I_{VIN}	Switching at no load		–	7	–	mA
		Shutdown, EN = V_{IL}, T_A = 25°C		–	0.1	1	µA
		Standby, EN = V_{IH}, PWM = V_{IL}, soft start completed	•	–	2	3	mA
Boost Controller							
Switching Frequency	f_{SW}		•	0.8	1	1.25	MHz
Minimum Switch Off-Time	$t_{off(min)}$	Driver output		–	72	–	ns
Minimum Switch On-Time	$t_{on(min)}$	Driver output		–	72	–	ns
Logic Input Levels (EN and PWM pins)							
Input Voltage Level Low	V_{IL}		•	–	–	0.4	V
Input Voltage Level High	V_{IH}		•	1.5	–	–	V
Input Leakage Current[2]	I_{IN}	EN = PWM = 5 V		–	100	–	µA
Error Amplifier							
COMP Pin Source Current	$I_{EA(src)}$	V_{COMP} = 1.5 V		–	160	–	µA
COMP Pin Sink Current	$I_{EA(snk)}$	V_{COMP} = 1.5 V		–	20	–	µA
COMP Pin Pull-Down Resistance	R_{COMPPD}	$\overline{FAULT}$ = 0		–	1000	–	kΩ
Driver Section							
Peak Source Current[5]	$I_{pk(src)}$	Measured at V_{DRIVER} = 0 V		–	2	–	A
Peak Sink Current[5]	$I_{pk(snk)}$	Measured at V_{DRIVER} = V_{REG7V}		–	2	–	A
High Side Gate Drive On Resistance	$R_{DS(on)H}$	Measured at V_{DRIVER} = V_{REG7V} / 2		–	4	–	Ω
Low Side Gate Drive On Resistance	$R_{DS(on)L}$	Measured at V_{DRIVER} = V_{REG7V} / 2		–	3	–	Ω
Sense Overcurrent Threshold Voltage	V_{SEN}	$V_{SENSE1} - V_{SENSE2}$		80	95	110	mV
LED Current Sinks							
LEDx Pin Regulation Voltage	V_{LEDx}	I_{LED} = 80 mA		–	1.4	–	V
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	I_{SET} = 100 µA		–	640	–	A/A
ISET Pin Voltage	V_{ISET}			–	1.235	–	V
I_{SET} Allowable Current Range[2]	I_{SET}		•	41	–	190	µA

Continued on the next page…

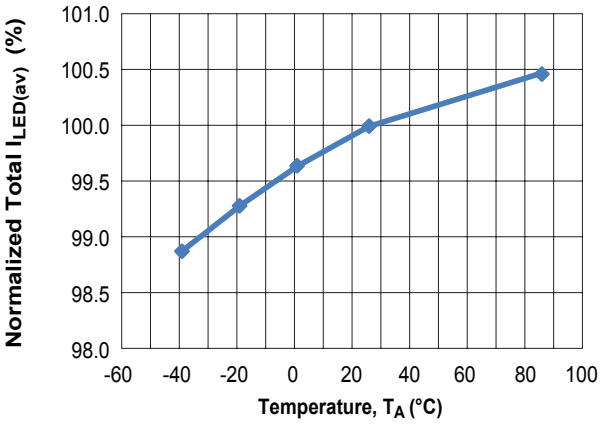
ELECTRICAL CHARACTERISTICS (continued) Valid at V_{IN} = 12 V; T_A = 25°C, R_{FSET} = 52 kΩ, R_{ISET} = 12.4 kΩ, except • indicates specifications guaranteed over the full operating temperature range with $T_A = T_J$, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit
LEDx Accuracy[3]	Err_{ILEDX}	LED1 through LED6 = 1.5 V, at 100% Current		–3	±0.6	3	%
LEDx Matching[4]	ΔI_{LEDX}	LED1 through LED6 = 1.5 V, I_{SET} = 100 µA		–3	±0.6	3	%
LEDx Switch Leakage Current[2]	I_{SL}	V_{LEDx} = 12 V, EN = 0		–	48	–	µA
LEDx Bleeder Resistor to GND	R_{LEDX}	PWM = Low, V_{LEDx} = 10 V		–	250	–	kΩ
Soft Start							
Soft Start Sense Threshold Voltage	V_{SENS}	Sense voltage for boost switch current sensing		–	28.5	–	mV
Soft Start LEDx Current Limit Relative to LED 100% Current	$I_{LED(SS)}$	Current through enabled LEDx pins during soft start		–	8	–	%
Protection Features							
Thermal Shutdown Threshold	T_{TSD}	T_J rising		–	165	–	°C
Short Circuit Detect Voltage	V_{SC}	Measured on any LEDx pin		–	25	–	V
Output Overvoltage Threshold	V_{OVP}	R_{OVP} = 0		18.0	19.5	21.0	V
OVP Pin Leakage Current[2]	I_{OVPLK}	V_{OVP} = 22 V, EN = V_{IL}, or PWM=V_{IL}		–	0.1	–	µA
Overvoltage Protection Sense Current[2]	I_{OVPH}			183	200	217	µA
$\overline{\text{FAULT}}$ Pin Output Leakage[2]	I_{FLT}	V = 5 V		–	–	1	µA
$\overline{\text{FAULT}}$ Pin Output Voltage	V_{OL}	I = 500 µA	•	–	–	0.4	V

[1]Typical specifications are at T_A = 25ºC.
[2]For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[3]LED accuracy is defined as (I_{SET} × 640 – I_{LED}(av)) / (I_{SET} × 640), I_{LED}(av) measured as the average of I_{LED1} through I_{LED6}. Refer to characterization chart for variation over temperature range.
[4]LED current matching is defined as (I_{LEDx} – I_{LED}(av)) / I_{LED}(av), with I_{LED}(av) as defined in footnote 3. Refer to characterization chart for variation over temperature range.
[5]Guaranteed by design and characterization.

Variation of Total LED Current versus Ambient Temperature

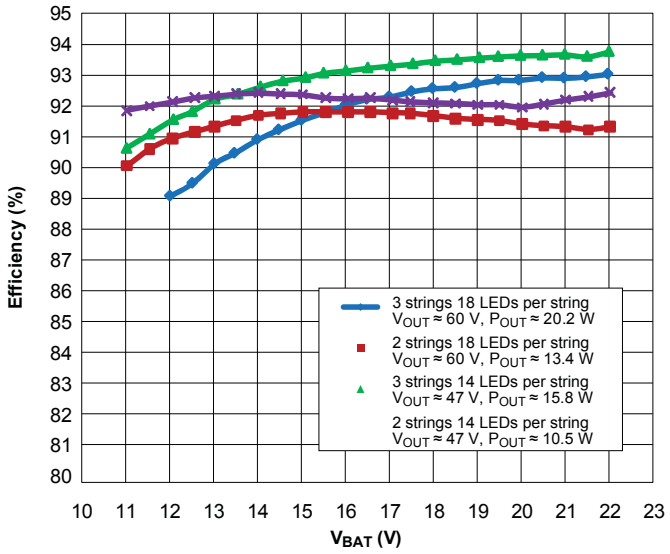
100% Current = 64 mA per channel at 25°C



Characteristic Performance

Efficiency versus Battery Voltage for Various LED Configurations

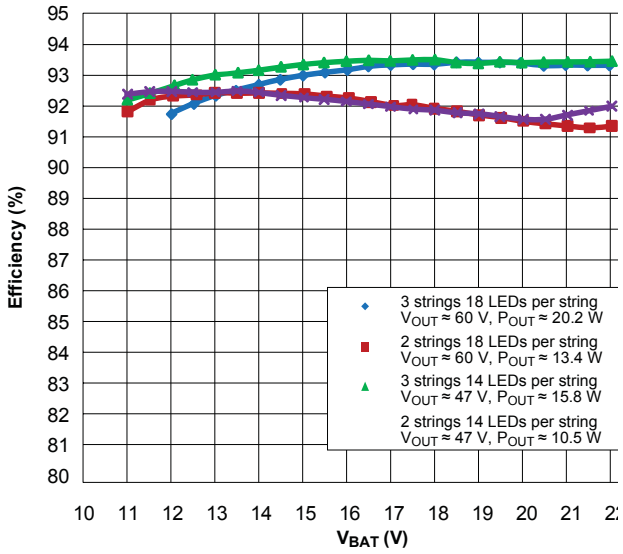
FET = IRFR120N, V_{IN} = 12 V, f_{SW} = 500 kHz
L = 22 µH, Load = W92050C LEDs at 112 mA per string



Efficiency of the boost converter stage is affected by the selection of power MOSFET, switching frequency, input/output voltages, and output power. The external MOSFET used for the above chart is the IRFR120N, which has a relatively high $R_{DS(on)}$ = 0.21 Ω. This causes higher conduction loss, especially at lower input voltage.

Efficiency versus Battery Voltage for Various LED Configurations

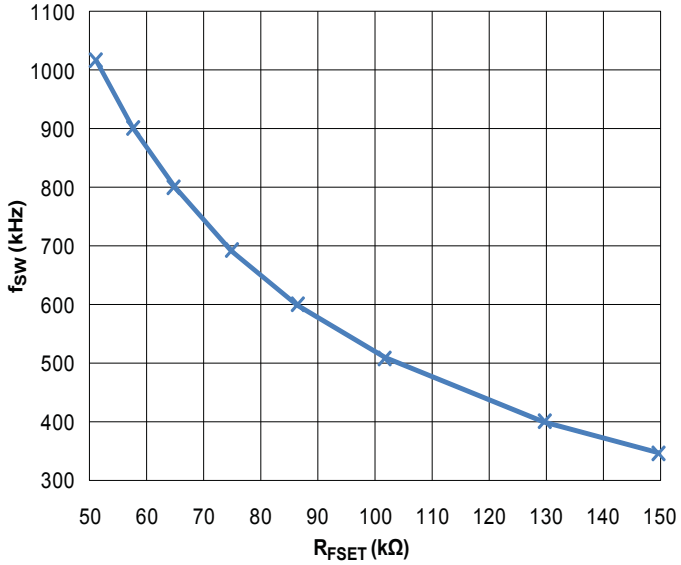
FET = FQB17N08L, V_{IN} = 12 V, f_{SW} = 500 kHz
L = 22 µH, Load = W92050C LEDs at 112 mA per strin



The power MOSFET is replaced with FQB17N08L, which has a lower $R_{DS(on)}$ = 0.115 Ω. This results in less conduction loss at lower input voltage, however, the switching loss becomes more significant at higher input voltage.

Switching Frequency versus FSET Resistor Value

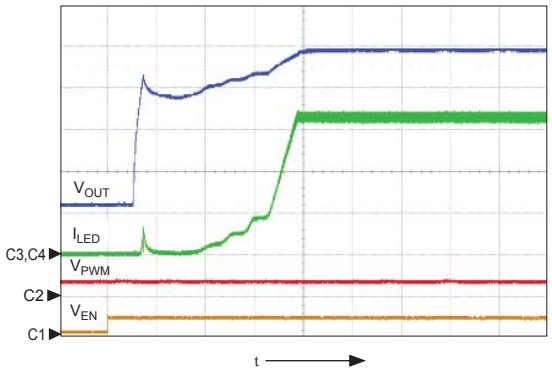
f_{SW} (MHz) = 52 / R_{FSET} (kΩ)



Normal Startup Power Sequences

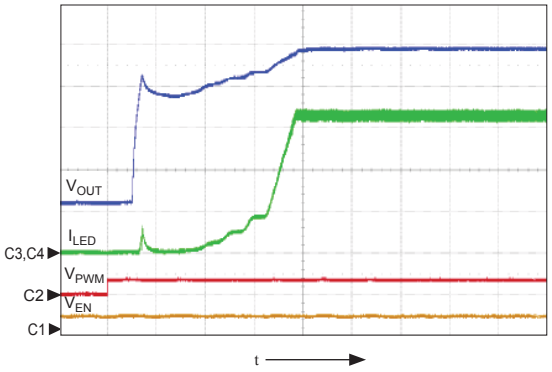
V_{BAT} = 12 V, Load = 6 strings, 16 LEDs each string, 56 mA per string, Output capacitors = 2 × 2.2 µF ceramic

The A8512 can startup with any combination of input and power sequences, as shown in waveforms below:



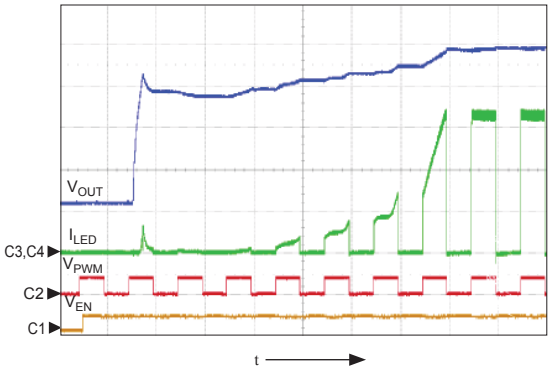
Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{PWM}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

Normal startup with EN = Low-to-High transition (PWM = High)



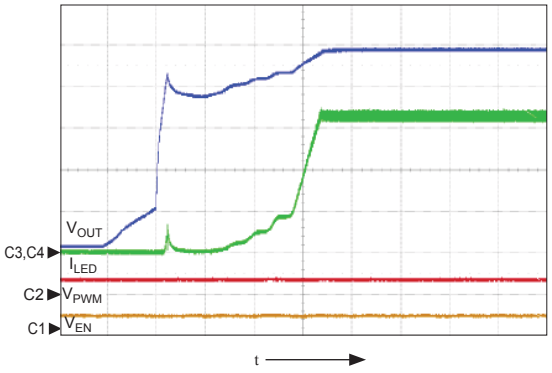
Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{PWM}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

Normal startup with PWM = Low-to-High transition (EN = High)



Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{PWM}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

Normal startup with PWM signal toggling at 500 Hz, 50% duty cycle

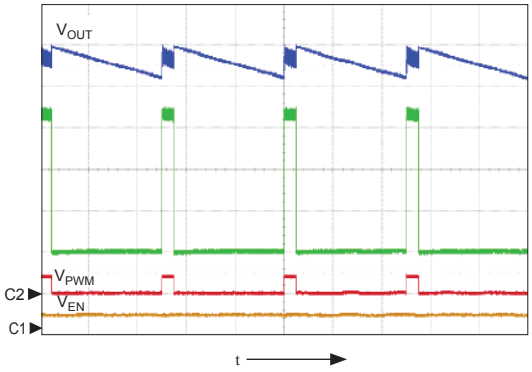


Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{PWM}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

Normal startup with battery voltage ramping up from 2 to 12 V (EN= PWM = High)

Typical PWM Operation Waveforms

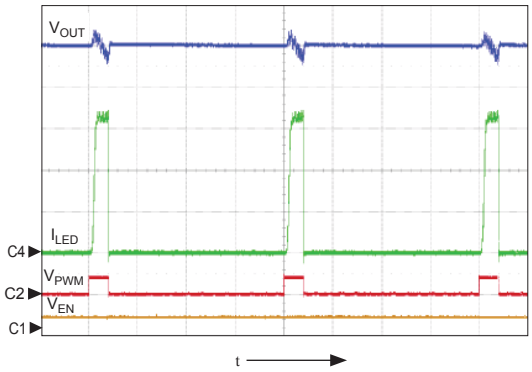
V_{BAT} = 12 V, Load = 6 strings, 16 LEDs each string, 56 mA per string, Output capacitors = 2 × 2.2 µF ceramic



Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{PWM}	10 V
–*	V_{OUT}	1 V
C4	Total I_{LED}	100 mA
t	time	2 ms

*Offset = 46 V

PWM dimming at 200 Hz 10% duty cycle;
Output voltage ripple approximately 0.8 V (out of 50 V)



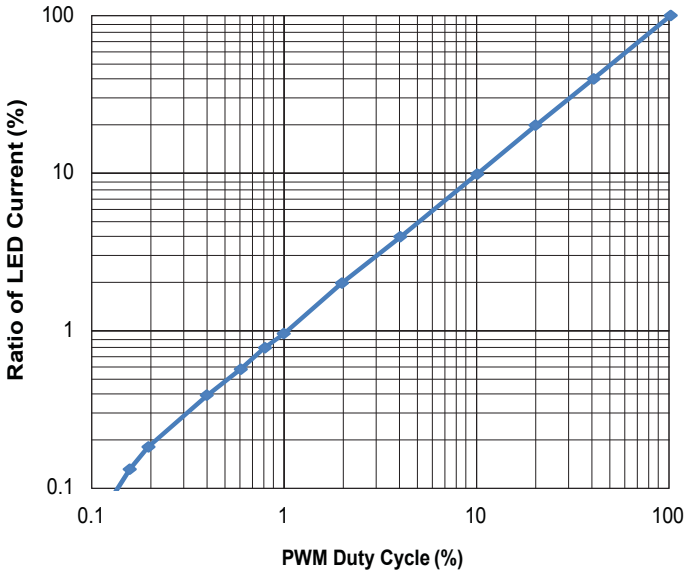
Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{PWM}	10 V
–*	V_{OUT}	1 V
C4	I_{LED}	100 mA
t	time	50 µs

*Offset = 46 V

PWM dimming at 5 kHz 10% duty cycle

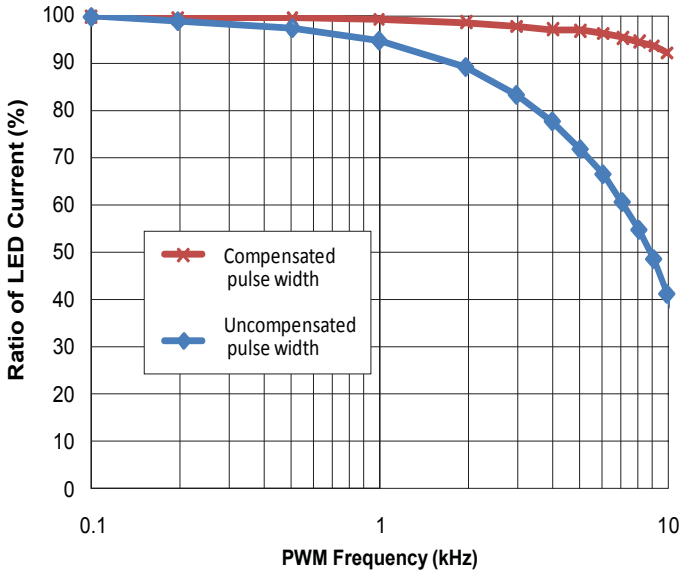
Ratio of LED Current versus PWM Duty Cycle

PWM frequency = 200 Hz



Ratio of LED Current versus PWM Frequency

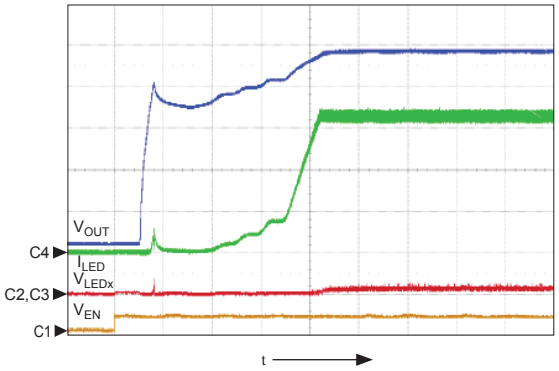
PWM duty cycle = 10%



To improve the accuracy of PWM dimming at very high frequency and/or very low duty cycle, it is necessary to compensate the PWM pulse width, as described in Application Information section.

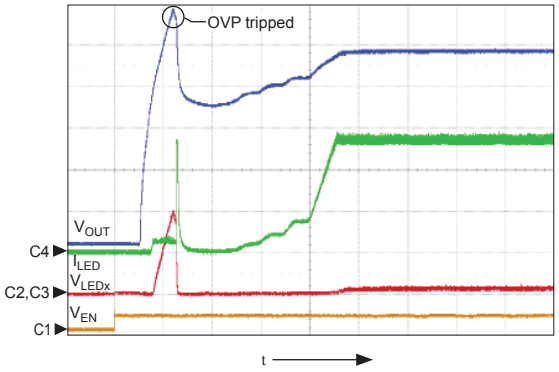
Normal Operation and Fault Conditions

V_{BAT} = 12 V, Load = 6 strings, 18 LEDs each string, 56 mA per string, Output capacitors = 2 × 2.2 µF ceramic, ROVP = 249 kΩ (OVP at 69 V)



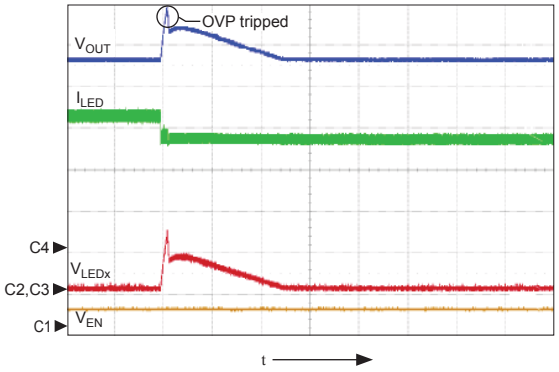
Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{LEDx}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

Normal startup with V_{BAT} = 12 V, (V_{OUT} ≈ 58 V when cold)



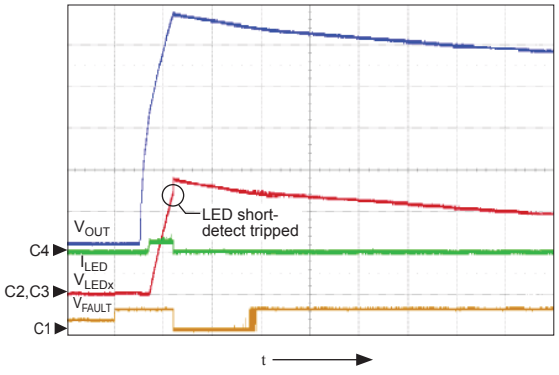
Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{LEDx}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

Startup with one LED string open; (OVP tripped at ≈69 V. Open string removed from regulation. Remaining strings operate normally.)



Symbol	Parameter	Units/Division
C1	V_{EN}	10 V
C2	V_{LEDx}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

Startup with all LED strings connected, then one LED string becomes open; (OVP tripped at ≈69 V. Open string removed from regulation. Remaining strings operate normally)



Symbol	Parameter	Units/Division
C1	V_{FAULT}	10 V
C2	V_{LEDx}	10 V
C3	V_{OUT}	10 V
C4	Total I_{LED}	100 mA
t	time	2 ms

OVP setpoint too high for the application. Startup with one string open; voltage at LEDx pin exceeded Short-Detect threshold (25 V) before OVP could be tripped. IC shuts down.

Functional Description

Overview The A8512 is a multi-output WLED/RGB controller for backlighting medium-size displays. It has an integrated gate driver for driving an external N-channel boost MOSFET. The gate driver voltage is regulated at 7 V, which allows a wide selection of power MOSFET (in contrast to being limited to logic-level MOSFETs when using a 5 V gate driver). The boost controller operates in fixed-frequency current-mode control. The switching frequency can be set in the range from 300 kHz to 1 MHz, by an external resistor, R_{FSET}, connected between FSET and ground.

The external MOSFET switch is protected by pulse-by-pulse current limiting. The current limit is independent of duty cycle, and is set using an external sense resistor, R_{SC}.

The A8512 has six well-matched current sinks that provide regulated current through the LEDs for uniform display brightness. The boost converter is controlled by monitoring all LEDx pins simultaneously and continuously.

Multiple A8512 can be connected in parallel, for applications that require more than six LED strings. One master controller is in charge of the boost converter stage, while other slave controllers act as LED current sinks only. The converter output voltage will be boosted to a level just sufficient for all LED currents to be within regulation.

Up to six A8512s (1 master + 5 slaves) can be connected in parallel, which allows up to 36 LED strings to be powered by just one boost converter. The maximum number of LEDs within each string is limited only by the voltage ratings of the external power components (MOSFET, diode, and capacitors).

LED Current Setting The maximum LED current can be set, at up to 130 mA/channel, through the ISET pin. Connect a resistor, R_{ISET}, between this pin and ground to set the reference current level, I_{SET}. The value of I_{SET} (mA) is determined by:

$$I_{SET} = 1.235 / R_{ISET}\,(k\Omega) \quad . \qquad (1)$$

The resulting current is multiplied internally with a gain of 640 and mirrored on all enabled LEDx pins:

$$I_{LED} = I_{SET} \times 640 \quad . \qquad (2)$$

This sets the maximum current through each LEDx, referred as the *100% Current*. The LEDx current can be reduced from the 100% Current value by applying an external PWM signal on the PWM pin. Conversely, we can calculate R_{ISET} according to the LED current required:

$$R_{ISET} = (1.235 / I_{LED}) \times 640 \quad . \qquad (3)$$

In steady-state operation, the maximum average LED current that can be handled by the IC depends on its thermal budget. That is, maximum power dissipation and acceptable temperature rise. The thermal budget is affected by various parameters, such as PCB size, copper plane around IC, LED V_f mismatch, selection of power components (MOSFET, inductor and diode), maximum board temperature, and so on.

Boost Switching Frequency Setting Connect an external resistor between the FSET pin and GND, to set boost switching frequency, f_{SW} . The value of f_{SW} (MHz) is determined by:

$$f_{SW} = 52 / R_{FSET} \quad , \qquad (4)$$

where f_{SW} is in MHz and R_{FSET} is in kΩ. The typical range of R_{FSET} is approximately 51 to 174 kΩ, which corresponds to 1 MHz to 300 kHz.

Enable The IC turns on when a high signal is applied on the EN pin, and turns off when this pin is pulled low. The LED current sinks are turned on when both the EN and the PWM inputs are high.

Channel Selection The A8512 can be used to drive 1 to 6 LED channels. During startup, the IC detects LED sink pins which are shorted to ground, and disables the corresponding LED channel. Therefore, any unused LED pins must be connected to ground, otherwise the IC will go into overvoltage protection fault during startup. LED pins can be paralleled together for higher current. For example for a 3 parallel string configuration, connect LED1-2, LED3-4, and LED5-6 together to deliver up to twice the current per LED.

PWM Dimming The A8512 has a very wide range for PWM signal input. It can accept a PWM signal from 100 Hz to 5 kHz. When a PWM high signal is applied, the LEDx pins sink

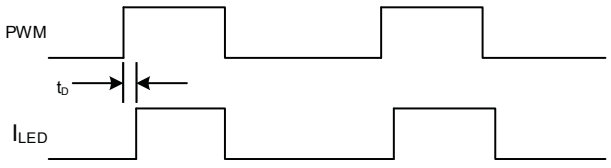


Figure 13. Propagation delay from the PWM signal rising edge to I_{LEDx} reaching the 90% level

100% Current. When the PWM signal is low, the LED sinks turn off.

Referring to figure 13, there is a ramp-up delay between when the PWM signal is applied and when the current reaches the 90% level. To improve current dimming linearity for PWM pulse widths less than 100 µs, increase the applied PWM pulse-width by 3 to 5 µs to compensate for this delay.

Startup Sequence When EN is pulled high, the IC enters soft start. The IC first tries to determine which LEDx pins are being used, by raising the LEDx pin voltage with a small current. After a duration of 512 switching cycles, the LEDx pin voltage is checked. Any LEDx channel with a drain voltage smaller then 100 mV is removed from the control loop. This is the reason why unused LEDx pins should be connected to GND,

After the first PWM positive trigger, the boost current is limited to 30% of normal value and all active LEDx pins sink $^1/_{12}$ of the set current until output voltage reaches sufficient regulation level. When the device comes out of soft start, boost current and the LEDx pin currents are set to normal operating level. Within a few cycles, the output capacitor charges to the voltage required to supply full LEDx current. After output voltage, V_{OUT}, reaches the required level, LEDx current toggles between 0% and 100% with each PWM command signal.

In case of a heavy overload on V_{OUT} at startup, the device will stay in soft start mode indefinitely, as the output voltage cannot rise to the LED regulation level.

LED Short Detect Any LEDx pins that have a voltage exceeding the Short Circuit Detect Voltage, V_{SC} , cause the device to shut down and this condition is latched. This faults occurs when multiple LEDs short. In case only a few LEDs short, the IC will continue to work as long as power dissipation in the IC is limited.

Overvoltage Protection The A8512 has an adjustable overvoltage protection feature to protect the power components (external MOSFET, output diode and capacitors) against output overvoltage. The overvoltage level can be set, from 19.5 V to a higher voltage, with an external resistor, R_{OVP}. When the current though the OVP pin exceeds 200 µA, internal OVP comparator goes high and the device shuts down. The OVP fault disables all LEDx strings that are below regulation, thus preventing them from controlling the boost output voltage.

Calculate the value for R_{OVP} (Ω) as follows:

$$R_{OVP} = (V_{OVP} - 19.5) / 200\ \mu A \ , \qquad (5)$$

where V_{OVP} is the required OVP level in V.

For single-IC operation, select R_{OVP} such that its OVP setpoint is approximately 10 V above the LED operating voltage at cold. For example, given the pin regulation voltage, V_{LEDx} of 1.4 V (typ.), if LED V_F = 3.4 V (max.) and there are 15 LEDs in series, then the operating voltage is approximately:

$$V_{OUT} = 3.4\ V \times 15 + 1.4\ V = 52.4\ V \ .$$

In this case, select OVP at about 60 V, which gives R_{OVP} = 200 kΩ.

Open LED Protection During normal operation, if any enabled LED string opens, voltage on the corresponding LEDx pin goes to zero. The boost loop operates in open loop till the OVP level is reached. The A8512 identifies the open LED string when overvoltage is detected. Open strings are then removed from the regulation loop. Afterwards, the boost controller operates in normal manner, and the output voltage is regulated to drive the remaining strings. If the open LED string is reconnected, it will sink current up to the programmed current level.

Note: Open strings are removed from boost regulation, but not disabled. This keeps the string in operation if LEDs open for only a short length of time, or reach OVP level on a transient event.

The disconnected string can be restored to normal mode by reenabling the IC. It can also be restored to normal operation if the fault is removed from the corresponding LEDx pin, but an OVP event occurs on any other LEDx pin.

Overcurrent Protection The IC provides pulse-by-pulse current limiting for the boost MOSFET. The current limit level, I_{SC} (A), can be set by selecting the external resistor, R_{SC} (Ω):

$$R_{SC} = 0.095 / I_{SC} \ . \qquad (6)$$

If the boost output voltage is unable to reach the regulation target even when the switch is operating at maximum current limit, the boost control loop will force the compensating capacitor, C_{COMP}, to rise in voltage until it reaches the overcurrent fault level (3.4 V approximately). The overcurrent fault forces the device into soft start.

Thermal Shutdown (TSD) The IC shuts down when junction temperature exceeds 165°C. It will recover automatically when the junction temperature falls below 125°C approximately.

VIN Undervoltage Lockout (UVLO) The device is shut down when input voltage, V_{IN} , falls below V_{UVLO}. Any existing latched fault is cleared.

V_{IN} Operating Range Considerations When V_{IN} is above V_{UVLO} and below 10 V, the IC will operate correctly, but its gate driver voltage may not reach the regulation target of 7 V. This may cause excessive switching and conduction loss if the external MOSFET is not fully enhanced.

During normal operation, the IC draws approximately 10 to 15 mA from the VIN pin, depending on switching frequency and the external MOSFET. At V_{IN} = 12 V, this translates into 120 to 180 mW of power consumption, most of it dissipated in internal linear regulators. This power increases proportionally with input voltage. Therefore it is highly recommended to keep V_{IN} between 10 and 24 V during normal operation.

If the input battery voltage must be higher than 24 V, a better solution is to power the VIN pin separately using a 12 V supply. Doing this reduces the heat dissipation of the IC, and improves the overall system efficiency.

Fault Mode in Single-Controller Operation

Fault State	Auto-Restart	Description
Over-voltage Protection	Yes	Fault occurs when output voltage exceeds the OVP setpoint voltage. Used to prevent the output voltage from damaging the power components.
Pulse-by-Pulse Current Limit	Yes	Fault occurs when the current through the external MOSFET increases such that the voltage across the SENSE1 and SENSE2 pins exceeds 95 mV typical. The MOSFET switch is turned off on a cycle-per-cycle basis.
Overcurrent Protection	Yes	Multiple pulse-by-pulse current limits will cause the COMP pin voltage to rise. After a time period determined by the COMP pin current and the COMP capacitor, the COMP voltage will exceed the overcurrent detect threshold, forcing a fault. System may hiccup if the total current requirement is too high.
Over-temperature Protection	Yes	Fault occurs when the die temperature exceeds the over-temperature threshold, 165°C typical.
LED Short Protection	No	Fault occurs when the LED pin voltage exceeds V_{SC}, 25 V typical.
VIN UVLO	No	Fault occurs when VIN drops below V_{UVLO}, 6.5 V typical. This fault resets all latched faults.

Parallel Operation The A8512 is designed to operate with up to six A8512 devices connected in parallel, in order to drive a greater number of LED strings. In this case, the A8512 which controls the boost converter is designated the master, while the other devices are slaves which serve as current sinks for their own LED strings. Slaves communicate with the master through the shared COMP signal. PWM dimming and protection mechanisms work consistently across all devices.

Select R_{OVP1} for the master controller such that its OVP setpoint is approximately 10 V above the LED operating voltage at cold. Select R_{OVP2} for each slave controller at approximately 15 to 25 kΩ lower than that for the master. This ensures that, in the case in which an open-LED fault occurs, the slave controllers will enable OVP before the master does.

Application Information

PCB Layout Guidelines As with any switching power supply, care should be taken in laying out the board. A switching power supply has sources of high dv/dt and high di/dt which can cause malfunction. All general norms should be followed for board layout. Refer to figure 14 for a typical application schematic. The A8512 evaluation board provides a useful model for designing application circuit layouts.

The following guidelines should be observed:

- Place bypass capacitors physically close to their respective pins (VIN, VBIAS, and VREG7V).
- Route analog ground, digital signal ground, LED ground (LGND pin), and power ground (PGND pin) separately. Connect all these grounds at the common ground plane under the A8512, serving as a star ground.
- Place the input capacitors (C1, C2), inductor (L1), boost diode (D1), MOSFET (Q1), and output capacitors (C3, C4) so that they form the smallest loop practical. Avoid long traces for these paths.
- Place the resistors R_{FSET} and R_{ISET}, and the compensation components (Rz and Cz) close to the FSET, ISET, and COMP pins, respectively. Connect the other ends to the common star ground.
- A8512 has 50 kΩ internal pull-down resistors on the EN and PWM pins to keep these pins low while driving through tri-state state (for example, shutdown). Add external resistors R2 and R3 between the EN and PWM pins and ground, for added noise immunity. Connect these resistors close to the pins and return to the common star ground.
- Sense voltage across R_{SC} with smaller length traces. Place the SENSE1 and SENSE2 traces as close to each other as possible to minimize noise pickup. Connect the SENSE2 trace to the negative end of the resistor and do not connect it to power ground plane.
- Provide a substantial copper plane near MOSFET Q1 and the IC, to provide good thermal conduction. When using multi-layer PCB, make sure there are sufficient numbers of thermal vias underneath and around the IC's exposed pads.

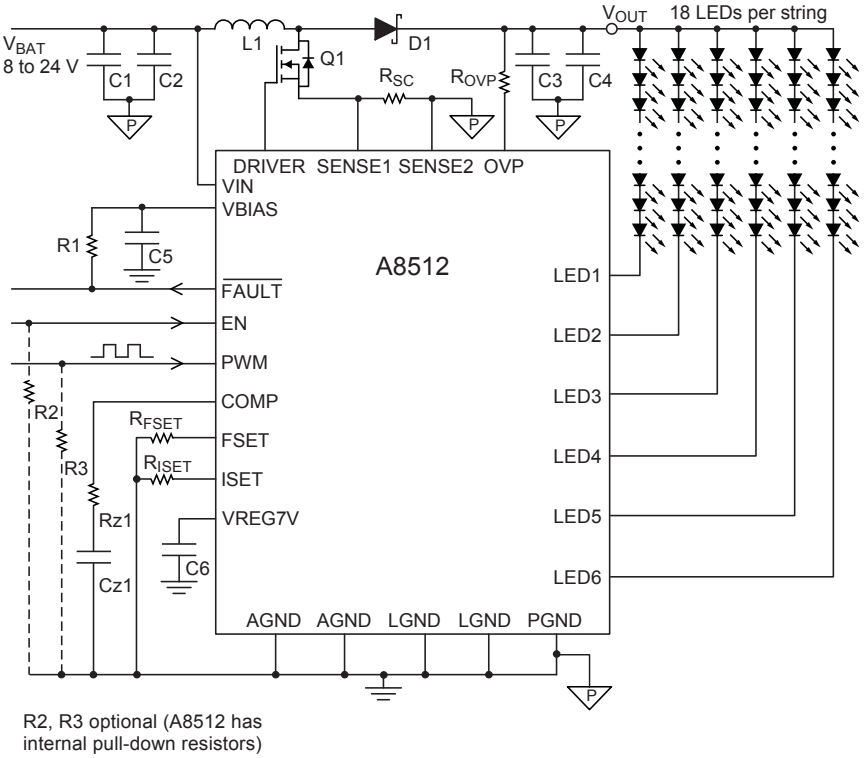


Figure 14. Typical application circuit with single controller; VIN pin tied to V_{BAT}.

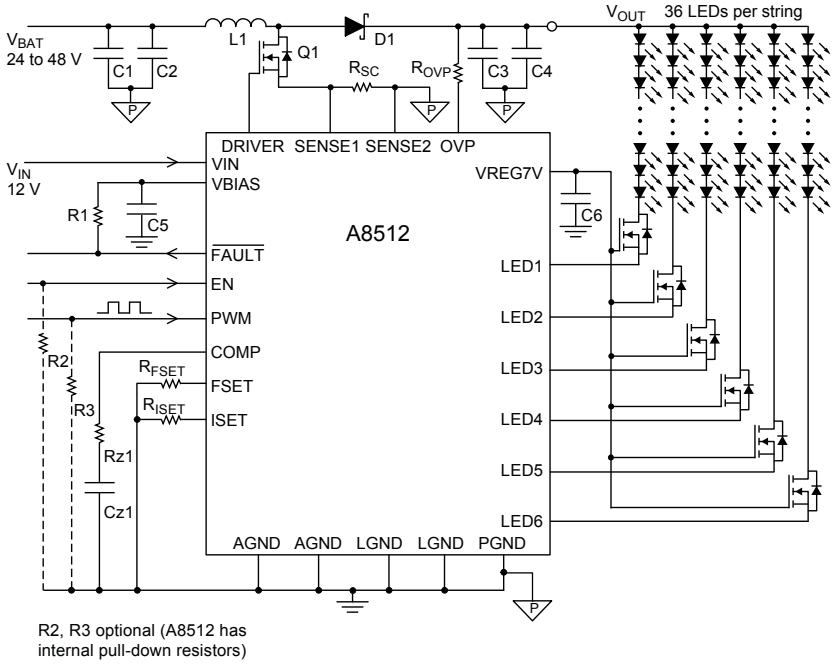


Figure 15. Typical high-voltage application circuit with single controller; VIN pin separate from V_{BAT}.

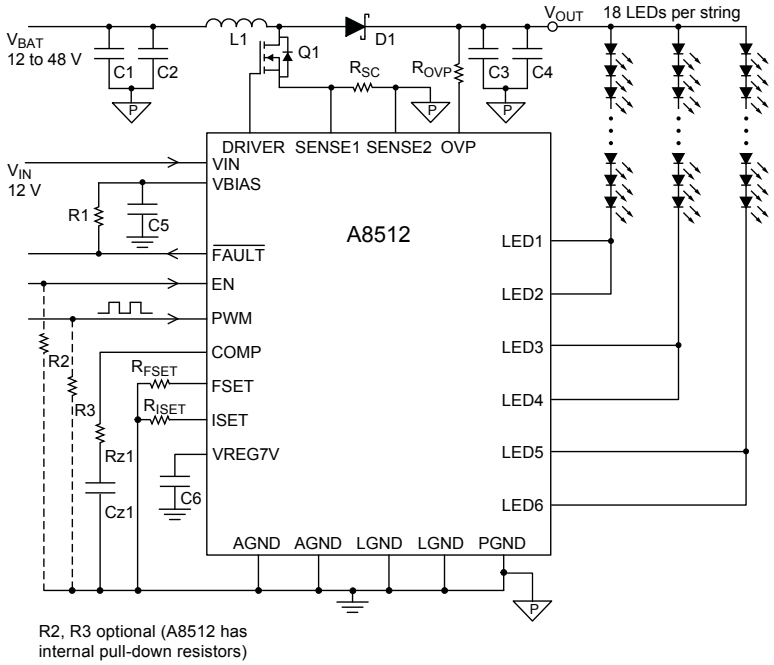
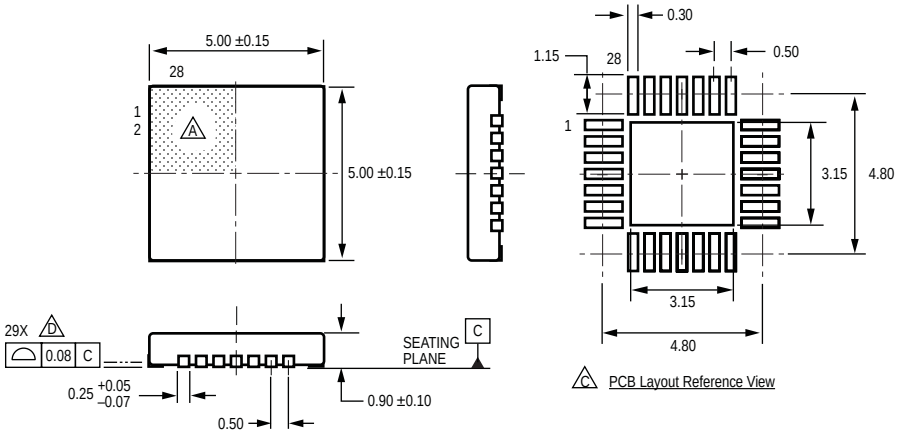
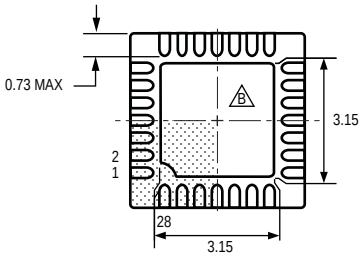


Figure 16. Typical medium-voltage application circuit driving high-current (up to 160 mA) LED strings.

Package ET 28-Contact QFN





For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

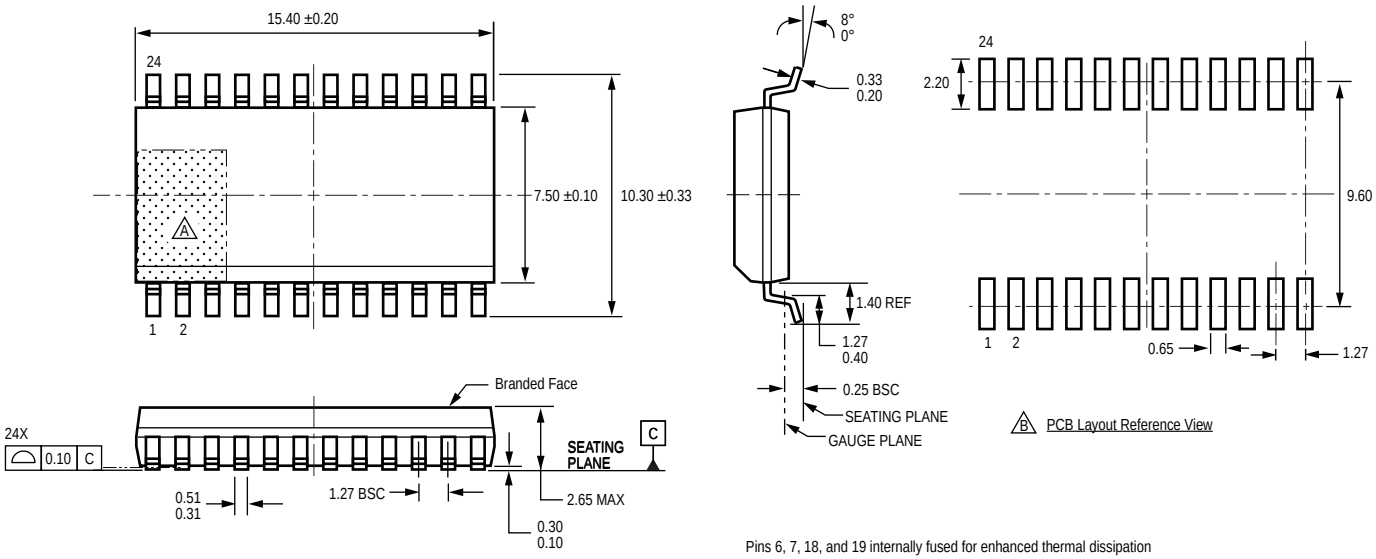
A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package LB 24-Pin SOICW with Internally Fused Pins



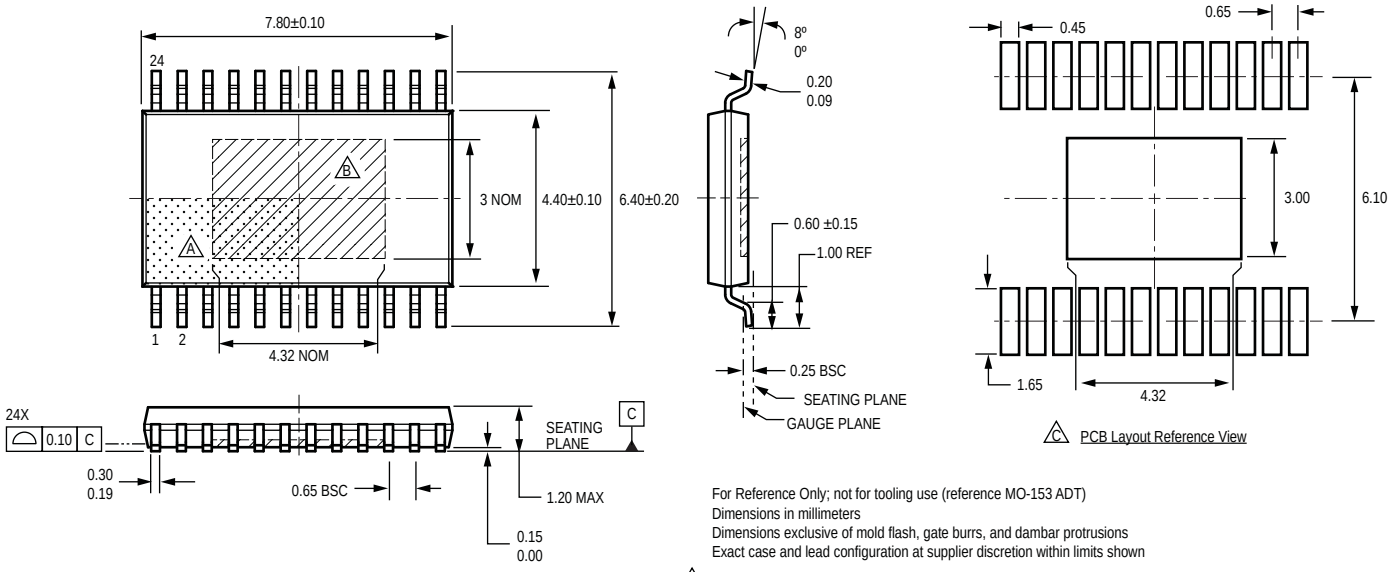
Pins 6, 7, 18, and 19 internally fused for enhanced thermal dissipation

For Reference Only; not for tooling use (reference MS-013AD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Package LP 24-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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