Preliminary specification   PCD4440

Analog Voice Scrambler / Descrambler

The PCD4440 is a silicon gate CMOS integrated circuit intended to be used in radio, mobile- and line powered telecommunications products utilizing a microcontroller for the control functions. Analog scrambling / descrambling is based on the split frequency method realized in a sophisticated switched-capacitor technology. The PCD4440 is compatible with most microcontrollers and communicates via a two line bidirectional bus (I2C).

Features

- Scrambler or descrambler function
- Scrambling in frequency domain
- Selectable split frequency (up to 10 selections per second)
- Telephony-band filtering included
- No increase in bandwidth
- No external components required
- Small signal delay
- Insensitive to distortion and group delay of transmission channel
- Control via serial (I2C) bus
- Low transfer loss of speech
- Mute option
- Transparent mode
- High signal input impedance
- Low signal output impedance
- Low power consumption

Applications

- Cordless telephones
- Security telephones
- Portable phones
- PMR

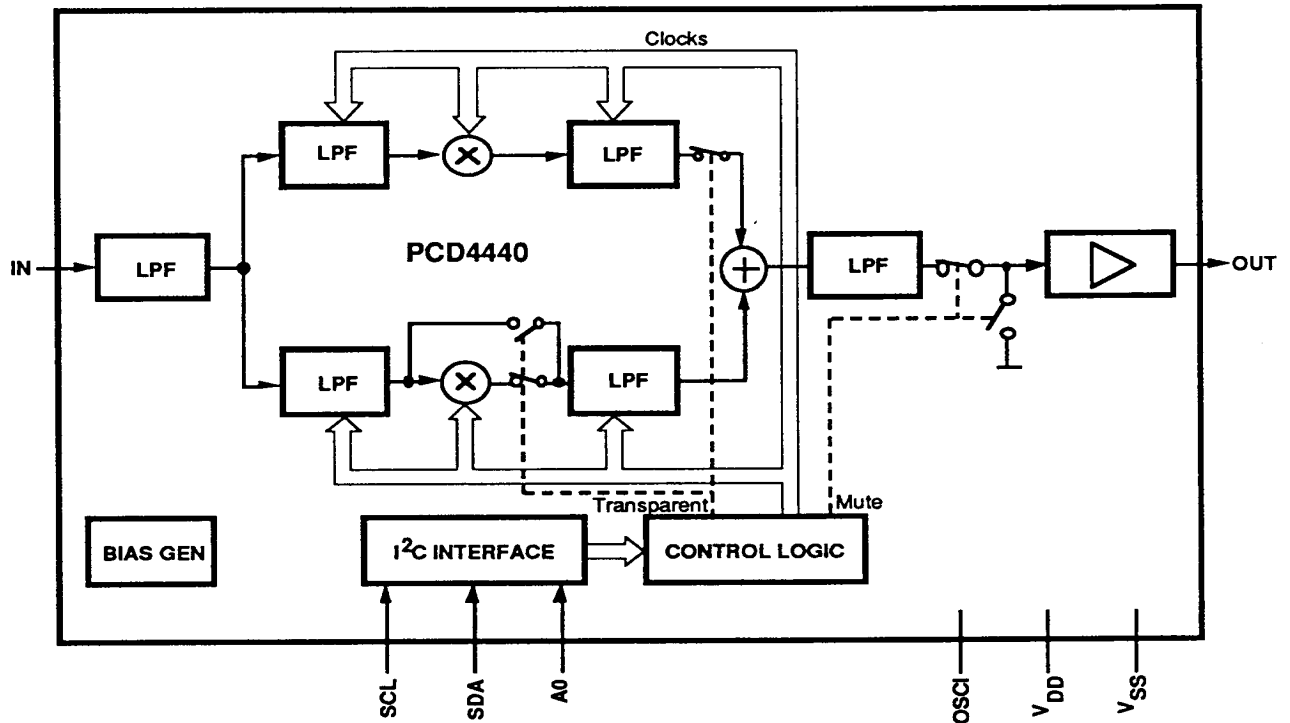### Package outlines

PCD4440T: 8-lead mini-pack (SO8L; SOT176C)

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BLOCK DIAGRAM

Fig. 1 Block diagram PCD4440

PINNING DIAGRAM
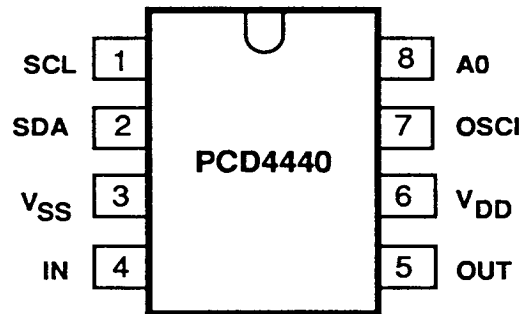
Fig. 2 Pinning PCD4440T

| Pin	Name	Function
1	SCL	Serial Clock Line (I2C)
2	SDA	Serial Data Line (I2C)
3	V_{SS}	Negative Supply
4	IN	Signal input
5	OUT	Signal output
6	V_{DD}	Positive supply
7	OSCI	Oscillator input
8	A0	Slave address input (I2C)

FUNCTIONAL DESCRIPTION

To provide privacy for the end user of a cordless telephone set, the radio-link audio signal must be scrambled. In the microphone as well as the incoming telephone line audio path a scrambler circuit has to be implemented. Consequently the audio signal to the telephone line as well as to the earpiece must be descrambled. Both functions can be fulfilled by the PCD4440 by simply inserting it in the audio path.

The PCD4440 accomplishes this task by first filtering the incoming signal, limiting the bandwidth to 3500 Hz. Then the signal is split into a high ($> f_S$) and a low ($< f_S$) frequency band. Both frequency bands are inverted and added again to provide a single output signal. Values for 9 split frequencies f_S can be controlled by a scramble code table in the microcontroller. Control of these split frequencies is accomplished via the serial two wire I2C bus (see table 1). In addition to the split frequencies (fs), a transparent mode and mute instruction can be selected (see table 1).

In Fig. 3, the signal path for both bands is drawn. The lower band path (on the left side of the diagram) works on frequencies $f \leq f_S$ (Split Frequency), the upper band path (on the right side) on frequencies $f \geq f_S$.
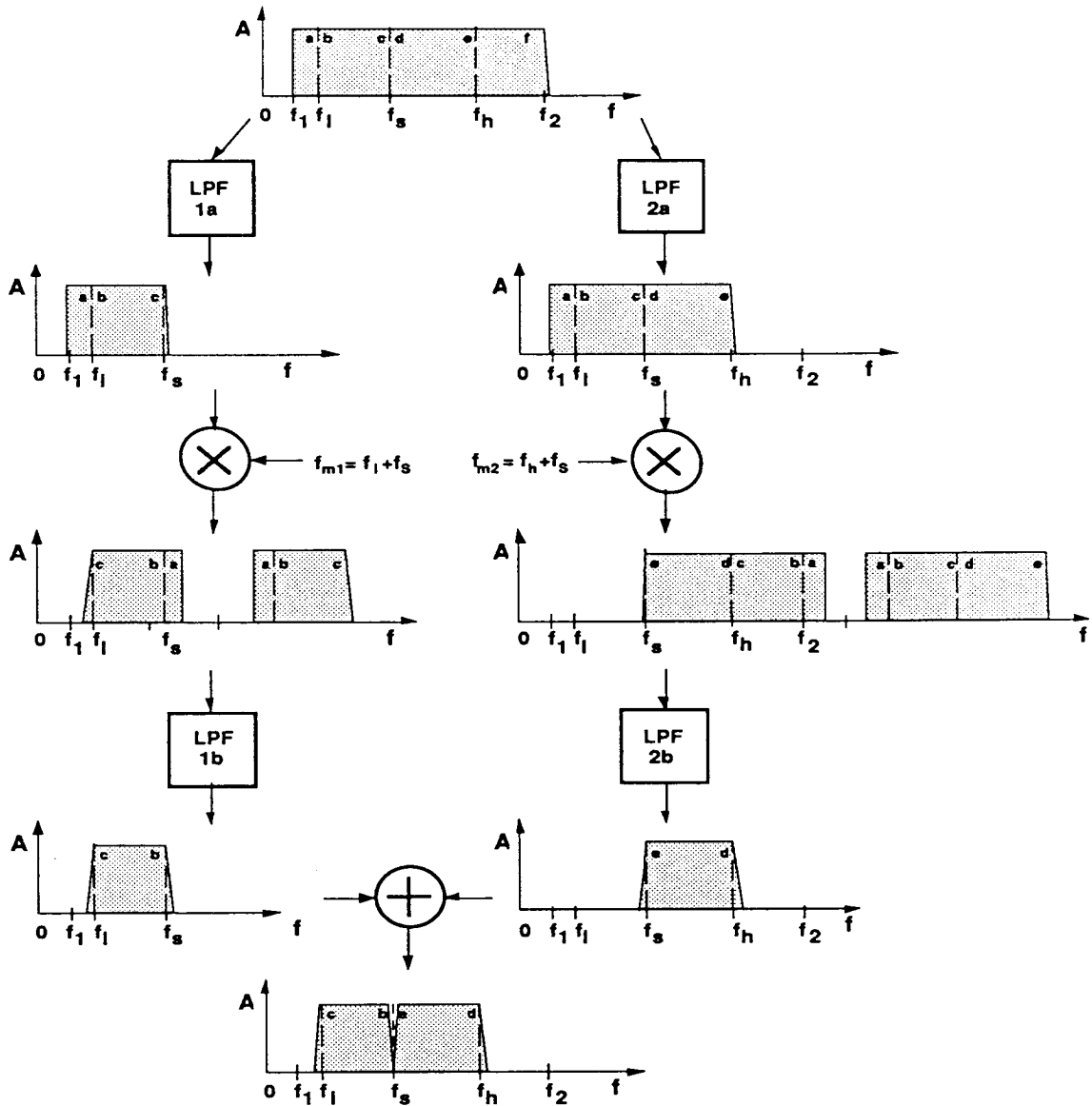
Fig. 3 Scrambler signal path

The input signal contains frequencies from f_1 up to f_2. The output signal is bandlimited (only in scrambling mode) from f_l (300 Hz) to f_h (3500 Hz). In the left path, the input signal is first limited to f_s. The following modulator inverts the lower band. f_l is folded up to f_s, f_s down to f_l. In general, an input frequency f_{in} is folded to $f_{out} = f_s + f_l - f_{in}$. Finally the folded signal is bandlimited to f_s again.

In the right path, the input signal is first limited to f_h. The following modulator inverts the upper band. f_s is folded up to f_h, f_h down to f_s. In general, an input frequency f_{in} is folded to $f_{out} = f_s + f_h - f_{in}$. Finally, the folded signal is bandlimited to f_h again. In the last step, the bands are added and buffered.

✳ In the transparent mode, the input signal is band limited to 3500 Hz. Frequencies form 0 - 300 Hz are not filtered out.

Power supply (V$_{DD}$, V$_{SS}$)

The positive supply of the circuit (V$_{DD}$) must meet the voltage requirement as indicated in the characteristics. To avoid undefined states of the device when powered-on, an internal power-on circuit clears the control logic. The power-on reset has the highest priority; it blocks and resets the complete circuit.

Oscillator (OSCI)

The time base for the PCD4440 is a 3.58 MHz input signal which can be derived from OSCO (oscillator output) of Philips' microcontroller families PCD33xx or PCF84Cxx.
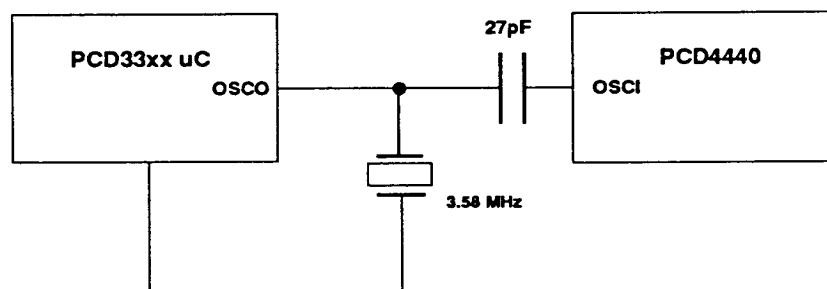

Figure 4   OCSI (freq. input) connection

D3	D2	D1	D0	HEX	APPLICATION	Fs (Hz*)
0	0	0	1	01	MUTE MODE	-
0	0	1	0	02	SELECT Fs	2461
0	0	1	1	03	SELECT Fs	1853
0	1	0	0	04	SELECT Fs	1507
0	1	0	1	05	SELECT Fs	1279
0	1	1	0	06	SELECT Fs	1117
0	1	1	1	07	SELECT Fs	1018
1	0	0	0	08	SELECT Fs	899
1	0	0	1	09	SELECT Fs	837
1	0	1	0	0A	SELECT Fs	767
1	0	1	1	0B	Transparent Mode	-
1	1	1	1	0F	Start scramble/ descramble mode	-

$*F_{osc}=3.58MHz$

Table 1   input data code

Note: input codes other than shown in the table are not allowed.

Serial clock input (SCL), Serial data input (SDA)

SCL and SDA are serial clock and data lines according to the Philips' I2C bus specification (see CHARACTERISTICS OF THE I2C BUS). Both inputs must be pulled-up externally to V_{DD} (through approximately 10KΩ).

Address input (A0)

A0 is the slave address input and it identifies the device when up to two PCD4440 devices are connected to the same I2C bus. In any case A0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see fig. 5)

The PCD4440 is always a slave receiver in the I²C bus configuration (R/W bit = 0). The slave address consist of 7 bits, where the least significant bit is selectable by hardware on input A0. The more significant bits are internally fixed. See figure 5, " I²C bus data format". For definition of D0-D4, see table 1.
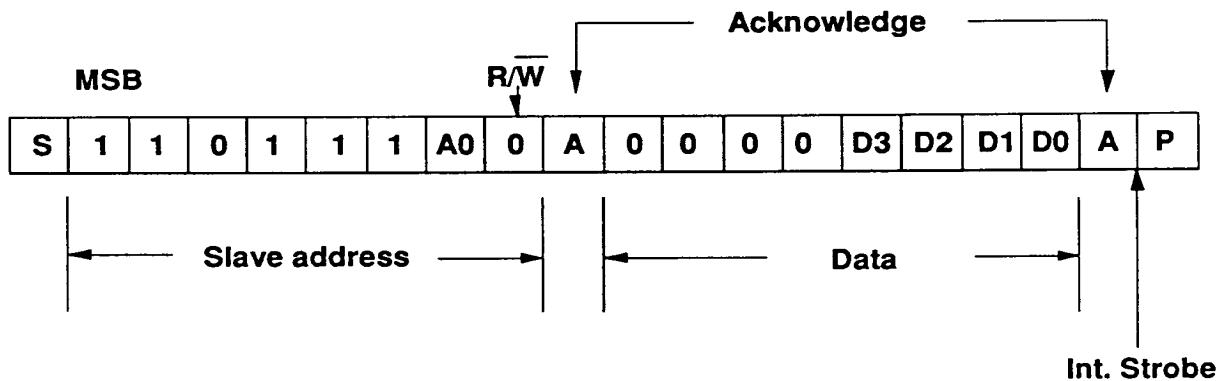

Figure 5 I²C bus data format

✳ Signal input (IN), Signal output (OUT)

Signal input for the scrambler / descrambler is coupled into a Sallen and Key anti-aliasing filter configuration. A DC bias voltage of $1/2V_{DD}$ is built-in.

The analog signal output is buffered to achieve a relatively low output impedance of roughly 1 KΩ which is sufficiently low to drive the earpiece amplifier or similar application.

CHARACTERISTICS OF THE I²C BUS

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.
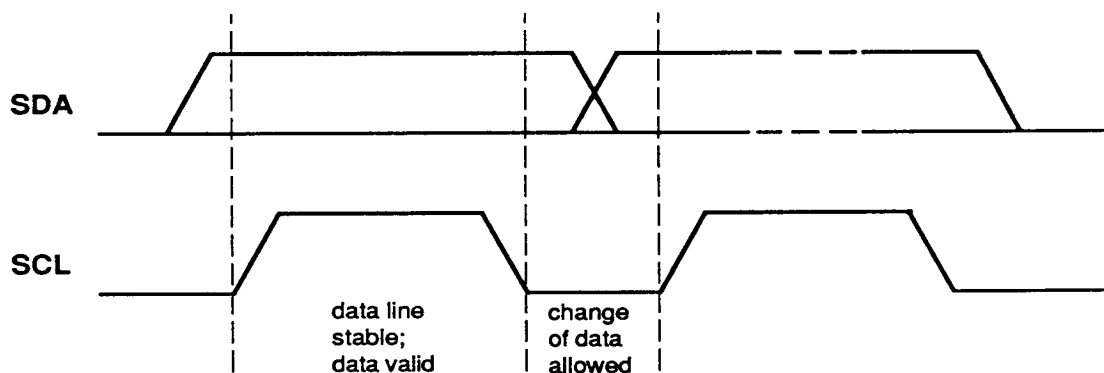

Fig. 6 Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).
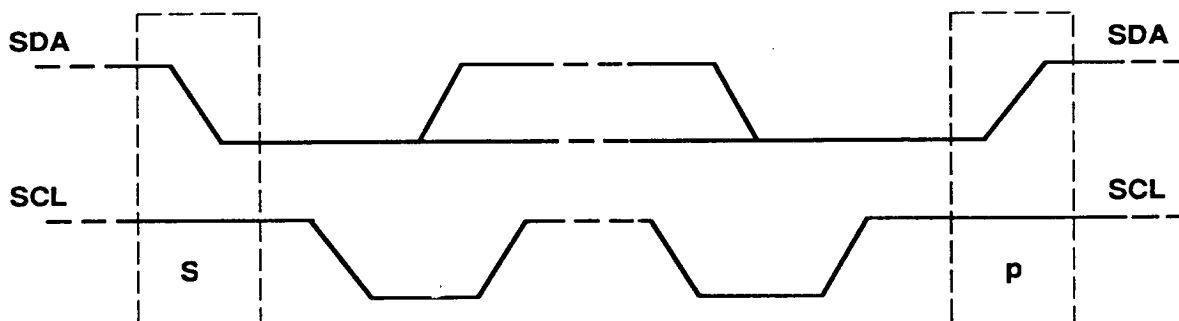

Fig. 7 Definition of start and stop conditions

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".
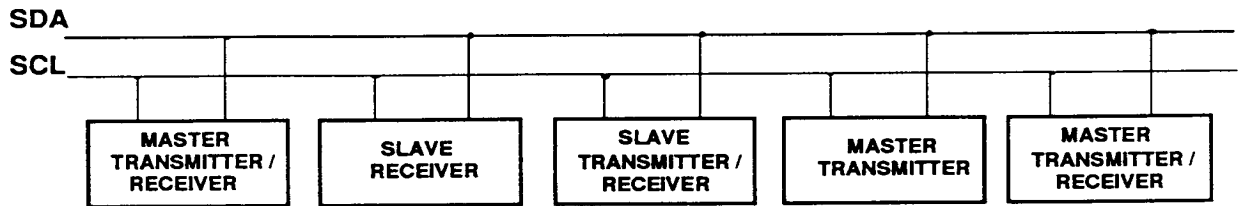

Fig.8 System configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.
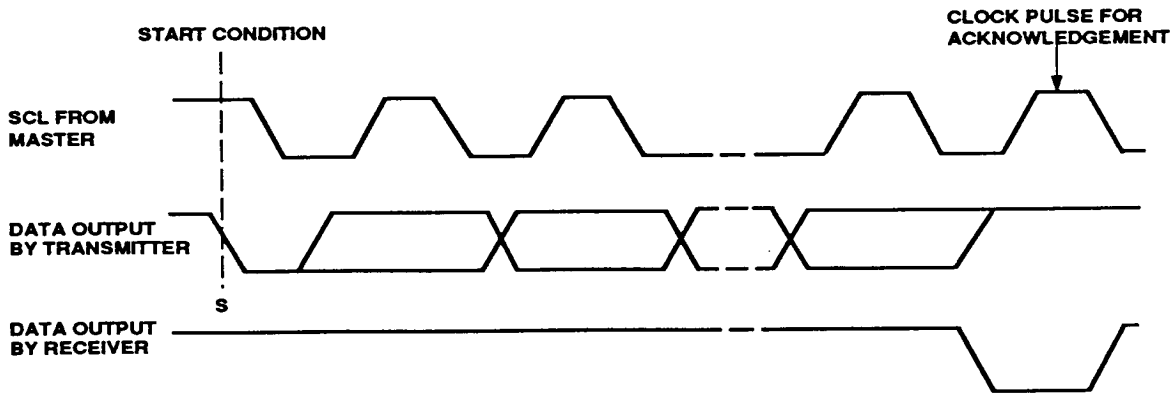

Fig. 9 Acknowledgement on the I2C-bus

Note: The general characteristics and detailed specification of the I2C-Bus are available on request.

I²C BUS TIMING SPECIFICATIONS

All the timing values area valid within the operating supply voltage and ambient temperature range and refer to V_{il} and V_{ih} with an input voltage swing of V_{ss} to V_{DD}.

Parameter	symbol	min.	max.	units
SCL clock frequency	f_{SCL}	0	100	kHz
Tolerable bus spike width	T_{sw}	-	100	ns
Bus free time	T_{buf}	4.7	-	µs
Start condition set-up time	$T_{su;STA}$	4.7	-	µs
Start condition hold time	$T_{hd;STA}$	4.0	-	µs
SCL LOW time	T_{low}	4.7	-	µs
SCL HIGH time	T_{high}	4.0	-	µs
SCL and SDA rise time	T_r	-	1.0	µs
SCL and SDA fall time	T_f	-	0.3	µs
Data set-up time	$T_{su;DAT}$	250	-	ns
Data hold time	$T_{hd;DAT}$	0	-	ns
Stop condition set-up time	$T_{su;STO}$	4.0	-	µs
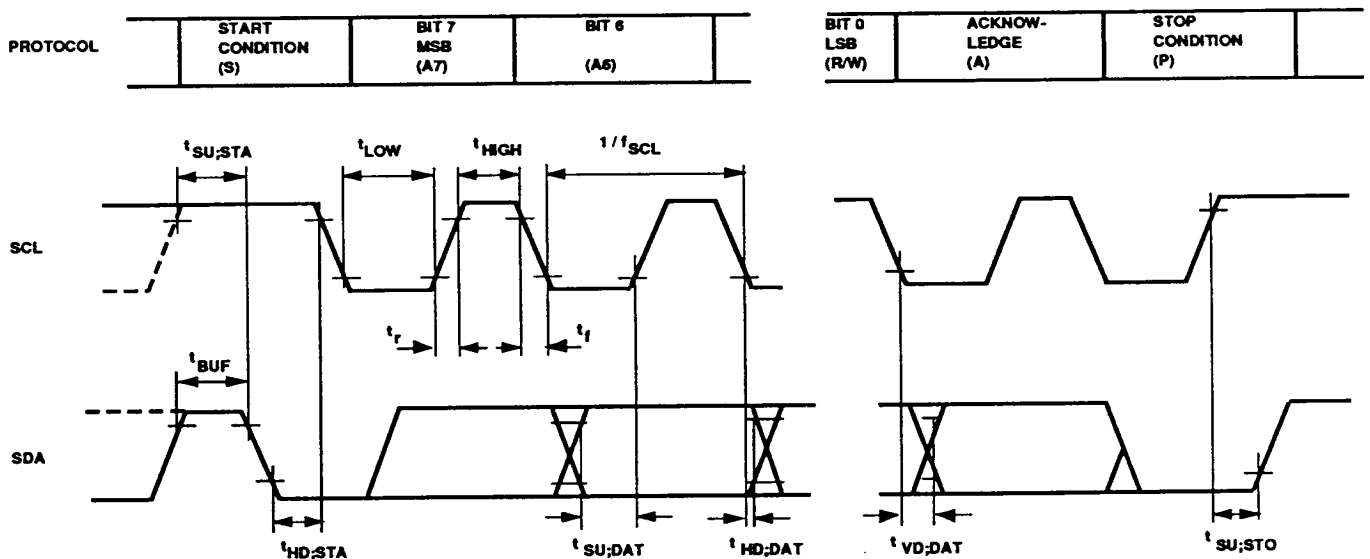
Fig. 10 I²C-bus timing diagram

CHARACTERISTICS

V_{DD} = 5.0 V; V_{SS} = 0 V; T_{amb} = +25 °C; f_{osci} = 3.579 MHz
unless otherwise specified

parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply						
Supply voltage	V_{DD}		2.8	-	6.0	V
Supply current						
mute mode	I_{DDP}	V_{DD}= 3 V	-	2.2	-	mA
Operating	I_{DD}	V_{DD}= 3 V	-	13	-	mA
Inputs/Outputs						
A0 ; SCL ; SDA						
Input voltage LOW	V_{IL}		0	-	$0.3V_{DD}$	V
Input voltage HIGH	V_{IH}		$0.7V_{DD}$	-	V_{DD}	V
input capacitance	C_1		-	-	7	pF
SDA output current low						
at V_{OL} = 0.4 V	I_{OL}		3.0	-	-	mA
Signal input						
IN						
DC voltage level	V_{DC}		-	$1/2V_{DD}$	-	V
allowed amplitude	$V_{i(P-P)}$		-	1.25	V_{DD} -1	V
input impedance	abs(Z_i)	freq. = 1 kHz	-	120	-	kΩ
Signal output						
OUT						
DC voltage level	V_{DC}		-	$1/2V_{DD}$	-	V
output impedance	abs(Z_0)	freq. = 1 kHz	-	-	1	kΩ
Unwanted Frequency Supression at $V_{i(P-P)}$ = 1.25 V F_{split} = 767 or 2461 Hz F_{in} = 1 kHz	UFS	V_{DD}= 3 V or 5 V	40			dB
Transfer loss V_o / V_i :						
transparent mode	abs(A_{tr})		-	3.5	-	dB
operating mode	abs(A_{op})		-	0	-	dB
Freq. input						
OSCI						
DC voltage level	V_{DC}		-	$1/2V_{DD}$	-	V
Input voltage LOW	V_{IL}		-	-	$0.3V_{DD}$	V
Input voltage HIGH	V_{IH}		$0.7V_{DD}$	-	-	V

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	-0.3 V to 7.0 V
Voltage range on any input*	V_I	-0.8 to V_{DD} + 0.8 V
DC input current (any input)	+/- I_I	10 mA
DC output current (any input)	+/- I_O	20 mA
Total power dissipation	P_{TOT}	300 mW
Power dissipation per output	P	50 mW
Operating ambient temperature range	T_{AMB}	-25 to +70 °C
Storage temperature range	T_{STR}	-65 to +150 °C

*Measured via a 500 Ohm resistor

Note: Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
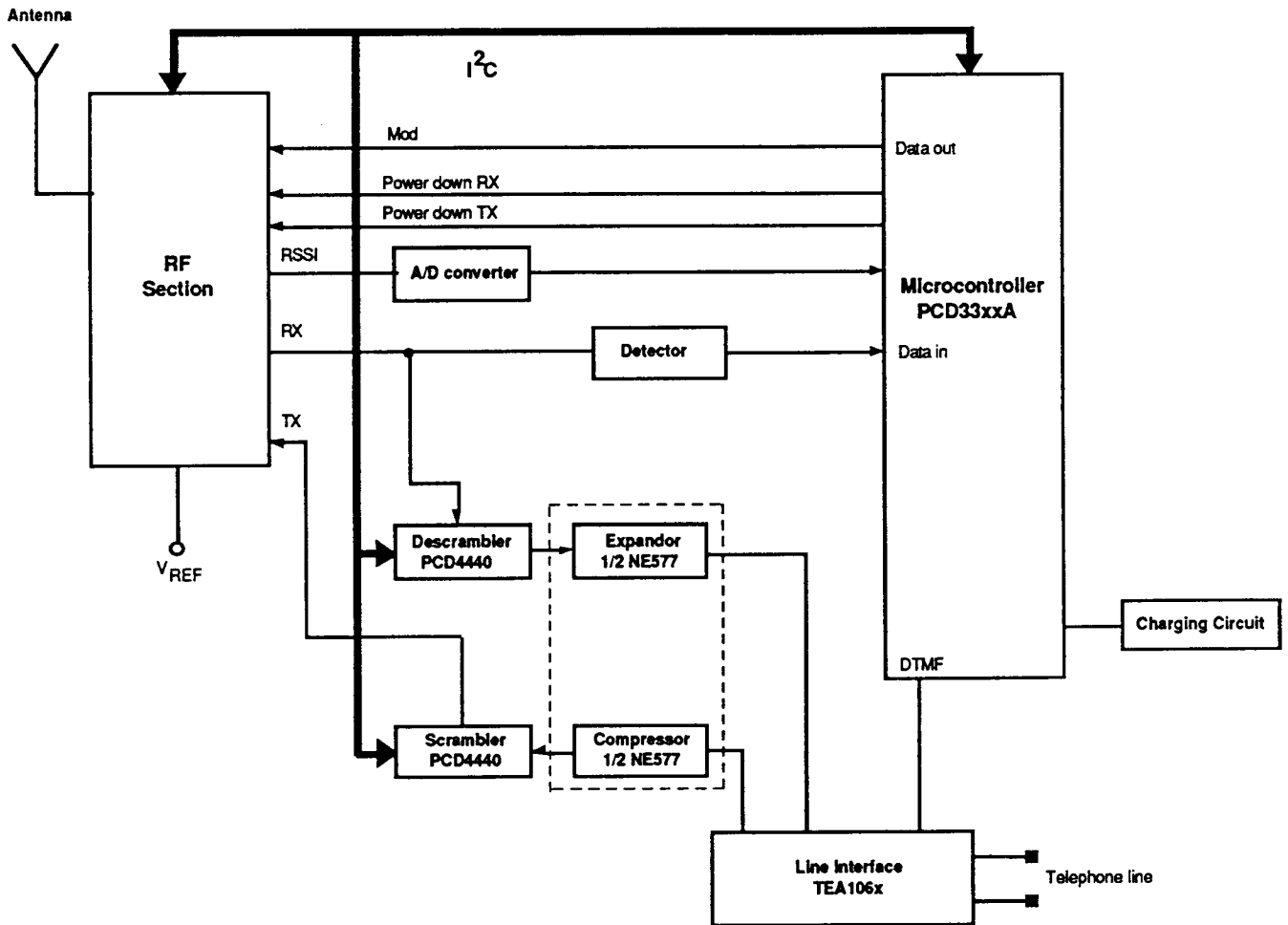
HANDLING

Inputs and Outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").
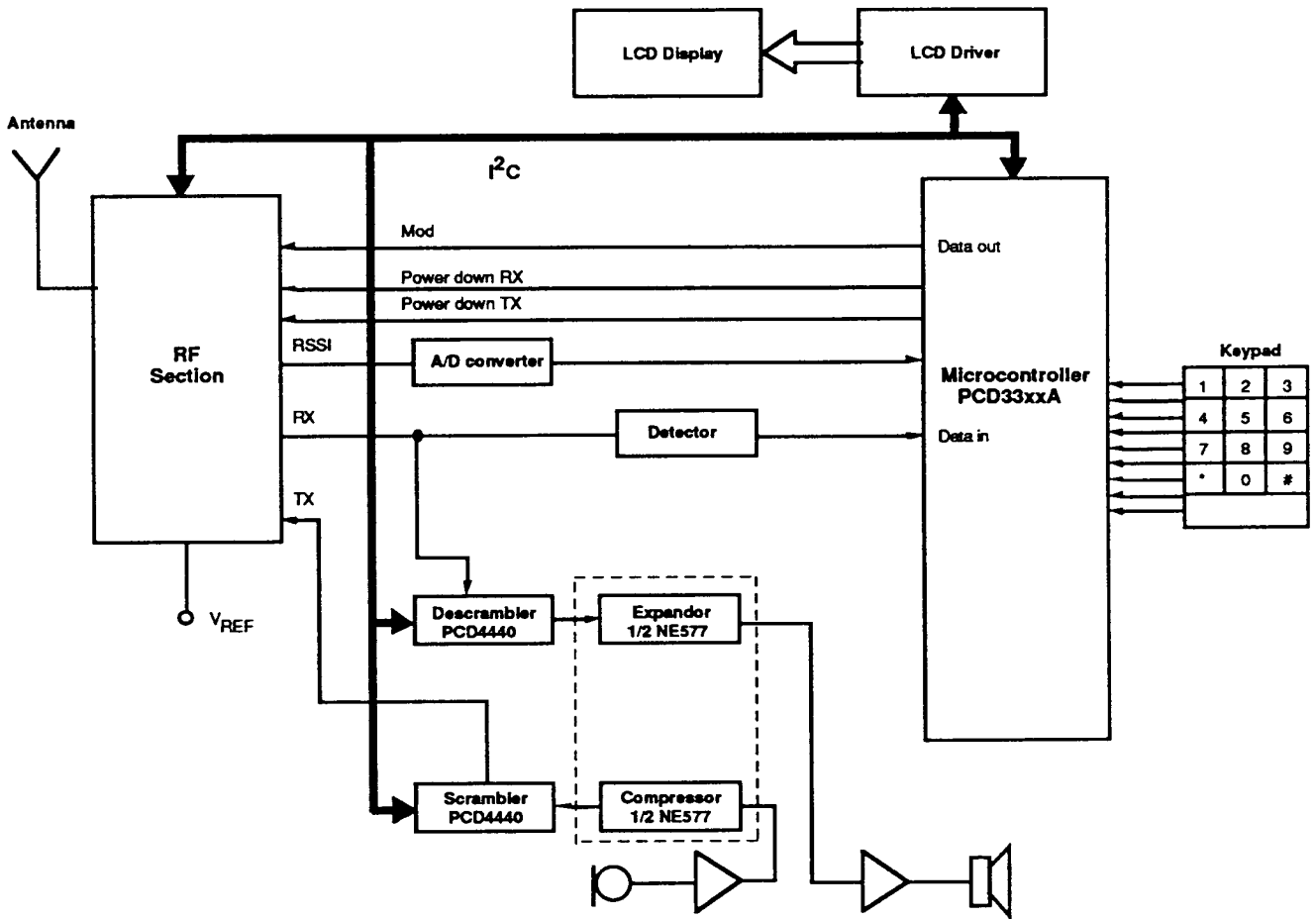
Fig. 11 Typical application: CT0 handset with direct (Manchester code) data system

Fig. 12 Typical applications; CT0 Base unit with direct (Manchester code) data system

DEFINITIONS

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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