International
IOR Rectifier

IR3514

DATA SHEET

XPHASE3™ AMD HYBRID CONTROL IC

DESCRIPTION

The IR3514 Hybrid Control IC combined with *xPHASE3*™ Phase ICs provides a full featured and flexible way to implement a complete AMD SVID or PVID power solution. It has the ability to independently control both the VDD core and VDDNB auxiliary planes required by the CPU when operated in SVI (Serial VID Interface) mode. The IR3514 can also receive Power Savings commands through the SVI serial bus and communicate this information to the IR3507 or other Phase ICs with PSI input capabilities. When operated in PVI (Parallel VID Interface) mode, the IR3514 controls the VDD core plane through 6 Parallel VID bits and the VDDNB auxiliary plane power stage goes to high impedance. PVI/SVI selection is made by sampling VID1 input upon Enable. The IR3514 interfaces with any number of Phase ICs each driving and monitoring a single phase. The *xPHASE3*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

- In SVI Mode (VID1=0 upon Enable)
  - 2 converter outputs for the AMD processor VDD core and VDDNB auxiliary planes
  - AMD Serial VID interface independently programs both output voltages and operation
  - Both converter outputs boot to 2-bit "Boot" VID codes which are read and stored from the SVC & SVD parallel inputs upon the assertion of the Enable input
  - PWROK input signal activates SVID after successful boot start-up
  - Both converter outputs can be independently turned on and off through SVID commands
  - Deassertion of PWROK prior to Enable causes the converter output to transition to the stored Pre-PWROK VID codes
  - Connecting the PWROK input to VCCL disables SVID and implements VFIX mode with both output voltages programmed via SVC & SVD parallel inputs per the 2 bit VFIX VID codes
  - PSI_L commands are forwarded to VDD core phase ICs

- In PVI Mode (VID1=1 upon Enable)
  - Single converter control for VDD with the VDDNB power stage in a high impedance state
  - AMD 6 bit parallel VID programs the VDD regulation voltage

- VRRDY monitors output voltages, VRRDY will deassert if any output voltage is out of spec
- 0.5% overall system set point accuracy
- Programmable Dynamic VID Slew Rates
- Programmable VID Offset (VDD output only)
- Programmable output impedance (VDD output only)
- High speed error amplifiers with wide bandwidths of 30MHz and fast slew rates of 12V/us
- Remote sense amplifiers provide differential sensing and require less than 50uA bias current
- Programmable per phase switching frequency of 250kHz to 1.5MHz
- Daisy-chain digital phase timing provides accurate phase interleaving without external components
- Hiccup over current protection with delay during normal operation
- Central over voltage detection and communication to phase ICs through the IIN (ISHARE) pin
- OVP disabled during dynamic VID down transitions to prevent false triggering
- Detection and protection of open remote sense lines
- Gate Drive and IC bias linear regulator control with programmable output voltage and UVLO
- Simplified VR Ready Output provides indication of proper operation and avoids false triggering
- Thermally enhanced 40L MLPQ (6mm x 6mm) package
- Over voltage signal to system with over voltage detection during powerup and normal operation

To request a complete datasheet contact Vijay Viswanathan at vviswan1@irf.com□□