





EH36 20

RoHS Compliant (Pb-free) 3.3V 4 Pad 3.2mm x 5mm Ceramic SMD LVCMOS High Frequency Oscillator

Frequency Tolerance/Stability \_\_\_\_\_\_ ±20ppm Maximum

Operating Temperature Range – 0°C to +70°C

T TS -55.000M

Nominal Frequency 55.000MHz

Pin 1 Connection
Tri-State (High Impedance)

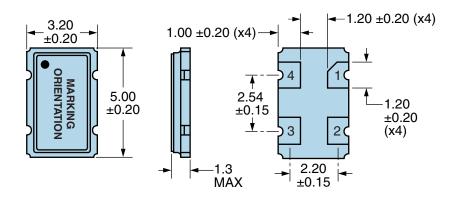
Duty Cycle 50 ±5(%)

#20ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)  ### Aging at 25°C  ### Appm/year Maximum  ### Operating Temperature Range  ### Occ to +70°C  ### Supply Voltage  ### Day Detail Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)  ### Day Detail Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)  ### Day Detail Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)  ### Day Detail Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)  ### Day Detail Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)  ### Day Detail Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration)  ### Day Detail Supply Voltage (Voltage Voltage)  ### Day Detail Supply Voltage (Voltage)  ###	ELECTRICAL SPECIFICATIONS		
Aging at 25°C	Nominal Frequency	55.000MHz	
Operating Temperature Range O°C to +70°C Supply Voltage 3.3Vdc ±0.3Vdc Input Current 35mA Maximum (No Load) Output Voltage Logic High (Voh) 2.7Vdc Minimum (IOH = -8mA) Output Voltage Logic Low (Vol) 0.5Vdc Maximum (IOL = +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±5(%) (Measured at 50% of waveform)  Load Drive Capability 30pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output. Absolute Clock Jitter  250pSec Maximum, ±10opSec Typical Start Up Time 10mSec Maximum	Frequency Tolerance/Stability	Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C,	
Supply Voltage       3.3Vdc ±0.3Vdc         Input Current       35mA Maximum (No Load)         Output Voltage Logic High (Voh)       2.7Vdc Minimum (IOH = -8mA)         Output Voltage Logic Low (Vol)       0.5Vdc Maximum (IOL = +8mA)         Rise/Fall Time       6nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       30pF Maximum         Output Logic Type       CMOS         Pin 1 Connection       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.         Absolute Clock Jitter       ±250pSec Maximum, ±100pSec Typical         One Sigma Clock Period Jitter       ±50pSec Maximum, ±40pSec Typical         Start Up Time       10mSec Maximum	Aging at 25°C	±5ppm/year Maximum	
Input Current  35mA Maximum (No Load)  Output Voltage Logic High (Voh)  2.7Vdc Minimum (IOH = -8mA)  Output Voltage Logic Low (Vol)  0.5Vdc Maximum (IOL = +8mA)  Rise/Fall Time  6nSec Maximum (Measured at 20% to 80% of waveform)  Duty Cycle  50 ±5(%) (Measured at 50% of waveform)  Load Drive Capability  30pF Maximum  Output Logic Type  CMOS  Pin 1 Connection  Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil)  70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.  Absolute Clock Jitter  250pSec Maximum, ±100pSec Typical  5tart Up Time  10mSec Maximum  10mSec Maximum	Operating Temperature Range	0°C to +70°C	
Output Voltage Logic High (Voh)       2.7Vdc Minimum (IOH = -8mA)         Output Voltage Logic Low (Vol)       0.5Vdc Maximum (IOL = +8mA)         Rise/Fall Time       6nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       30pF Maximum         Output Logic Type       CMOS         Pin 1 Connection       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.         Absolute Clock Jitter       ±250pSec Maximum, ±100pSec Typical         One Sigma Clock Period Jitter       ±50pSec Maximum, ±40pSec Typical         Start Up Time       10mSec Maximum	Supply Voltage	3.3Vdc ±0.3Vdc	
Output Voltage Logic Low (Vol)       0.5Vdc Maximum (IOL = +8mA)         Rise/Fall Time       6nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       30pF Maximum         Output Logic Type       CMOS         Pin 1 Connection       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.         Absolute Clock Jitter       ±250pSec Maximum, ±100pSec Typical         One Sigma Clock Period Jitter       ±50pSec Maximum, ±40pSec Typical         Start Up Time       10mSec Maximum	Input Current	35mA Maximum (No Load)	
Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform)  Duty Cycle 50 ±5(%) (Measured at 50% of waveform)  Load Drive Capability 30pF Maximum  Output Logic Type CMOS  Pin 1 Connection Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.  Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical  One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical  Start Up Time 10mSec Maximum	Output Voltage Logic High (Voh)	2.7Vdc Minimum (IOH = -8mA)	
Duty Cycle 50 ±5(%) (Measured at 50% of waveform)  Load Drive Capability 30pF Maximum  Output Logic Type CMOS  Pin 1 Connection Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.  Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical  One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical  Start Up Time 10mSec Maximum	Output Voltage Logic Low (Vol)	0.5Vdc Maximum (IOL = +8mA)	
Load Drive Capability       30pF Maximum         Output Logic Type       CMOS         Pin 1 Connection       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.         Absolute Clock Jitter       ±250pSec Maximum, ±100pSec Typical         One Sigma Clock Period Jitter       ±50pSec Maximum, ±40pSec Typical         Start Up Time       10mSec Maximum	Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)	
Output Logic Type CMOS  Pin 1 Connection Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.  Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical  One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical  Start Up Time 10mSec Maximum	Duty Cycle	50 ±5(%) (Measured at 50% of waveform)	
Pin 1 Connection Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.  Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical  One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical  Start Up Time 10mSec Maximum	Load Drive Capability	30pF Maximum	
Tri-State Input Voltage (Vih and Vil)  70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.  Absolute Clock Jitter  ±250pSec Maximum, ±100pSec Typical  One Sigma Clock Period Jitter  ±50pSec Maximum, ±40pSec Typical  Start Up Time  10mSec Maximum	Output Logic Type	CMOS	
output.  Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical  One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical  Start Up Time 10mSec Maximum	Pin 1 Connection	Tri-State (High Impedance)	
One Sigma Clock Period Jitter ±50pSec Maximum, ±40pSec Typical  Start Up Time 10mSec Maximum	Tri-State Input Voltage (Vih and Vil)		
Start Up Time 10mSec Maximum	Absolute Clock Jitter	±250pSec Maximum, ±100pSec Typical	
	One Sigma Clock Period Jitter	±50pSec Maximum, ±40pSec Typical	
Storage Temperature Range -55°C to +125°C	Start Up Time	10mSec Maximum	
	Storage Temperature Range	-55°C to +125°C	

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS		
Fine Leak Test	MIL-STD-883, Method 1014, Condition A	
Gross Leak Test	MIL-STD-883, Method 1014, Condition C	
Mechanical Shock	MIL-STD-202, Method 213, Condition C	
Resistance to Soldering Heat	MIL-STD-202, Method 210	
Resistance to Solvents	MIL-STD-202, Method 215	
Solderability	MIL-STD-883, Method 2003	
Temperature Cycling	MIL-STD-883, MEthod 1010	
Vibration	MIL-STD-883, Method 2007, Condition A	



### **MECHANICAL DIMENSIONS (all dimensions in millimeters)**

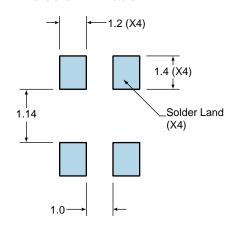


PIN	CONNECTION
1	Tri-State
2	Ground/Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E55.000 E=Ecliptek Designator

#### **Suggested Solder Pad Layout**

All Dimensions in Millimeters



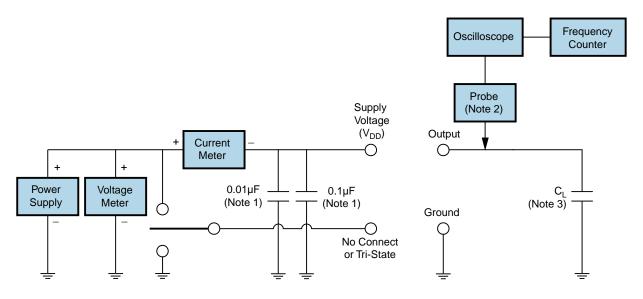
All Tolerances are ±0.1



#### **OUTPUT WAVEFORM & TIMING DIAGRAM**



#### **Test Circuit for CMOS Output**



- Note 1: An external  $0.1\mu F$  low frequency tantalum bypass capacitor in parallel with a  $0.01\mu F$  high frequency ceramic bypass capacitor close to the package ground and  $V_{DD}$  pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3: Capacitance value  $\dot{C}_L$  includes sum of all probe and fixture capacitance.



## **Recommended Solder Reflow Methods**



### **High Temperature Infrared/Convection**

T <sub>s</sub> MAX to T <sub>∟</sub> (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	150°C
- Temperature Typical (T <sub>s</sub> TYP)	175°C
- Temperature Maximum (T <sub>s</sub> MAX)	200°C
- Time (t <sub>s</sub> MIN)	60 - 180 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T <sub>P</sub> )	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T <sub>P</sub> Target)	250°C +0/-5°C
Time within 5°C of actual peak (tp)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1



### **Recommended Solder Reflow Methods**



#### Low Temperature Infrared/Convection 240°C

T <sub>S</sub> MAX to T <sub>L</sub> (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T <sub>s</sub> MIN)	N/A
- Temperature Typical (T <sub>s</sub> TYP)	150°C
- Temperature Maximum (T <sub>s</sub> MAX)	N/A
- Time (t <sub>s</sub> MIN)	60 - 120 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t <sub>L</sub> )	200 Seconds Maximum
Peak Temperature (T <sub>P</sub> )	240°C Maximum
Target Peak Temperature (T <sub>P</sub> Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (t <sub>p</sub> )	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

#### **Low Temperature Manual Soldering**

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

### **High Temperature Manual Soldering**

260°C Maximum for 5 seconds Maximum, 2 times Maximum.