# HMC895LP4E

## FILTER - TUNABLE, BAND PASS SMT 6.8 - 12.6 GHz

### Typical Applications

The HMC895LP4E is ideal for:

- Test & Measurement Equipment
- Military RADAR & EW/ECM
- SATCOM & Space
- Industrial & Medical Equipment

### Features

Fast Tuning Response

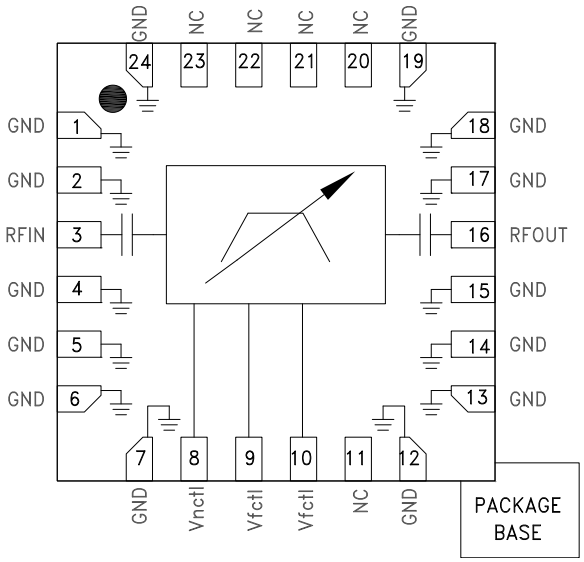
Excellent Wideband Rejection

Tunable low side/high side rejection “notch”

Single Chip Replacement for Mechanically Tuned Designs

24 Lead 4x4 mm SMT Package

### Functional Diagram




### General Description

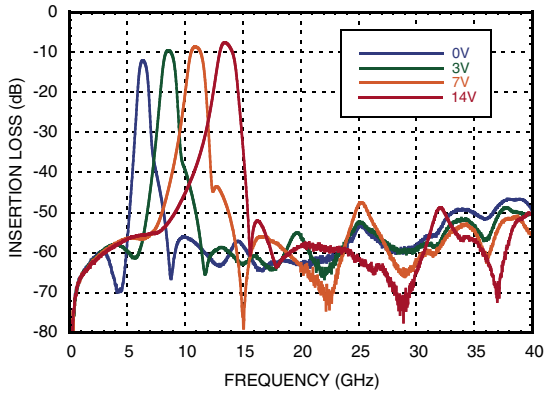
The HMC895LP4E is a MMIC band pass filter which features a user selectable passband frequency. The 3 dB filter bandwidth is approximately 10%. The 20 dB filter bandwidth is approximately 22%. The center frequency can be varied between 6.8 and 12.6 GHz by applying an analog tune voltage between 0 and 14V. This tunable filter can be used as a much smaller alternative to physically large switched filter banks and cavity tuned filters. The HMC895LP4E has excellent microphonics due to the monolithic design, and provides a dynamically adjustable solution in advanced communications applications.

### Electrical Specifications, $T_A$ = +25 °C, Vfctl = Vnctl Unless Otherwise Stated

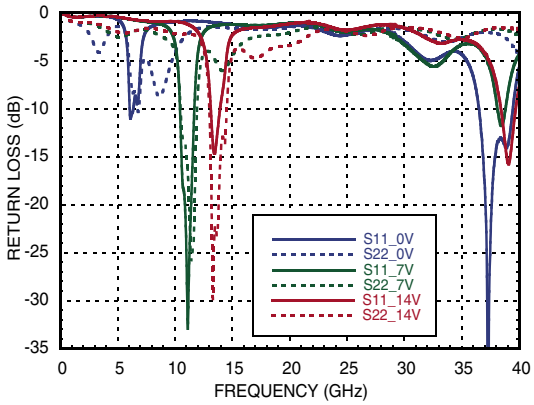
| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| $F_{center}$ Tuning Range | 6.8 | | 12.6 | GHz |
| 3 dB Bandwidth | | 10 | | % |
| Low Side Rejection Frequency (Rejection >20 dB) | | 0.88 *$F_{center}$ | | GHz |
| High Side Rejection Frequency (Rejection >20 dB) | | 1.10 *$F_{center}$ | | GHz |
| Low Side Sub-Harmonic Rejection (Rejection >40 dB) | | 0.75 *$F_{center}$ | | GHz |
| High Side Sub-Harmonic Rejection (Rejection >40 dB) | | 1.22 *$F_{center}$ | | GHz |
| Re-entry Frequency (Rejection <30 dB) | | >40 | | GHz |
| Insertion Loss | | 9 | | dB |
| Return Loss (2 dB bandwidth) | | 12 | | dB |
| Input IP3 (Pin = 0 to +15 dBm) | | 28 | | dBm |
| Input Power @ 5° Shift In Insertion Phase (Vfctl = 0V) | | 8 | | dBm |
| Input Power @ 5° Shift In Insertion Phase (Vfctl = 1V) | | 16.5 | | dBm |
| Frequency Control Voltage (Vfctl) | 0 | | 14 | V |
| Source/Sink Current (Ifctl | | | ±1 | mA |
| Low Side/High Side Rejection Control Voltage (Vnctl) | 0 | | 14 | V |
| Source/Sink current (Inctl) | | | ±1 | mA |
| Residual Phase Noise [1] (100 kHz Offset) | | -155 | | dBc/Hz |
| $F_{center}$ Drift Rate | | -1.0 | | MHz/°C |
| Tuning Speed, Phase Settling to within 10° [2] | | <200 | | ns |

[1] Optimum residual phase noise performance requires the use of a low noise driver circuit.
[2] Tuning speed includes 40 ns tuning voltage ramp from driver.

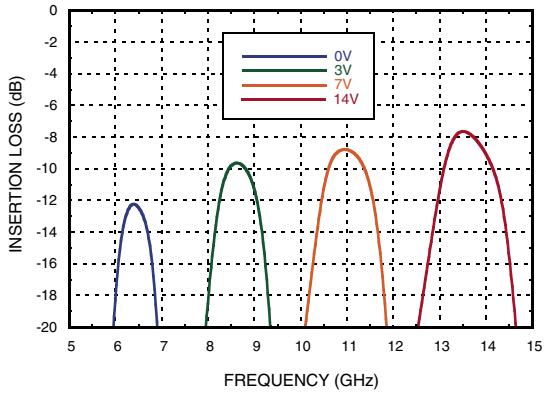
### Broadband Insertion Loss, Vfctl = Vnctl



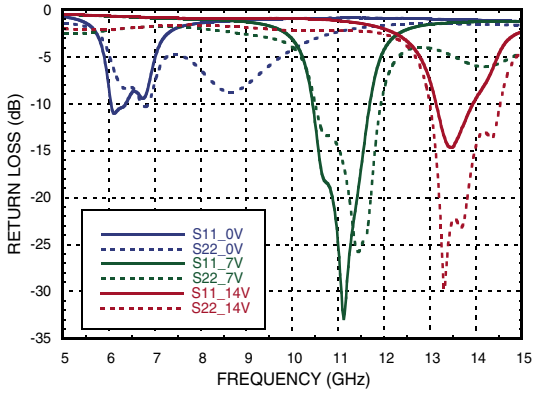

### Broadband Return Loss, Vfctl = Vnctl



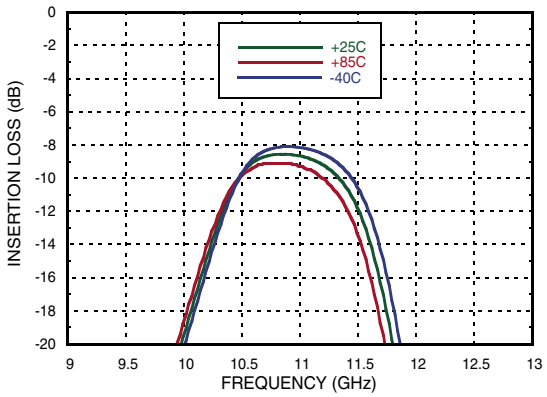

### Insertion Loss, Vfctl = Vnctl



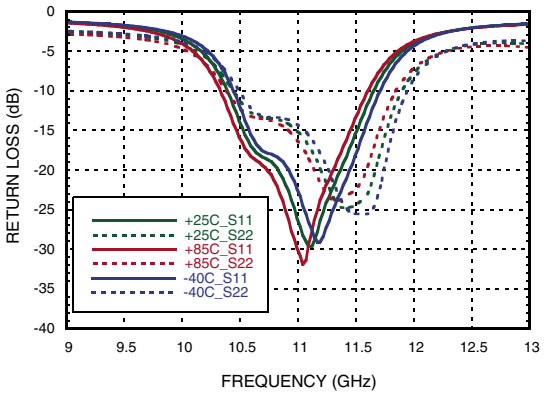

### Return Loss Vfctl, = Vnctl



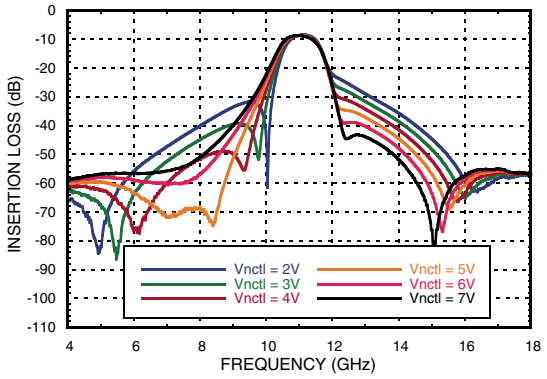

### Insertion Loss vs. Temperature Vfctl = Vnctl = 7V



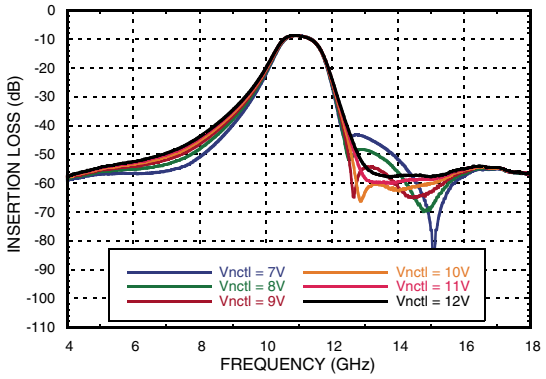

### Return Loss vs. Temperature Vfctl = Vnctl = 7V



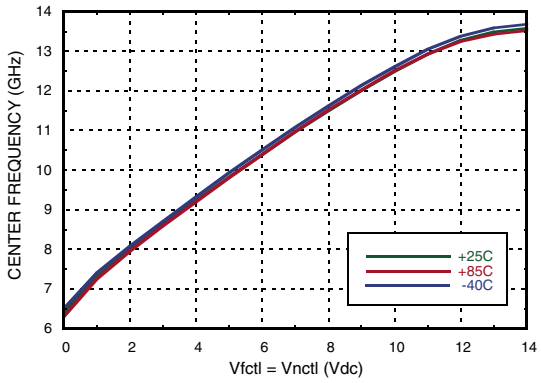
### Insertion Loss vs. Vnctl, Low Side Vfctl = 7V



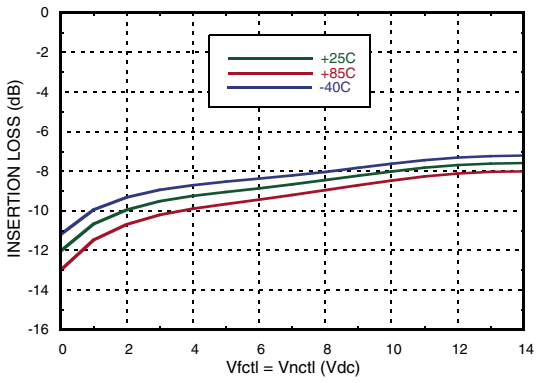

### Insertion Loss vs. Vnctl, High Side Vfctl = 7V



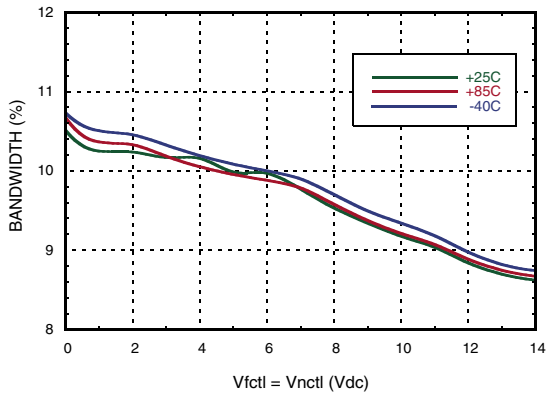

### Center Frequency vs. Temperature, Vfctl = Vnctl



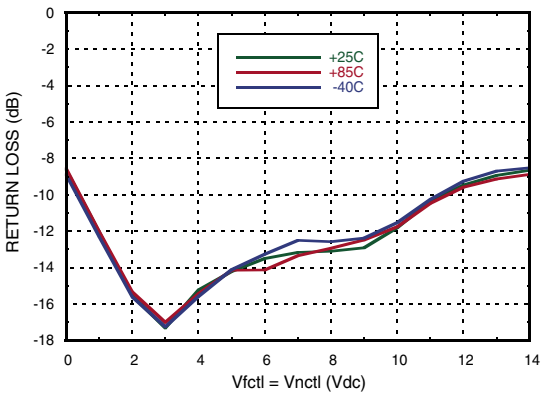

### Insertion Loss vs. Temperature, Vfctl = Vnctl



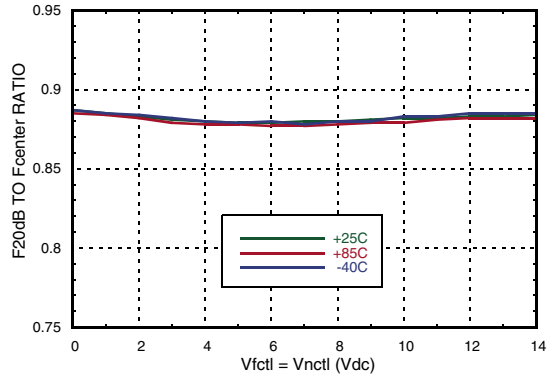

### 3 dB Bandwidth vs. Temperature, Vfctl = Vnctl



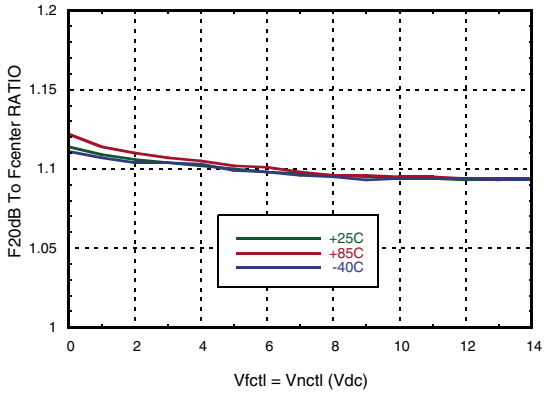

### Input Return Loss in a 2 dB Bandwidth vs. Temperature, Vfctl = Vnctl



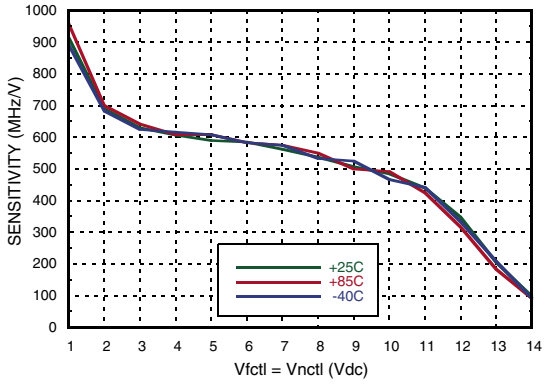
### Low Side Rejection Ratio vs. Temperature [1]



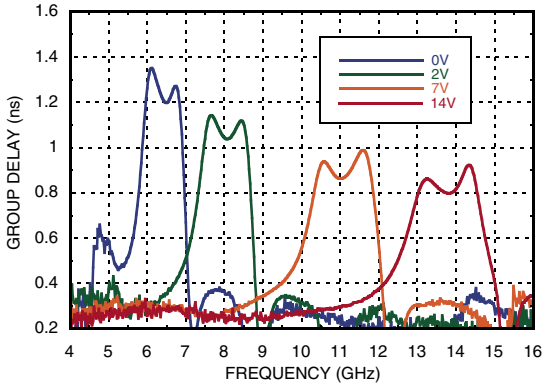

### High Side Rejection Ratio vs. Temperature [1]



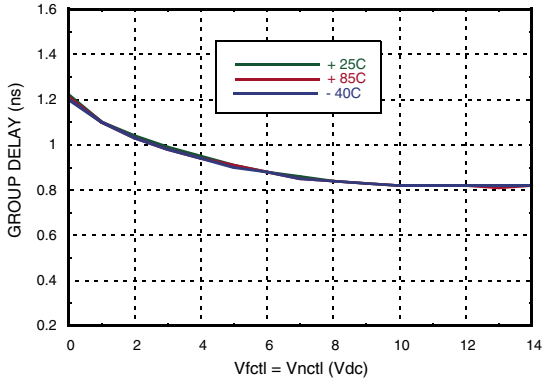

### Tuning Sensitivity vs. Temperature



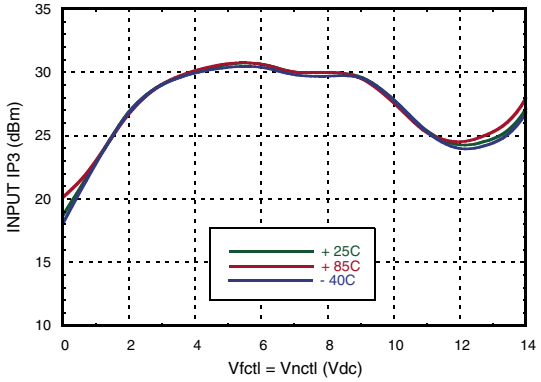

### Group Delay vs. Frequency




### Group Delay vs. Fcenter vs. Temperature




### Input IP3 vs. Temperature




1] Rejection ratio is defined as the ratio of the frequency at which the relative insertion loss is 20 dB to ƒcenter

# HMC895LP4E

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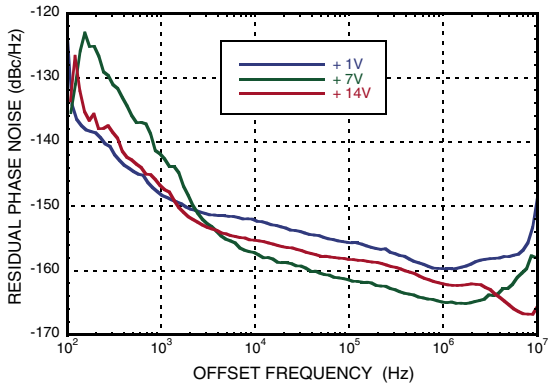
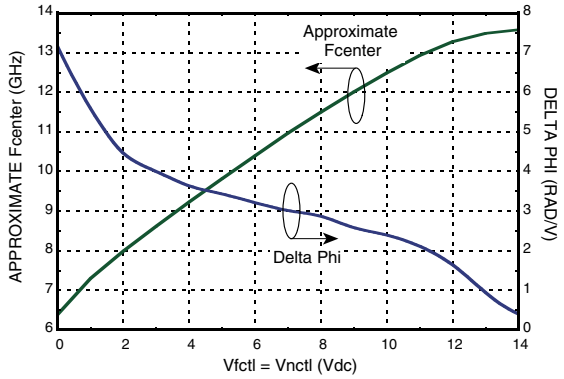
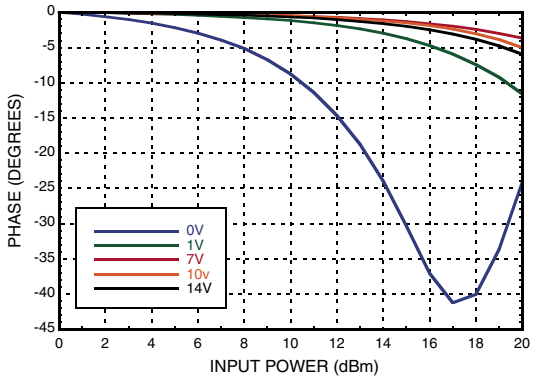
### Residual Phase Noise, Vfctl = Vnctl



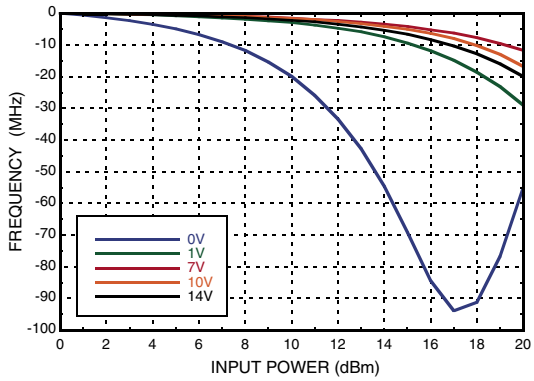

### Phase Sensitivity vs. Vfctl




### Insertion Phase Shift vs. Input Power Vfctl = Vnctl




### Fcenter vs. Input Power Vfctl = Vnctl




### Absolute Maximum Ratings

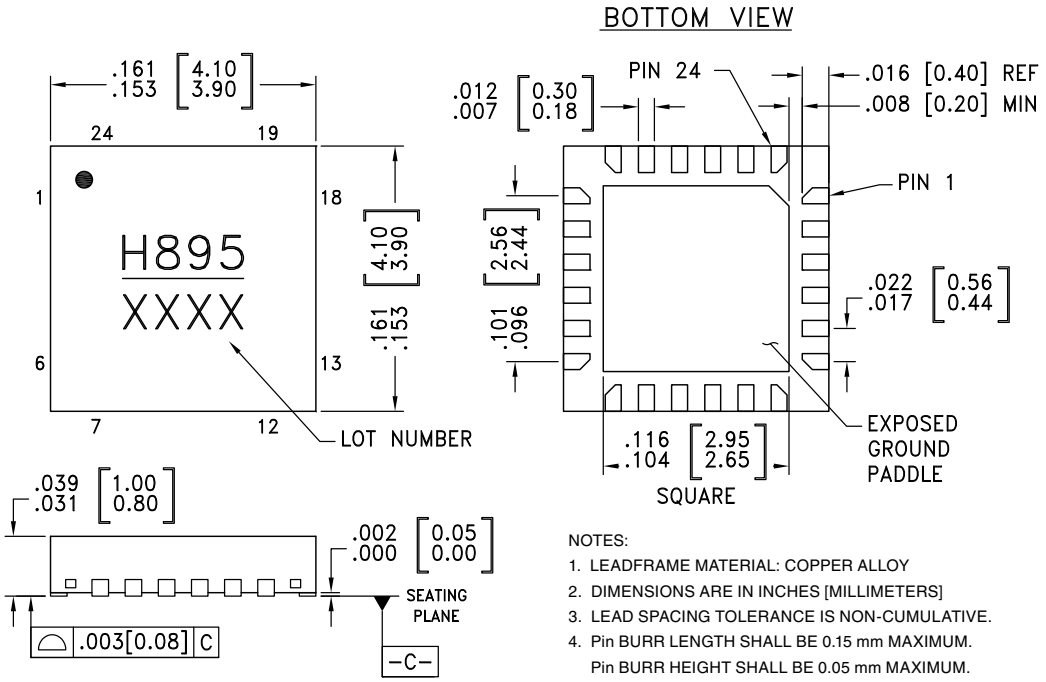
| | |
|---|---|
| Frequency Control Voltage (Vfctl) | -0.5 to +15V |
| Notch Control Voltage (Vnctl) | -0.5 to +15V |
| RF Power Input | 27 dBm |
| Storage Temperature | -65 to +150 °C |
| ESD Sensitivity (HBM) | 150V |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

### Reliability Information

| | |
|---|---|
| Junction Temperature to Maintain 1 Million Hour MTTF | 150 °C |
| Nominal Junction Temperature (T= 85 °C and Pin = 27 dBm) | 103 °C |
| Operating Temperature | -40 to +85 °C |

## Outline Drawing




NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. Pin BURR LENGTH SHALL BE 0.15 mm MAXIMUM. Pin BURR HEIGHT SHALL BE 0.05 mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

## Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [1] |
|---|---|---|---|---|
| HMC895LP4E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [2] | H895<br>XXXX |

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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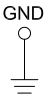
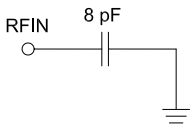
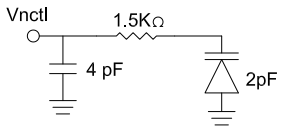
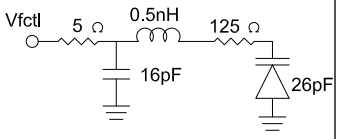
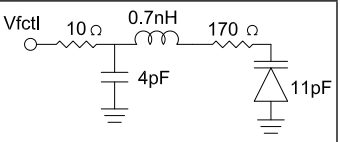
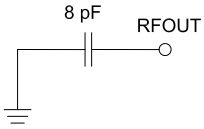
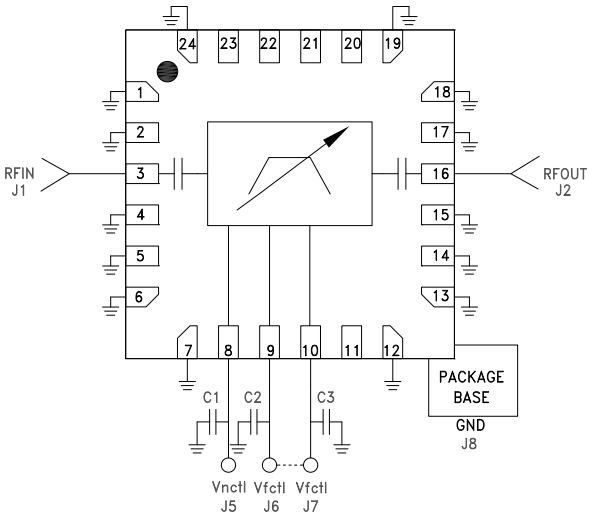
## Pin Descriptions

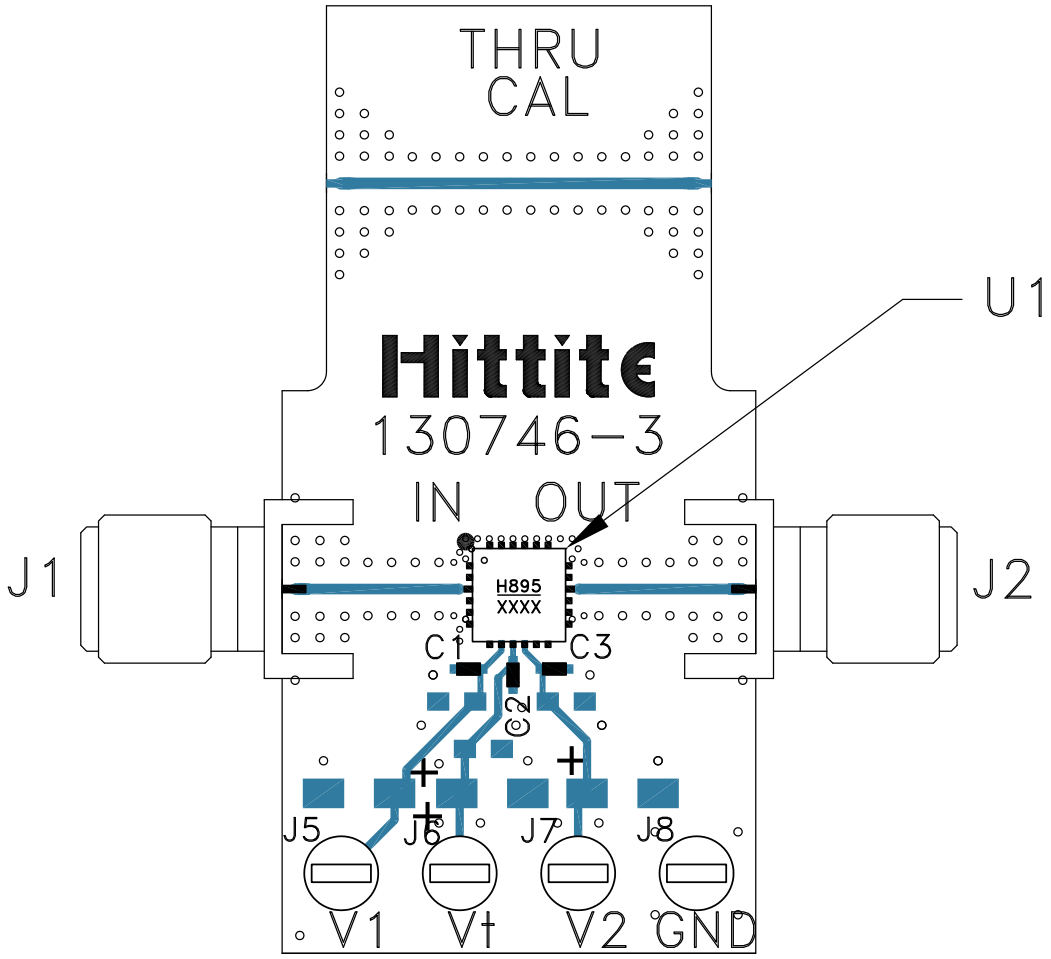
| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 2, 4 - 7, 12 - 15, 17 - 19, 24 | GND | These pins and exposed paddle must be connected to RF/DC ground. |   |
| 11, 20 - 23 | NC | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally | |
| 3 | RFIN | This pin is AC coupled and matched to 50 Ohms. |   |
| 8 | Vnctl | Low side/high side notch control voltage |   |
| 9 | Vfctl | Center frequency control voltage. For proper operation Pins 9 and10 must be connected together externally. |   |
| 10 | Vfctl | Center frequency control voltage. For proper operation Pins 9 and10 must be connected together externally. |   |
| 16 | RFOUT | This pin is AC coupled and matched to 50 Ohms. |   |

## Application Circuit




NOTE: FOR PROPER OPERATION PINS 9 AND 10 MUST BE CONNECTED TOGETHER EXTERNALLY.

## Evaluation PCB




## List of Materials for Evaluation PCB 129736 [1]

| Item | Description |
|---|---|
| J1, J2 | Connector, SMA, Female |
| J5,J6,J7, J8 | DC Pin |
| C1, C2, C3 | 100 pF Capacitor, 0402 Pkg. |
| U1 | HMC895LP4E Filter - Tunable |
| PCB [2] | 130746 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.