19-3098; Rev 0; 12/03

MAXIM

MAX1124 Evaluation Kit

Evaluates: MAX1121–MAX1124

General Description

The MAX1124 evaluation kit (EV kit) is a fully assembled and tested circuit board that contains all the components for evaluating the MAX1121 (8-bit, 250Msps), MAX1122 (10-bit, 170Msps), MAX1123 (10-bit, 210Msps), and MAX1124 (10-bit, 250Msps) analog-to-digital converters (ADCs). The MAX1121–MAX1124 accept differential analog input signals; however, the EV kit generates these signals from a user-provided single-ended signal source. The digital output produced by the ADCs can be easily captured with a user-provided high-speed logic analyzer or data-acquisition system. The EV kit operates from 1.8V and 3.3V power supplies. It includes circuitry that generates a differential clock signal from a user-provided AC signal. The EV kit comes with the MAX1124 installed. Contact the factory for free samples of the pin-compatible MAX1121/MAX1122/MAX1123 to evaluate these parts.

Features

- **Up to 250Msps Sampling Rate with the MAX1124**
- **Low Voltage and Power Operation**
- **Fully Differential Signal Input Configuration**
- **On-Board Differential Output Drivers**
- **Optional On-Board Secondary Transformer**
- **Fully Assembled and Tested**
- **Also Evaluates the MAX1121 (8-bit), MAX1122 (10-bit), and MAX1123 (10-bit)**

Part Selection Table

PART	RESOLUTION	SPEED (Msps)
MAX1121EGK	8	250
MAX1122EGK	10	170
MAX1123EGK	10	210
MAX1124EGK	10	250

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX1124EVKIT	0°C to +70°C	68 QFN

Note: *To evaluate the MAX1121/MAX1122/MAX1123, request a MAX1121EGK, MAX1122EGK, or MAX1123EGK free sample with the MAX1124 EV kit.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C11, C13–C16, C18, C19, C20, C36–C39	22	0.1µF ±20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M
C12, C17	0	Not installed (0402)
C21–C24	4	0.22µF ±20%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J224M
C25, C26	2	Not installed (0603)
C27, C28, C40	3	47µF ±20%, 10V tantalum capacitors (C-case) AVX TAJC476M010
C29, C30, C31, C41	4	10µF ±20%, 6.3V X5R ceramic capacitors (0805) TDK C2012X5R0J106M
C32, C33, C34, C42	4	1.0µF ±20%, 10V X5R ceramic capacitors (0603) TDK C1608X5R1A105M
C35	1	0.01µF ±20%, 25V X7R ceramic capacitor (0402) TDK C1005X7R1E103M
J1, J2, J3	3	SMA PC-mount connectors
J4–J7	4	Dual-row, 40-pin headers

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
JU1	0	Not installed
JU3, JU4, JU5	3	Jumper, 3-pin headers
R1, R2, R3	3	49.9Ω ±1% resistors (0603)
R4, R5	2	150Ω ±5% resistors (0603)
R6–R9	0	Not installed (0603)
R10–R15, R42, R43	0	Not installed (0603)
R16, R17	2	10Ω ±1% resistors (0603)
R18–R24, R28–R32, R34, R35	14	100Ω ±1% resistors (0603)
R25, R26, R27, R33	4	100Ω ±5% resistors (0603)
R36, R37	2	510Ω ±5% resistors (0603)
R38, R39, R41, R44–R68	28	510Ω ±5% resistors (0402)

DESIGNATION	QTY	DESCRIPTION
R40	1	Not installed
T1, T2	2	1:1 800MHz RF transformers Mini-Circuits ADT1-1WT
TP1, TP2	2	Test points (Black)
U1	1	Maxim MAX1124EGK (QFN-68)
U2	1	3.3V differential receiver (SO-8) Fairchild 100LVEL16M ON Semiconductor MC100LVEL16D
U3–U6	4	3.3V ECL quad differential receivers (SO-20) ON Semiconductor MC100LVEL17DW
Y1	0	Not installed
None	3	Shunts
None	1	MAX1124 PC board

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
Fairchild	888-522-5372	—	www.fairchildsemi.com
Mini-Circuits	718-934-4500	718-332-4661	www.minicircuits.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com

Note: *Please indicate that you are using the MAX1124 when contacting these component suppliers.*

Quick Start

Recommended Equipment

- DC power supplies:
  - Analog (VCC) 1.8V, 300mA
  - Clock (VCLK) 3.3V, 150mA
  - Buffers (VPECL) 3.3V, 350mA
- Signal generator with low phase noise and low jitter for clock input (e.g., HP8662A, HP8644B)
- Signal generator for analog signal input (e.g., HP8662A, HP8644B)
- Logic analyzer or data-acquisition system (e.g., HP16500C, TLA621)
- Digital voltmeter

Procedure

The MAX1124 EV kit is a fully assembled and tested surface-mount board. Follow the steps below for board operation. **Do not turn on power supplies or enable signal generators until all connections are completed:**

1) Verify that shunts are installed in the following locations:
   - JU3 (2-3)—two's complement output
   - JU4 (1-2)—divide-by-two disabled
   - JU5 (2-3)—internal reference enabled
2) Connect the clock signal generator to the SMA connector labeled J2.
3) Connect the analog input signal generator to the SMA connector labeled J3.
4) Connect the logic analyzer to either headers J4/J5

(LVDS-compatible signals) or J6/J7 (LVPECL-compatible signals). See the *Output Bit Locations* section for header connections.

5) Connect a 1.8V, 300mA power supply to VCC. Connect the ground terminal of this supply to GND.
6) Connect a 3.3V, 150mA power supply to VCLK. Connect the ground terminal of this supply to GND.
7) Connect a 3.3V, 350mA power supply to VPECL. Connect the ground terminal of this supply to GND.
8) Turn on all of the power supplies.
9) Enable the signal generators. Set the clock signal generator to output a 250MHz signal with an amplitude of 2.4V_{P-P}. Set the analog input signal generators to output the desired frequency with an amplitude ≤ 2V_{P-P}. The signal generators should be phase-locked.
10) Enable the logic analyzer.
11) Collect data using the logic analyzer.

Detailed Description

The MAX1124 EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1121 (8-bit, 250Msps), MAX1122 (10-bit, 170Msps), MAX1123 (10-bit, 210Msps), and MAX1124 (10-bit, 250Msps) LVDS-output ADCs. The EV kit comes with the MAX1124 installed, which can be evaluated with a maximum clock frequency (f_{CLK}) of 250MHz. The MAX1124 accepts differential input signals; however, an on-board transformer (T2) converts a readily available single-ended source output to the required differential signal.

Output level translators (U3–U6) buffer and convert the LVDS output signals of the MAX1124 to higher-voltage LVPECL signals, which can be captured by a wide variety of logic analyzers. The LVDS outputs are accessed at headers J4 and J5. The LVPECL outputs are accessed at headers J6 and J7.

The EV kit is designed as a four-layer PC board to optimize the performance of the MAX1124. Separate analog, clock, and buffer power planes minimize noise-coupling between analog and digital signals. For analog and clock inputs, 50Ω coplanar transmission lines are used. For all digital LVDS outputs, 100Ω differential coplanar transmission lines are used. All LVDS differential outputs are properly terminated with 100Ω termination resistors between true and complementary digital outputs. The trace lengths of the 100Ω differential LVDS lines are matched to within a few thousandths of an inch to minimize layout-dependent delays.

Power Supplies

The MAX1124 EV kit requires separate analog, clock, and buffer power supplies for best performance. A 1.8V power supply is used to power the analog and digital portion of the MAX1124. The on-board clock circuitry is powered by a 3.3V power supply. A separate 3.3V power supply is used to power the output buffers (U3–U6) of the EV kit.

Clock

The MAX1124 requires a differential clock input signal. An on-board clock-shaping circuit generates a differential clock signal from an AC sine-wave signal applied to the clock-input SMA connector (J2). The input signal should not exceed an amplitude of 2.6V_{P-P}. The frequency of the signal should not exceed 250MHz for the MAX1124. The frequency of the sinusoidal input signal determines the sampling frequency (f_{CLK}) of the ADC. A differential line receiver (U2), processes the input signal to generate the required clock signal.

Clock Divider

The MAX1124 features an internal divide-by-two clock divider. Use jumper JU4 to enable/disable this feature. See Table 1 for shunt positions.

Input Signal

The MAX1124 accepts differential analog input signals. The MAX1124 EV kit only requires a single-ended analog input signal with an amplitude ≤2V_{P-P} provided by the user. An on-board transformer takes the single-ended analog input and generates a differential analog signal at the ADCs differential input pins.

Table 1. Clock Divider Shunt Settings (JU4)

SHUNT POSITION	MAX1124 CLKDIV PIN	DESCRIPTION
1-2*	VCC	Clock signal divided by 1
2-3	GND	Clock signal divided by 2

**Default Configuration: JU4 (1-2).*

Optional Secondary Input Transformer

Using the optional on-board secondary transformer can reduce common-mode signal levels and marginally improve performance of the MAX1124. To use this transformer, follow the directions below:

1) Cut the trace at R43.
2) Install 0Ω resistors at R10 and R12.
3) Remove C14.
4) Connect the analog signal source to J1 instead of J3.

Reference Voltage

There are two methods to set the full-scale range of the MAX1124. The MAX1124 EV kit can be configured to use the MAX1124's internal reference, or a stable, low-noise external reference can be applied to the REFIO pad. Jumper JU5 controls which reference source is used. See Table 2 for shunt settings.

Table 2. Reference Shunt Settings (JU5)

SHUNT POSITION	DESCRIPTION
1-2	Internal reference disabled; apply a stable reference voltage at the REFIO pad
2-3*	Internal reference enabled

*****Default configuration: JU5 (2-3).*

Output Signal

The MAX1124 features a single,10-bit, parallel, LVDS-compatible, digital output bus. The digital outputs also feature a clock bit (CLK) for data synchronization, and a data overrange bit. See the *Output Bit Locations* section for header connections.

Output Format

The digital output coding can be chosen to be either in two's complement or straight offset binary format by configuring jumper JU3. See Table 3 for shunt settings.

Table 3. Output Format Shunt Settings (JU3)

SHUNT POSITION	MAX1124 $\overline{T}$/B PIN	DESCRIPTION
1-2	VCC	Digital output in straight offset binary
2-3*	GND	Digital output in two's complement

*****Default configuration: JU3 (2-3).*

Output Bit Locations

The digital outputs of the ADC are connected to two 40-pin headers (J4 and J5). PC board trace lengths are matched to minimize output skew and improve performance of the device. In addition, four drivers (U3–U6) buffer and level-translate the ADC's digital outputs to LVPECL-compatible signals. The drivers increase the differential voltage swing, and are able to drive large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to two 40-pin headers (J6 and J7). See Table 4 for header J4–J7 bit locations.

Table 4. Output Bit Locations (MAX1122/MAX1123/MAX1124) (JU3)

BIT		UNBUFFERED (LVDS)	BUFFERED (LVPECL)	DESCRIPTION
D9	P	J6-10	J4-10	MSB
	N	J6-9	J4-9	
D8	P	J6-16	J4-16	Data bits
	N	J6-15	J4-15	
D7	P	J6-22	J4-22	
	N	J6-21	J4-21	
D6	P	J6-28	J4-28	
	N	J6-27	J4-27	
D5	P	J6-34	J4-34	
	N	J6-33	J4-33	
D4	P	J6-40	J4-40	
	N	J6-39	J4-39	
D3	P	J7-8	J5-8	
	N	J7-7	J5-7	
D2	P	J7-14	J5-14	
	N	J7-13	J5-13	
D1	P	J7-20	J5-20	
	N	J7-19	J5-19	
D0	P	J7-26	J5-26	LSB
	N	J7-25	J5-25	
OR	P	J6-4	J4-4	Overrange bit
	N	J6-3	J4-3	
DCO	P	J7-2	J5-2	Clock output signal
	N	J7-1	J5-1	

*****Default configuration: JU3 (2-3).*

Evaluating the MAX1121/MAX1122/MAX1123

The MAX1124 EV kit is also capable of evaluating the MAX1121/MAX1122/MAX1123. To evaluate the MAX1121, MAX1122, or MAX1123, replace the MAX1124 with the desired IC.

When evaluating the 8-bit MAX1121, do not connect the logic analyzer to the header pins marked D0 and D1. See Table 5 for output bit locations of headers J4–J7.

Table 5. Output Bit Locations (MAX1121)

BIT		UNBUFFERED (LVDS)	BUFFERED (LVPECL)	DESCRIPTION
D7	P	J6-10	J4-10	MSB
	N	J6-9	J4-9	
D6	P	J6-16	J4-16	Data bits
	N	J6-15	J4-15	
D5	P	J6-22	J4-22	
	N	J6-21	J4-21	
D4	P	J6-28	J4-28	
	N	J6-27	J4-27	
D3	P	J6-34	J4-34	
	N	J6-33	J4-33	
D2	P	J6-40	J4-40	
	N	J6-39	J4-39	
D1	P	J7-8	J5-8	
	N	J7-7	J5-7	
D0	P	J7-14	J5-14	LSB
	N	J7-13	J5-13	
OR	P	J6-4	J4-4	Overrange bit
	N	J6-3	J4-3	
DCO	P	J7-2	J5-2	Clock output signal
	N	J7-1	J5-1	

MAX1124 Evaluation Kit

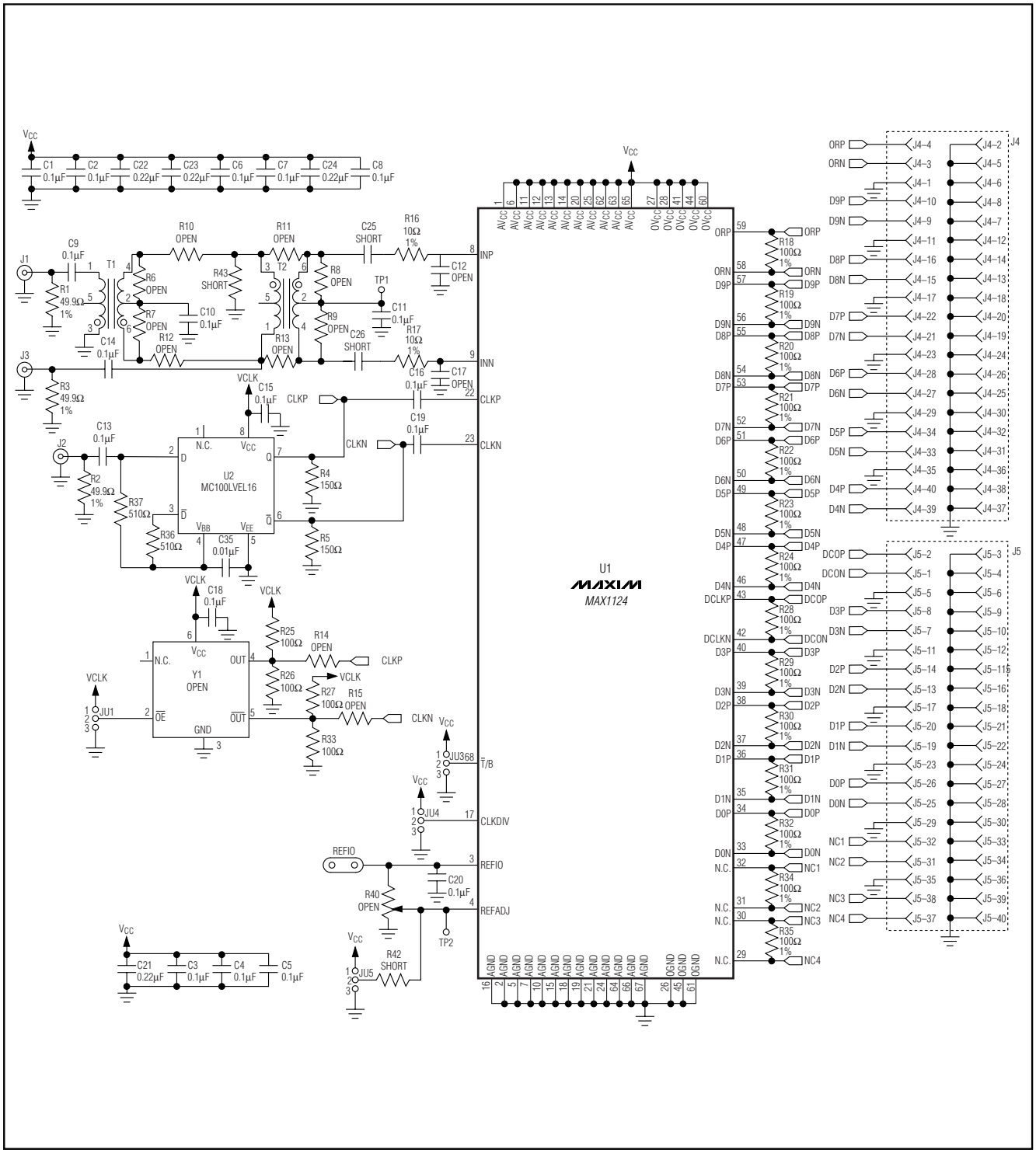

Figure 1. MAX1124 EV Kit Schematic (Sheet 1 of 3)

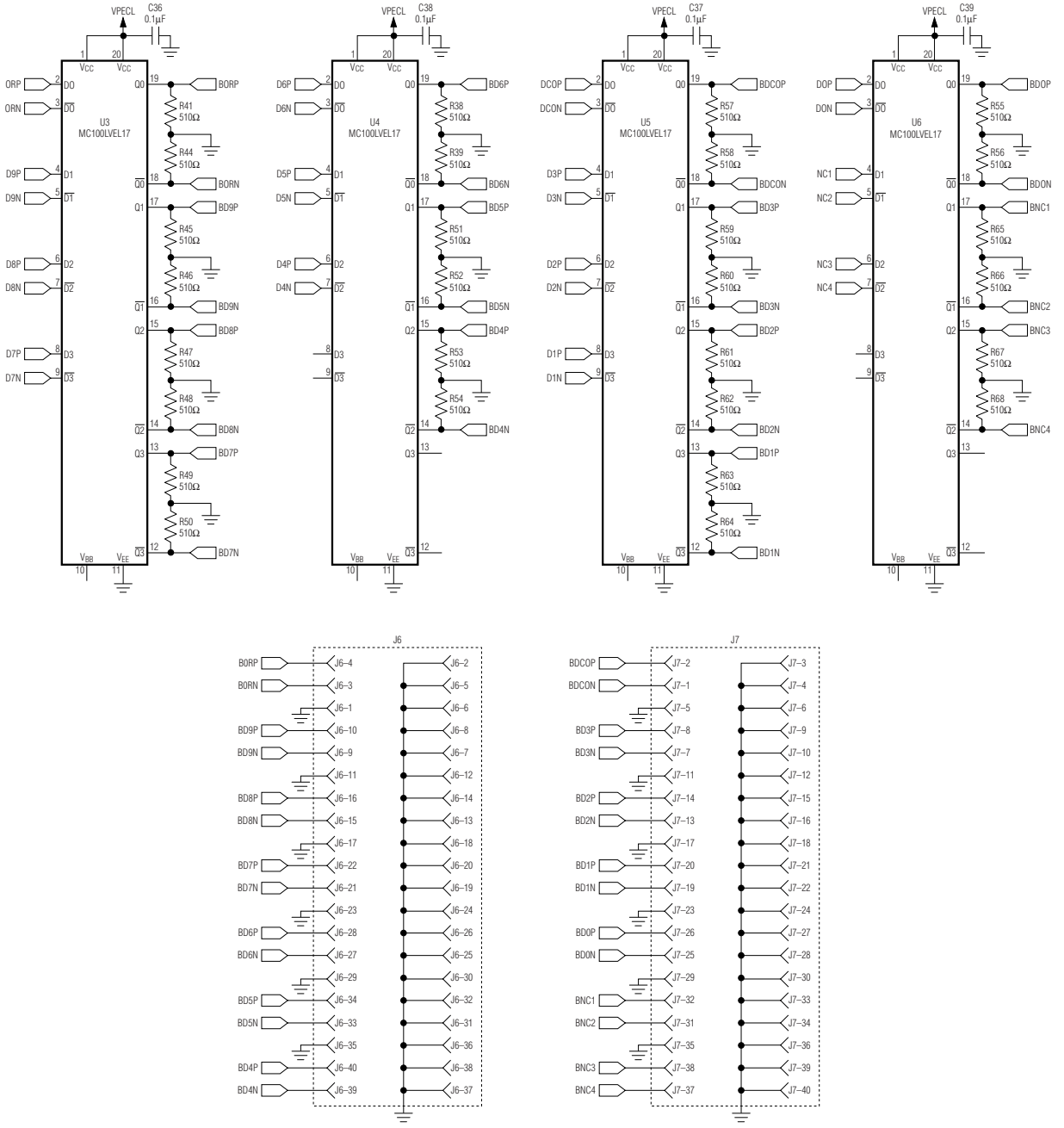

Figure 1. MAX1124 EV Kit Schematic (Sheet 2 of 3)

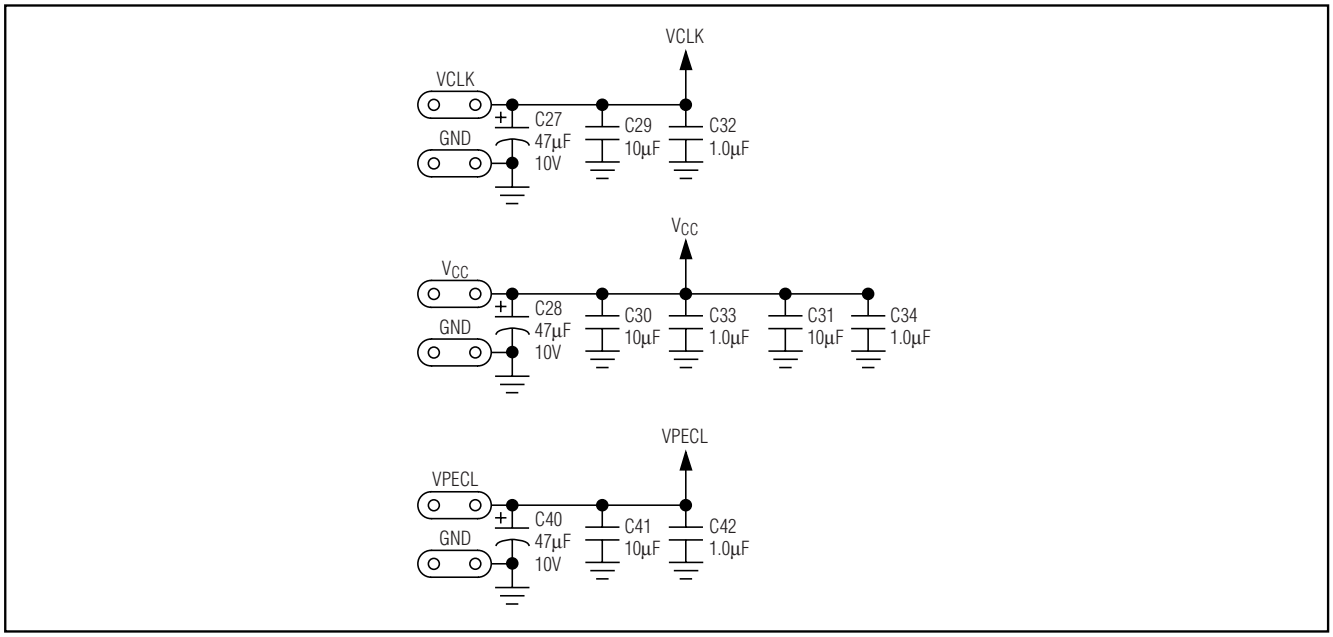

Figure 1. MAX1124 EV Kit Schematic (Sheet 3 of 3)

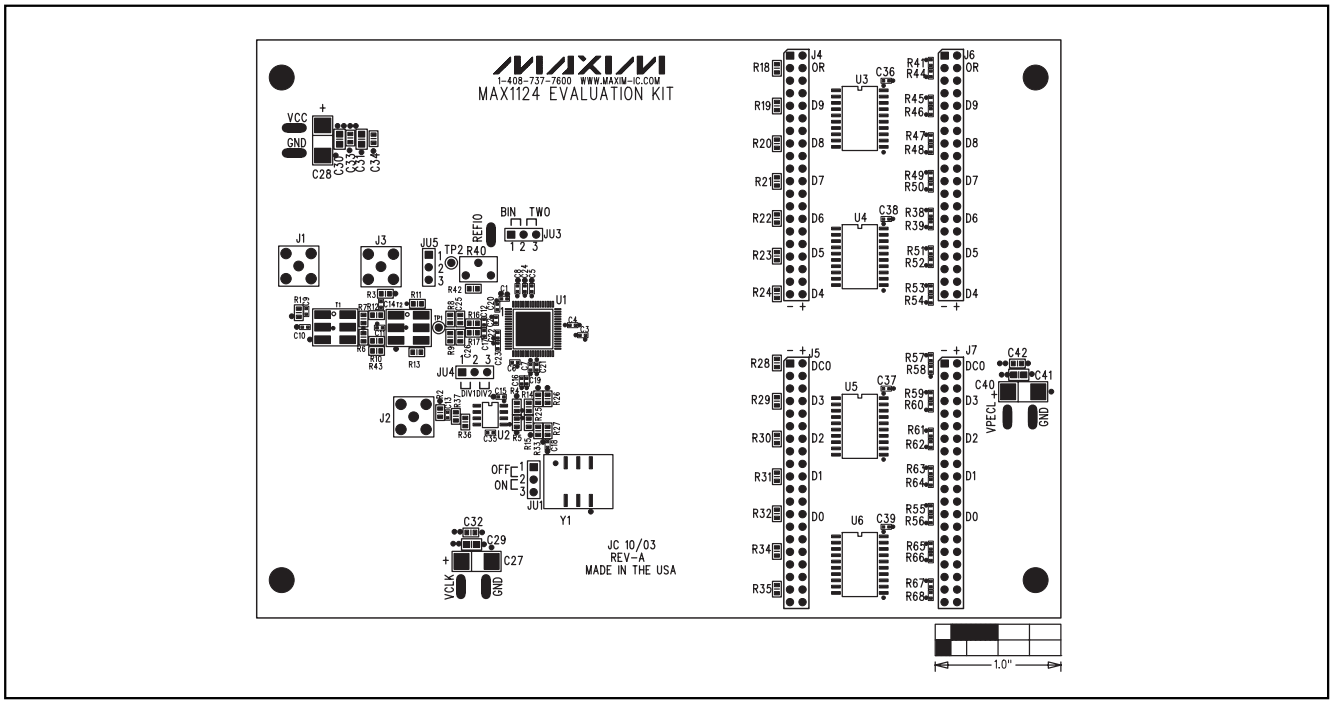

Figure 2. Component Placement Guide—Component Side

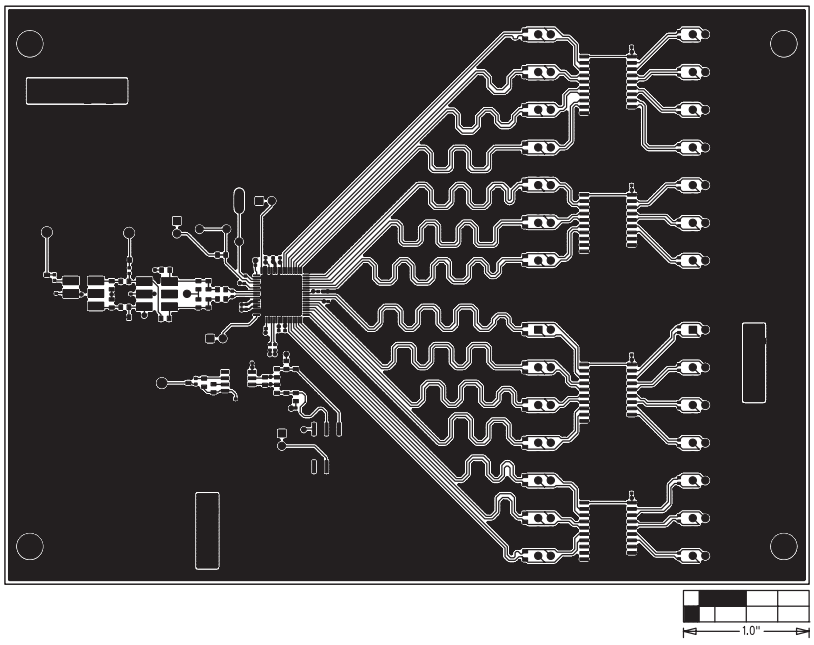

Figure 3. PC Board Layout—Component Side

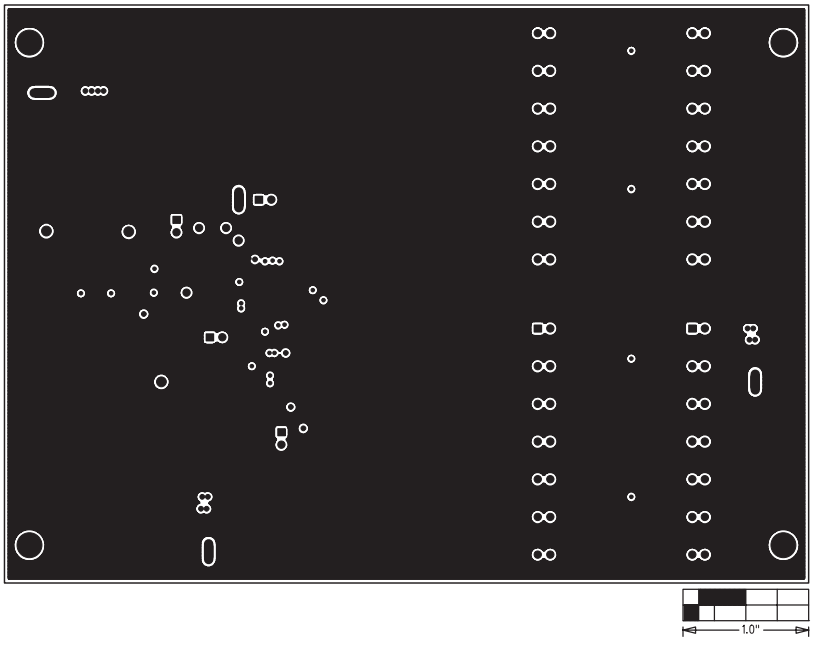

Figure 4. PC Board Layout (Inner Layer 2)—Ground Planes

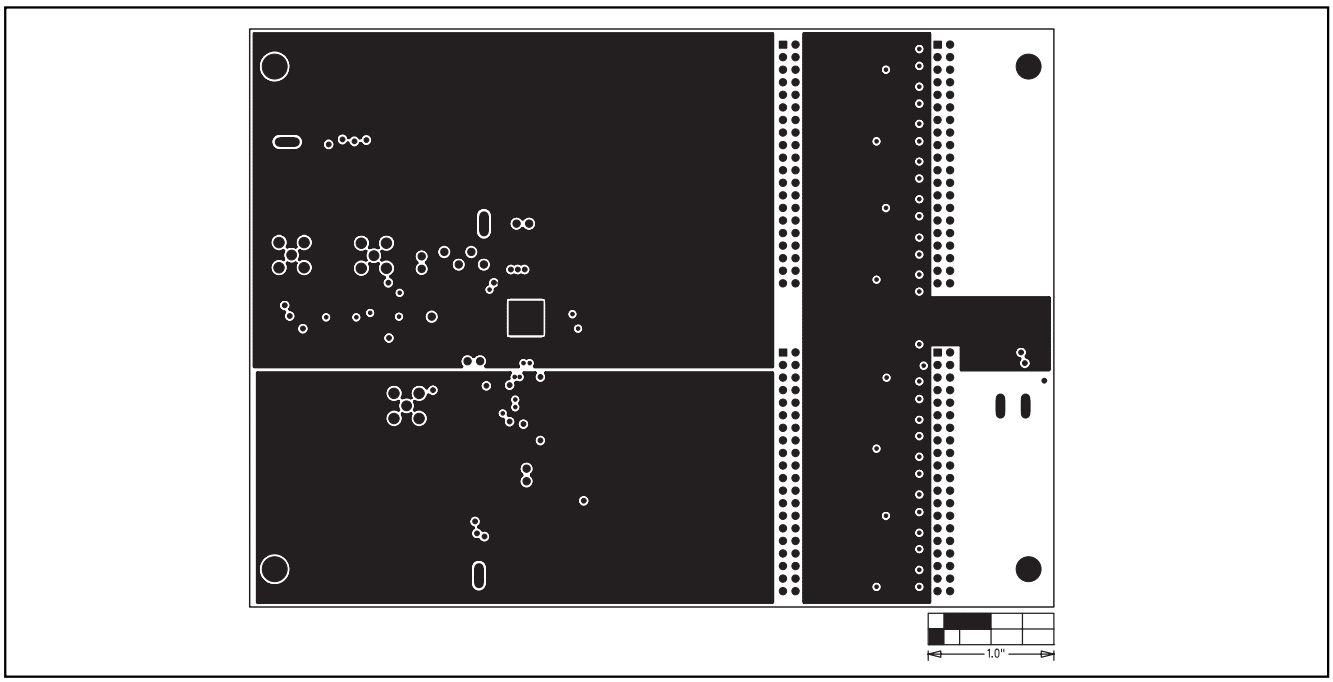

Figure 5. PC Board Layout (Inner Layer 3)—Power Planes

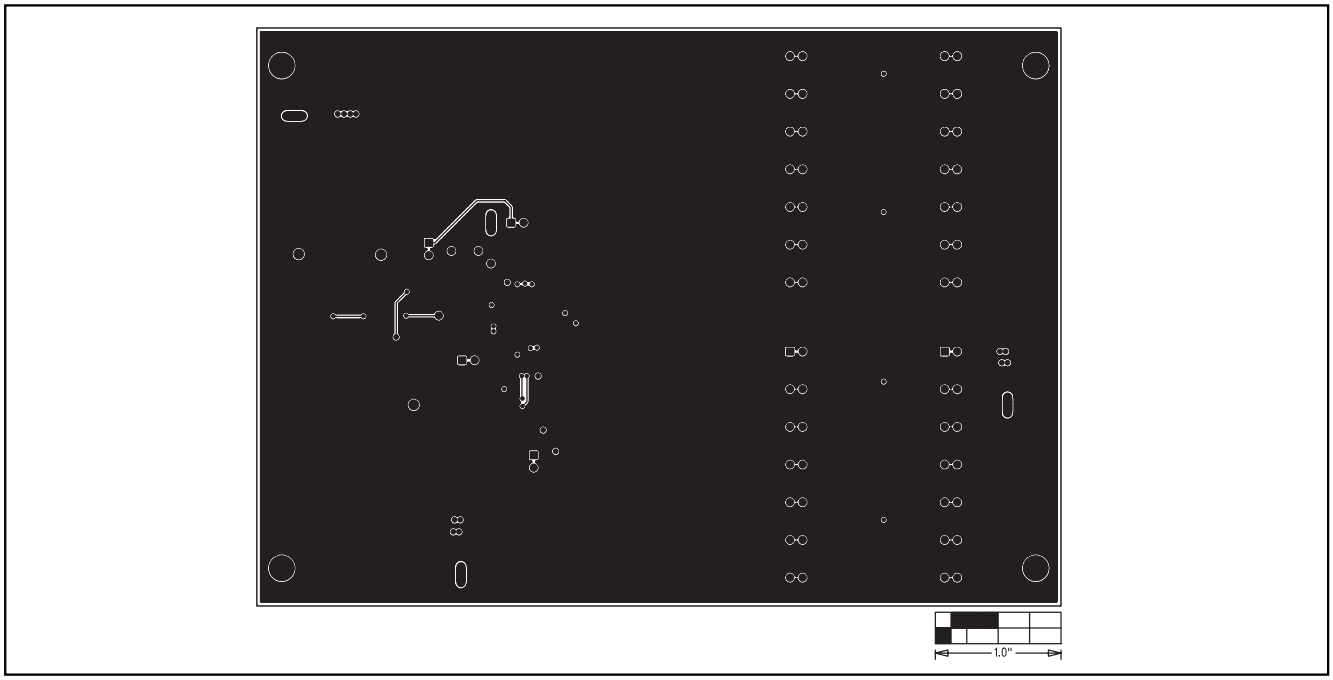

Figure 6. PC Board Layout—Solder Side