TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

36M 2.5V Pipelined N*t*RAM™ 1M Word by 36Bit SYNCHRONOUS NO-TURNAROUND STATIC RAM

DESCRIPTION

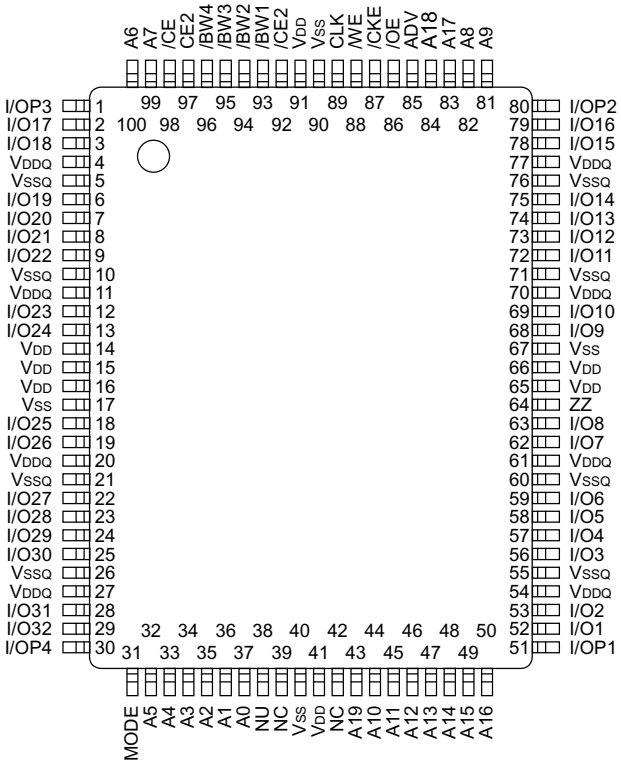
The TC55WDM536AFFN is a synchronous static random access memory (SRAM) organized as 1,048,576 words by 36 bits. NtRAM™(no-turnaround SRAM) offers high bandwidth by eliminating dead cycles during the transition from a read to a write and vice versa. All inputs except Output Enable $\overline{OE}$ and the Snooze pin ZZ are synchronized with the rising edge of the CLK input. A Read operation is initiated by the ADV Address Advanced Input signal ; the input from the address pins and all control pins except the $\overline{OE}$ and ZZ pins are loaded into the internal registers on the rising edge of CLK in the cycle in which ADV is asserted. The output data is available two clock cycles later. Write operations are internally self-timed and are initiated by the rising edge of CLK in the cycle in which ADV is asserted. The input from the address pins and all control pins except the $\overline{OE}$ and ZZ pins are loaded into the internal registers on the rising edge of CLK in the cycle in which ADV is asserted. Input data is loaded in the third cycle after the cycle in which ADV is asserted. Byte Write Enables ($\overline{BW1}$ to $\overline{BW4}$) allow from one to four Byte Write operations to be performed. A 2-bit burst address counter and control logic are integrated into this SRAM. The TC55WDM536AFFN uses a single power supply (2.5V) and is available in a 100-pin low-profile plastic QFP (LQFP).

FEATURES

- Organized as 1,048,576 words by 36 bits
- No-turnaround operation with pipeline data output
- 2-bit burst address counter
  (support for interleaved or linear burst sequences)
- Synchronous self-timed Write
- Byte Write control
- Snooze mode pin (ZZ) for power down
- LVTTL-compatible interface
- Single 2.5V ±5% power supply V_{DD} and V_{DDQ}
- Available in 100-pin LQFP package (LQFP100-P-1420-0.65B ; ,weight : grams (typical))

		225	200	167	150	MHz
Clock Cycle Time	t_{KC}	4.4	5.0	6.0	6.6	ns
Clock Access Time	t_{KQV}	2.8	3.2	3.5	3.8	ns
Operating Current	I_{DDO1}	TBD				mA

PIN ASSIGNMENT (TOP VIEW)

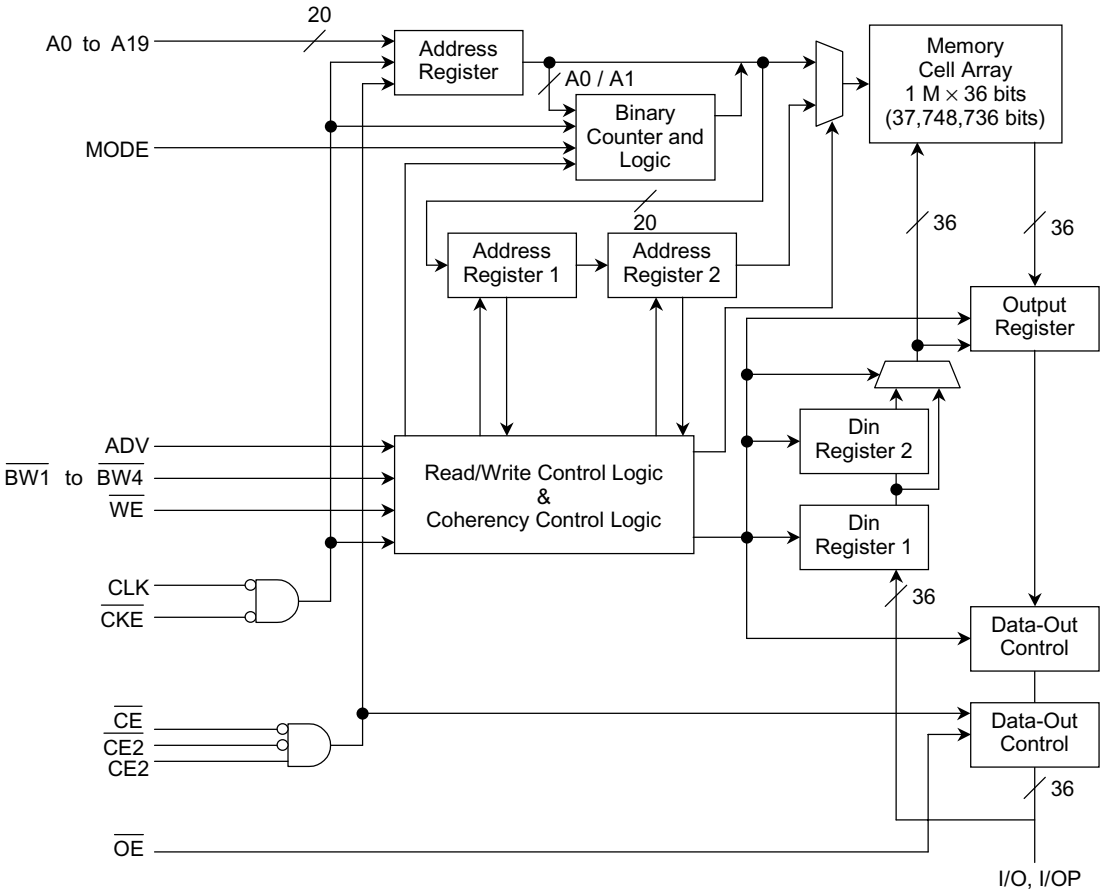


PIN NAMES

CLK	Clock Input
A0 to A19	Address Inputs
$\overline{CE}$, $\overline{CE2}$, CE2	Chip Enable Inputs
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable input
$\overline{BW1}$ to $\overline{BW4}$	Byte Write Enable
ADV	Address Advance Input
$\overline{CKE}$	Clock Enable
ZZ	Snooze Input
I/O1 to I/O32	Data Inputs/Outputs
I/OP1 to I/OP4	Parity Data Inputs/Outputs
MODE	Mode select Input
NC	No Connection
NU	Not Usable
V_{DD}	Power Supply for Core
V_{DDQ}	Power Supply for Output Buffer
V_{SS}	Ground for Core
V_{SSQ}	Ground for Output Buffer

Note : N*t*RAM™ and No-Turnaround Random Access Memory are trademarks of Samsung Electronics Co., Ltd..

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
89	CLK	Input (NA)	**Clock Input** All synchronous input signals are registered on the rising edge of CLK. When the chip is enabled, address inputs and control pins except for $\overline{OE}$ and ZZ must meet the specified setup and hold times with respect to the CLK rising edge.
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83,84,43	A0 to A19	Input (synchronous)	**Address Inputs** These address inputs are registered on the rising edge of CLK. When the chip is enabled, address inputs must meet the specified setup and hold times with respect to the CLK rising edge.
98	$\overline{CE}$	Input (synchronous)	**Chip Enable Input** This active-Low signal controls the chip status (enabled or disabled). It is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input (synchronous)	**Chip Enable Input** This active-Low signal controls the chip status (enabled or disabled). It is sampled only when a new external address is loaded.
97	CE2	Input (synchronous)	**Chip Enable Input** This active-High signal controls the chip status (enabled or disabled). It is sampled only when a new external address is loaded.
86	$\overline{OE}$	Input (asynchronous)	**Output Enable Input** This active-Low signal controls all 36 bits of the I/O output buffer.
88	$\overline{WE}$	Input (synchronous)	**Write Enable Input** This active-Low input controls Read/Write operations.
93, 94, 95, 96	$\overline{BW1}$ to $\overline{BW4}$	Input (synchronous)	**Byte Write Enable** These active-Low inputs control Byte Write operations when a Write cycle is active. A Byte Write pin controls I/O pins as follows. $\overline{BW1}$: I/O1 to I/O8, I/OP1 $\overline{BW2}$: I/O9 to I/O16, I/OP2 $\overline{BW3}$: I/O17 to I/O24, I/OP3 $\overline{BW4}$: I/O25 to I/O32, I/OP4
85	ADV	Input (synchronous)	**Address Advance Input** This is used to load the internal registers with the input from the address and control signals when it is Low on the rising edge of CLK. When it is High, the internal burst address counter is incremented. The external address inputs are ignored when this signal is High.
87	$\overline{CKE}$	Input (synchronous)	**Clock Enable** When High, CLK input is ignored and outputs retain the same state.
64	ZZ	Input (asynchronous)	**Snooze Input** This active-High signal is used to place the device into Sleep Mode (Low-Power Standby Mode). When Low, the device remains in the Active state. When High, the device goes into the Sleep state and memory data is retained. After this signal has been de-asserted, the device will wake up when a read or write operation is initiated by ADV.

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	I/O1 to I/O32	I/O (synchronous)	**Data Input/Output**
51, 80, 1, 30	I/OP1 to I/OP4	I/O (synchronous)	**Parity Data Input/Output**
31	MODE	Input (synchronous)	**Mode Select Input** This signal selects the burst sequence. When High, the burst sequence is interleaved. When Low, it is linear.
39, 42	NC	NC	**Not Connected**
38	NU	Input (asynchronous)	**Not Usable**
14, 15, 16, 41, 65, 66, 91	VDD	Supply	**Power Supply for Core**
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	Supply	**Power Supply for Output Buffers**
17, 40, 67, 90	VSS	Ground	**Ground for Core**
5, 10, 21, 26, 55, 60, 71, 76	VSSQ	Ground	**Ground for Output Buffers**

OPERATING MODE

(1) Synchronous Input Truth Table

OPERATION	$\overline{WE}$	ADV	CE	$\overline{BW}$	Addr. Used	$\overline{CKE}$	ZZ	I/O (2 cycles later)
Read (begin burst)	H	L	Select	X	External	L	L	Output
Read (continue burst)	X	H	X	X	Internal	L	L	Output
Write (begin burst)	L	L	Select	L	External	L	L	Input
Write (continue burst)	X	H	X	L	Internal	L	L	Input
NOP/Write Abort (begin burst)	L	L	Select	H	X	L	L	Hi-Z
Write Abort (continue burst)	X	H	X	H	Internal	L	L	Hi-Z
Deselected	X	L	Deselect	X	X	L	L	Hi-Z
Deselect Continue (Note 2)	X	H	X	X	X	L	L	Hi-Z
Ignore Clock Edge (Note 3)	X	X	X	X	X	H	L	Previous value
Snooze	X	X	X	X	X	X	H	Hi-Z

Notes: 1. H means logical High and L means logical Low. X means Don't care.
2. A Deselect Continue cycle can only be entered if a Deselect cycle is executed before it.
3. When the Ignore Clock Edge command is asserted during a Read operation, the output data for the previous cycle still appear on the I/O pins. When the command is asserted during a Write operation, the I/O pins remain at Hi-Z and the Write operation is not executed.
4. All synchronous Inputs must exhibit adequate setup and hold times either side of the rising edge of the CLK pin.
5. ZZ input is asynchronous, but is included is this table.

(2) Write Enable Truth Table

OPERATION	$\overline{WE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	I/O1 to I/O8 I/OP1	I/O9 to I/O16 I/OP2	I/O17 to I/O24 I/OP3	I/O25 to I/O32 I/OP4
Read	H	X	X	X	X	Output	Output	Output	Output
Write	L	L	L	L	L	Input	Input	Input	Input
	L	L	H	H	H	Input	Hi-Z	Hi-Z	Hi-Z
	L	H	L	H	H	Hi-Z	Input	Hi-Z	Hi-Z
	L	H	H	L	H	Hi-Z	Hi-Z	Input	Hi-Z
	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	Input
	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes: 1. H means logical High and L means logical Low. X means Don't care.
2. The status for I/O pins described in this column appears two clock cycles after the cycle in which the Read or Write command is asserted.

(3) Asynchronous Inputs Truth Table

OPERATION	$\overline{OE}$	ZZ	I/O
Read	L	L	Dout
	H	L	Hi-Z
Write	X	L	Din, Hi-Z
Stop clock (Note 2)	H	L	Hi-Z
	L	L	Low-Z
Snooze (Note 3)	X	H	Hi-Z

Notes: 1. H means logical High and L means logical Low. X means Don't care.
2. The Stop CLK Mode achieves Low-Power Standby by stopping the input clock.
3. The Snooze Mode achieves Low-Power Standby by asserting the ZZ pin.
4. The cycle immediately prior to a Snooze brought about by the ZZ pin must be a Read Mode or Deselect Mode cycle.
5. Memory data is retained during Snooze Mode cycles.

(4) Burst Sequence

MODE PIN	BURST OPERATION
L	Linear burst order
H or NC	Interleaved burst order

a) Linear Burst Sequence (MODE input = V_{SS})

Bit Order : A_{19} - - - - - - - - - A_1 A_0

1st Address (external)	2nd Address (internal)	3rd Address (internal)	4th Address (internal)
XX - - - - - - XX00	XX - - - - - - XX01	XX - - - - - - XX10	XX - - - - - - XX11
XX - - - - - - XX01	XX - - - - - - XX10	XX - - - - - - XX11	XX - - - - - - XX00
XX - - - - - - XX10	XX - - - - - - XX11	XX - - - - - - XX00	XX - - - - - - XX01
XX - - - - - - XX11	XX - - - - - - XX00	XX - - - - - - XX01	XX - - - - - - XX10

b) Interleaved Burst Sequence (MODE input = V_{DD} or NC)

Bit Order : A_{19} - - - - - - - - - A_1 A_0

1st Address (external)	2nd Address (internal)	3rd Address (internal)	4th Address (internal)
XX - - - - - - XX00	XX - - - - - - XX01	XX - - - - - - XX10	XX - - - - - - XX11
XX - - - - - - XX01	XX - - - - - - XX00	XX - - - - - - XX11	XX - - - - - - XX10
XX - - - - - - XX10	XX - - - - - - XX11	XX - - - - - - XX00	XX - - - - - - XX01
XX - - - - - - XX11	XX - - - - - - XX10	XX - - - - - - XX01	XX - - - - - - XX00

DEVICE OPERATION

(1) Read Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	X	L	L	X	L	X	Address & control valid
n + 1	X	X	X	X	X	X	L	X	
n + 2	X	X	X	X	X	L	X	Q0	Read out A0

Notes: 1. H means logical High and L means logical Low. X means Don't care. Q is data output.

(2) Burst Read Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	X	L	L	X	L	X	Address & control valid
n + 1	X	X	X	H	X	X	L	X	
n + 2	X	X	X	H	X	L	L	Q0	Read out A0
n + 3	X	X	X	H	X	L	L	Q0 + 1	Read out A0 + 1
n + 4	X	X	X	H	X	L	L	Q0 + 2	Read out A0 + 2
n + 5	A1	H	X	L	L	L	L	Q0 + 3	Read out A0 + 3
n + 6	X	X	X	H	X	L	L	Q0	Read out A0
n + 7	X	X	X	H	X	L	L	Q1	Read out A1
n + 8	A2	H	X	L	L	L	L	Q1 + 1	Read out A1 + 1
n + 9	A3	H	X	L	L	L	L	Q1 + 2	Read out A1 + 2
n + 10	X	X	X	X	X	L	L	Q2	Read out A2

Notes: 1. H means logical High and L means logical Low. X means Don't care. Q is data output.

(3) Write Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	X	L	X	Address & control valid
n + 1	X	X	X	X	X	X	L	X	
n + 2	X	X	X	X	X	X	L	D0	Write to A0

Notes: 1. H means logical High and L means logical Low. X means Don't care. D is data input.

(4) Burst Write Operation

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	X	L	X	Address & control valid
n + 1	X	X	L	H	X	X	L	X	
n + 2	X	X	L	H	X	X	L	D0	Write A0
n + 3	X	X	L	H	X	X	L	D0 + 1	Write A0 + 1
n + 4	X	X	L	H	X	X	L	D0 + 2	Write A0 + 2
n + 5	A1	L	L	L	L	X	L	D0 + 3	Write A0 + 3
n + 6	X	X	L	H	X	X	L	D0	Write A0
n + 7	X	X	L	H	X	X	L	D1	Write A1
n + 8	A2	L	L	L	L	X	L	D1 + 1	Write A1 + 1
n + 9	A3	L	L	L	L	X	L	D1 + 2	Write A1 + 2
n + 10	X	X	L	X	X	X	L	D2	Write A2

Notes: 1. H means logical High and L means logical Low. X means Don't care. D is data input.

(5) Read Operation with Clock Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	X	L	L	X	L	X	Address & control valid
n + 1	X	X	X	X	X	X	H	X	Ignore cycle
n + 2	A1	H	X	L	L	X	L	X	Address & control valid
n + 3	X	X	X	X	X	L	H	Q0	Ignore clock, Q0 is on bus
n + 4	X	X	X	X	X	L	H	Q0	Ignore clock, Q0 is on bus
n + 5	A2	H	X	L	L	L	L	Q0	Read out A0
n + 6	A3	H	X	L	L	L	L	Q1	Read out A1
n + 7	X	X	X	X	X	L	L	Q2	Read out A2

Notes: 1. H means logical High and L means logical Low. X means Don't care. Q is data output.

(6) Write Operation with Clock Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	X	L	X	Address & control valid
n + 1	X	X	X	X	X	X	H	X	Ignore clock
n + 2	A1	L	L	L	L	X	L	X	Address & control valid
n + 3	X	X	X	X	X	X	H	X	Ignore clock
n + 4	X	X	X	X	X	X	H	X	Ignore clock
n + 5	A2	L	L	L	L	X	L	D0	Address & control valid
n + 6	A3	L	L	L	L	X	L	D1	Write A1
n + 7	X	X	X	X	X	X	L	D2	Write A2

Notes: 1. H means logical High and L means logical Low. X means Don't care. D is data input.

(7) Read Operation with Chip Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	H	X	L	L	X	L	X	Address & control valid
n + 1	X	X	X	L	H	X	L	X	Deselect
n + 2	A1	H	X	L	L	L	L	Q0	Read A0
n + 3	X	X	X	L	H	X	L	Z	Deselect
n + 4	X	X	X	L	H	L	L	Q1	Read A1
n + 5	A2	H	X	L	L	X	L	Z	Deselect
n + 6	X	X	X	L	H	X	L	Z	Deselect
n + 7	X	X	X	L	H	L	L	Q2	Read A2

Notes: 1. H means logical High and L means logical Low. X means Don't care. Q is data output. Z means Hi-Z.

(8) Write Operation with Chip Enable

CYCLE	ADDRESS	$\overline{WE}$	$\overline{BW}$	ADV	$\overline{CE}$	$\overline{OE}$	$\overline{CKE}$	I/O	OPERATION
n	A0	L	L	L	L	X	L	X	Address & control valid
n + 1	X	X	X	L	H	X	L	X	Deselect
n + 2	A1	L	L	L	L	X	L	D0	Write A0
n + 3	X	X	X	L	H	X	L	Z	Deselect
n + 4	X	X	X	L	H	X	L	D1	Write A1
n + 5	A2	L	L	L	L	X	L	Z	Deselect
n + 6	X	X	X	L	H	X	L	Z	Deselect
n + 7	X	X	X	L	H	X	L	D2	Write A2

Notes: 1. H means logical High and L means logical Low. X means Don't care. D is data input. Z means Hi-Z.

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	−0.5 to 3.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	−0.5 to V_{DD} + 0.5 (≤ 3.6 V max)	V
V_{IN}	Input Terminal Voltage	−0.5* to 3.6	V
$V_{I/O}$	Input/Output Terminal Voltage	−0.5* to V_{DDQ} + 0.5** (≤ 3.6 V max)	V
P_D	Power Dissipation	1.5	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−65 to150	°C
T_{opr}	Operating Temperature	−10 to 85	°C

*: −1.0 V with a pulse width of 20% of t_{KC} min (3 ns max)

**: V_{DDQ} + 1.0 V with a pulse width of 20% of t_{KC} min (3 ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{DD}	Power Supply Voltage	2.375	2.5	2.625	V
V_{DDQ}	Output Buffer Power Supply Voltage	2.375	2.5	2.625	V
V_{IH}	Input High Voltage	1.7	—	V_{DD} + 0.3**	V
V_{IH1}	Input High Voltage for MODE pin	V_{DD} − 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.7	V
V_{IL1}	Input Low Voltage for MODE and NU pins	−0.3	0.0	0.3	V

*: −0.7 V with a pulse width of 20% of t_{KC} min (3 ns max)

**: V_{DD} + 0.7 V with a pulse width of 20% of t_{KC} min (3 ns max)

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.7V.
You must not apply a voltage of more than 0.7V to the NU.

DC CHARACTERISTICS ($Ta = 0°$ to $70°C$, $V_{DD} = V_{DDQ} = 2.5\ V \pm 5\ \%$)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 to V_{DD}		−1	—	1	μA
I_{NU}	Input Current (NU pin)	V_{IN} = 0 to 0.3 V		−1	—	1	μA
I_{LO}	Output Leakage Current	Device Deselected or Output Deselected, V_{OUT} = 0 to V_{DDQ}		−1	—	1	μA
V_{OH}	Output High Voltage	I_{OH} = −1 mA		2.0	—	—	V
		I_{OH} = −100 μA		V_{DDQ} − 0.2	—	—	
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		—	—	0.4	V
		I_{OL} = 100 μA		—	—	0.2	
I_{DDO1}	Operating Current	Device Selected I_{OUT} = 0 mA, All Inputs = V_{DD} − 0.2 V/0.2 V Clock ≥ t_{KC} Minimum	22(225 MHz)	—	—	TBD	mA
			20(200 MHz)	—	—	TBD	
			16(167 MHz)	—	—	TBD	
			15(150 MHz)	—	—	TBD	
I_{DDO2}	Operating Current (idle)	Device Deselected I_{OUT} = 0 mA, All Inputs = V_{DD} − 0.2 V/0.2 V Clock ≥ t_{KC} Minimum	22(225 MHz)	—	—	TBD	mA
			20(200 MHz)	—	—	TBD	
			16(167 MHz)	—	—	TBD	
			15(150 MHz)	—	—	TBD	
I_{DDS1}	Standby Current (TTL level)	Clock = V_{SS} All Inputs = V_{IH} or V_{IL}		—	—	100	mA
I_{DDS2}	Standby Current (MOS level)	Clock = V_{SS} All Inputs = V_{DD} − 0.2 V or 0.2 V		—	—	10	mA
I_{DDS3}	Standby Current (Snooze Mode)	ZZ ≥ V_{DD} − 0.2 V All Inputs = V_{DD} − 0.2 V or 0.2 V Clock ≥ t_{KC} Minimum		—	—	10	mA
I_{DDS4}	Standby Current ($\overline{CKE}$ Mode)	$\overline{CKE}$ ≥ V_{IH} All Inputs = V_{DD} − 0.2 V or 0.2 V Clock ≥ t_{KC} Minimum		—	—	10	mA

Note: Operating Current (I_{DDO1}) is specified with 50% Read cycles and 50% Write cycles.

CAPACITANCE (Ta = 25°C, f = 1 .0 MHz)

SYMBOL	PARAMETER	TEST CONDITIONS	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	7	pF
C_{NU}	Input Capacitance of NU	V_{NU} = GND	10	pF
C_{MODE}	Input Capacitance of MODE	V_{MODE} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = V_{DDQ} = 2.5 V ± 5 %)

SYMBOL	PARAMETER	TC55WDM536AFFN								UNIT
		22 (225MHz)		20 (200MHz)		16 (167MHz)		15 (150MHz)		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{KC}	CLK Cycle Time	4.4	—	5.0	—	6.0	—	6.6	—	ns
t_{KH}	CLK High Pulse Width	2.0	—	2.0	—	2.2	—	2.5	—	
t_{KL}	CLK Low Pulse Width	2.0	—	2.0	—	2.2	—	2.5	—	
t_{KQV}	CLK High to Output Valid	—	2.8	—	3.2	—	3.5	—	3.8	
t_{KQX}	CLK High to Output Invalid	1.5	—	1.5	—	1.5	—	1.5	—	
t_{KQLZ}	CLK High to Output Low-Z	1.5	—	1.5	—	1.5	—	1.5	—	
t_{KQHZ}	CLK High to Output High-Z	1.5	2.8	1.5	3.0	1.5	3.0	1.5	3.0	
t_{GQV}	$\overline{OE}$ Low to Output Valid	—	2.8	—	3.2	—	3.5	—	3.8	
t_{GQLZ}	$\overline{OE}$ Low to Output Low-Z	1.5	—	1.5	—	1.5	—	1.5	—	
t_{GQHZ}	$\overline{OE}$ High to Output High-Z	0	2.8	0	3.0	0	3.0	0	3.0	
t_{AS}	Address Setup Time from CLK	1.4	—	1.4	—	1.5	—	1.5	—	
t_{DS}	Data Setup Time from CLK	1.4	—	1.5	—	1.5	—	1.5	—	
t_{WS}	$\overline{WE}$ Setup Time from CLK	1.4	—	1.4	—	1.5	—	1.5	—	
t_{CES}	CE Setup Time from CLK	1.4	—	1.4	—	1.5	—	1.5	—	
t_{ADVS}	ADV Setup Time from CLK	1.4	—	1.4	—	1.5	—	1.5	—	
t_{BWS}	$\overline{BW}$ Setup Time from CLK	1.4	—	1.4	—	1.5	—	1.5	—	
t_{CKES}	$\overline{CKE}$ Setup Time from CLK	1.4	—	1.4	—	1.5	—	1.5	—	
t_{AH}	Address Hold Time from CLK	0.4	—	0.4	—	0.5	—	0.5	—	
t_{DH}	Data Hold Time from CLK	0.4	—	0.4	—	0.5	—	0.5	—	
t_{WH}	$\overline{WE}$ Hold Time from CLK	0.4	—	0.4	—	0.5	—	0.5	—	
t_{CEH}	CE Hold Time from CLK	0.4	—	0.4	—	0.5	—	0.5	—	
t_{ADVH}	ADV Hold Time from CLK	0.4	—	0.4	—	0.5	—	0.5	—	
t_{BWH}	$\overline{BW}$ Hold Time from CLK	0.4	—	0.4	—	0.5	—	0.5	—	
t_{CKEH}	$\overline{CKE}$ Hold Time from CLK	0.4	—	0.4	—	0.5	—	0.5	—	
t_{ZS}	ZZ Standby Time	5	—	5	—	5	—	5	—	
t_{ZR}	ZZ Recovery Time	5	—	5	—	5	—	5	—	
t_{ZHZ}	ZZ to Output in High-Z	—	2	—	2	—	2	—	2	cycle

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Input Pulse Level	2.5 V/ 0.0 V
Input Pulse Rise and Fall Time	1 V/ns (20%/80%)
Input Timing Measurement Reference Level	1.25 V
Output Timing Measurement Reference Level	1.25 V
Output Load	As shown in Fig.1 and Fig.2

Fig.1:AC test load

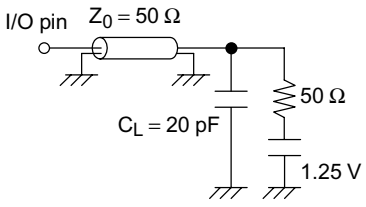
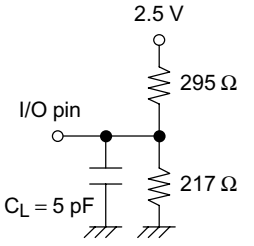


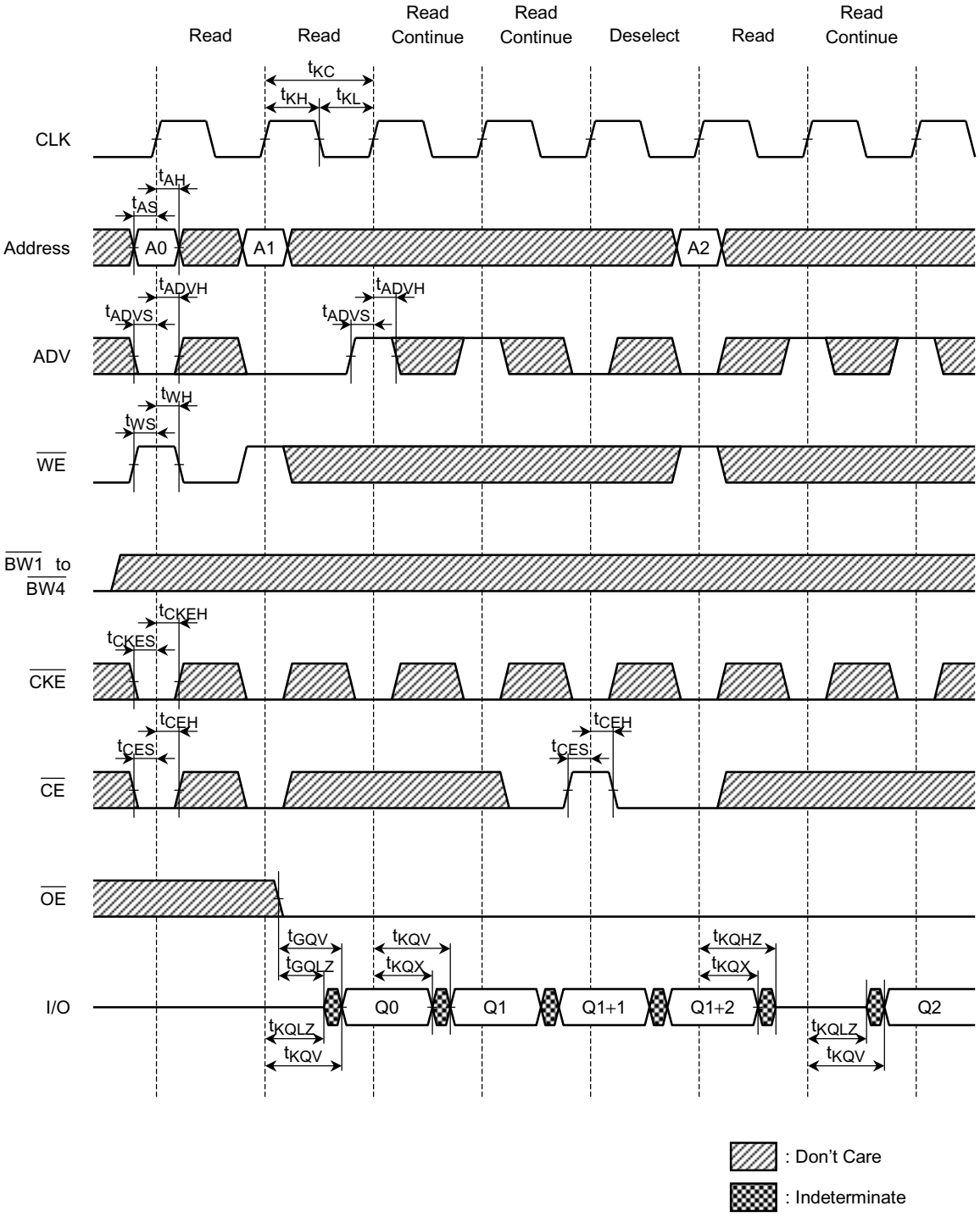
Fig.2:AC test load



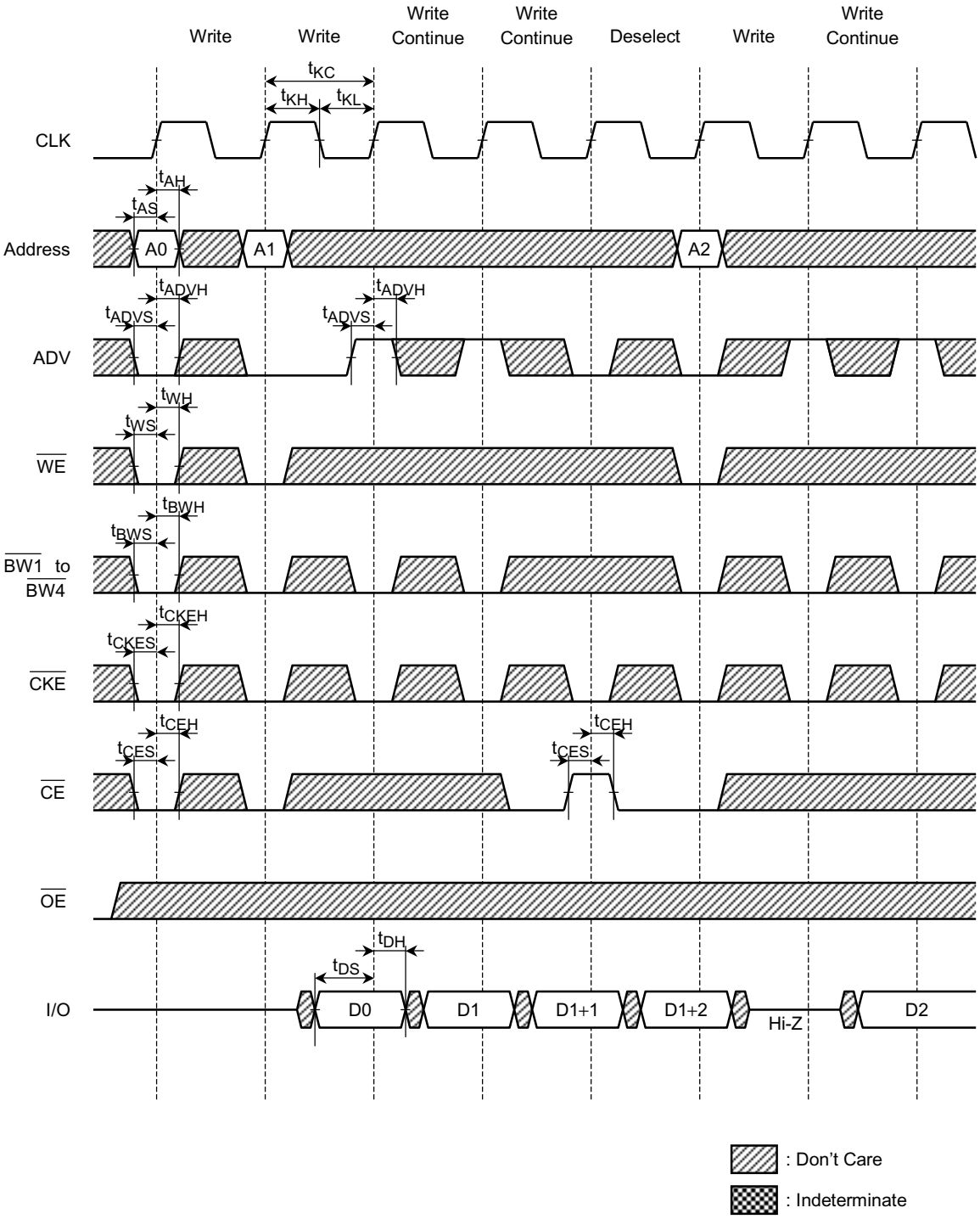
(for Enable/Disable spec)

TIMING DIAGRAMS

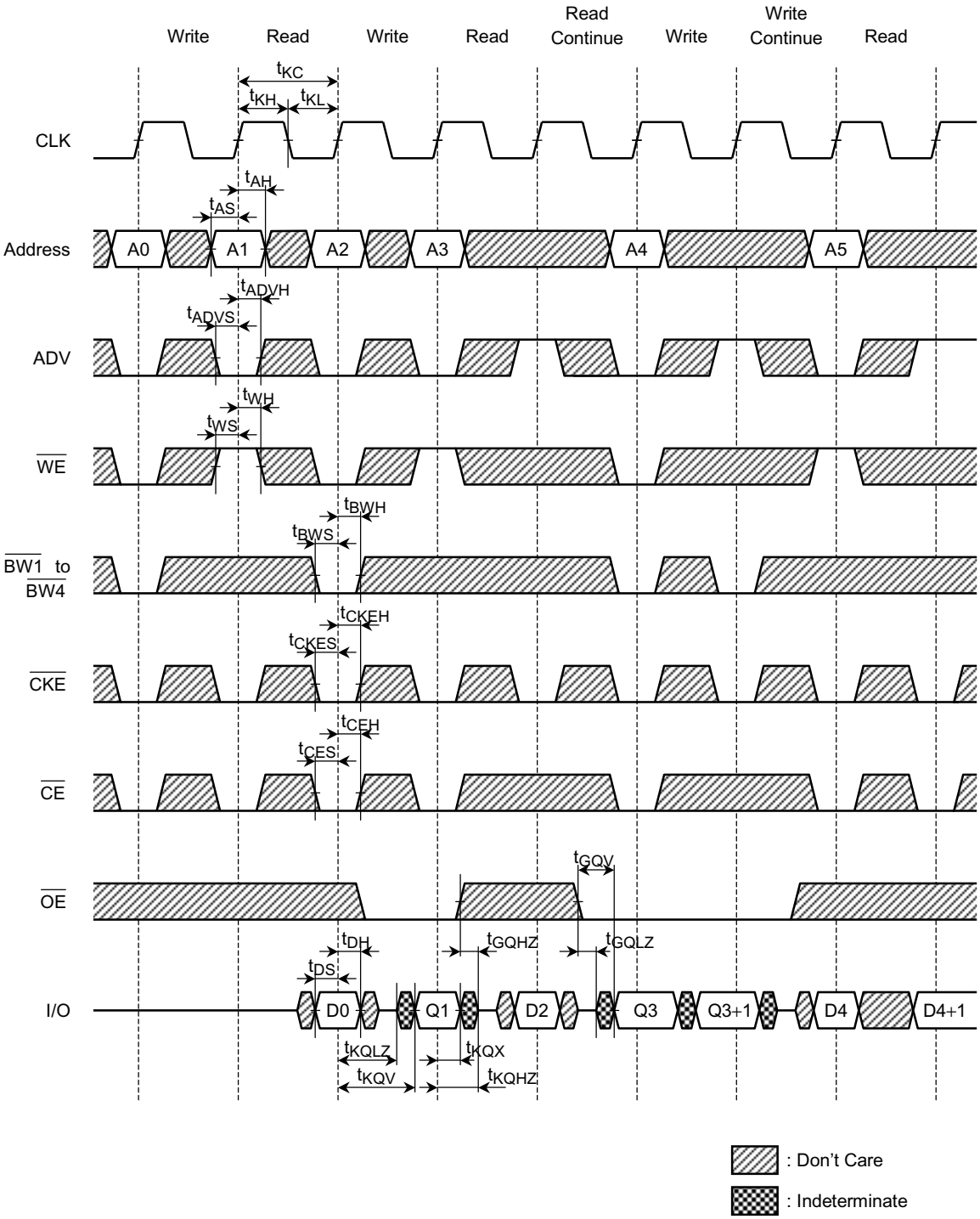
(1) READ CYCLE



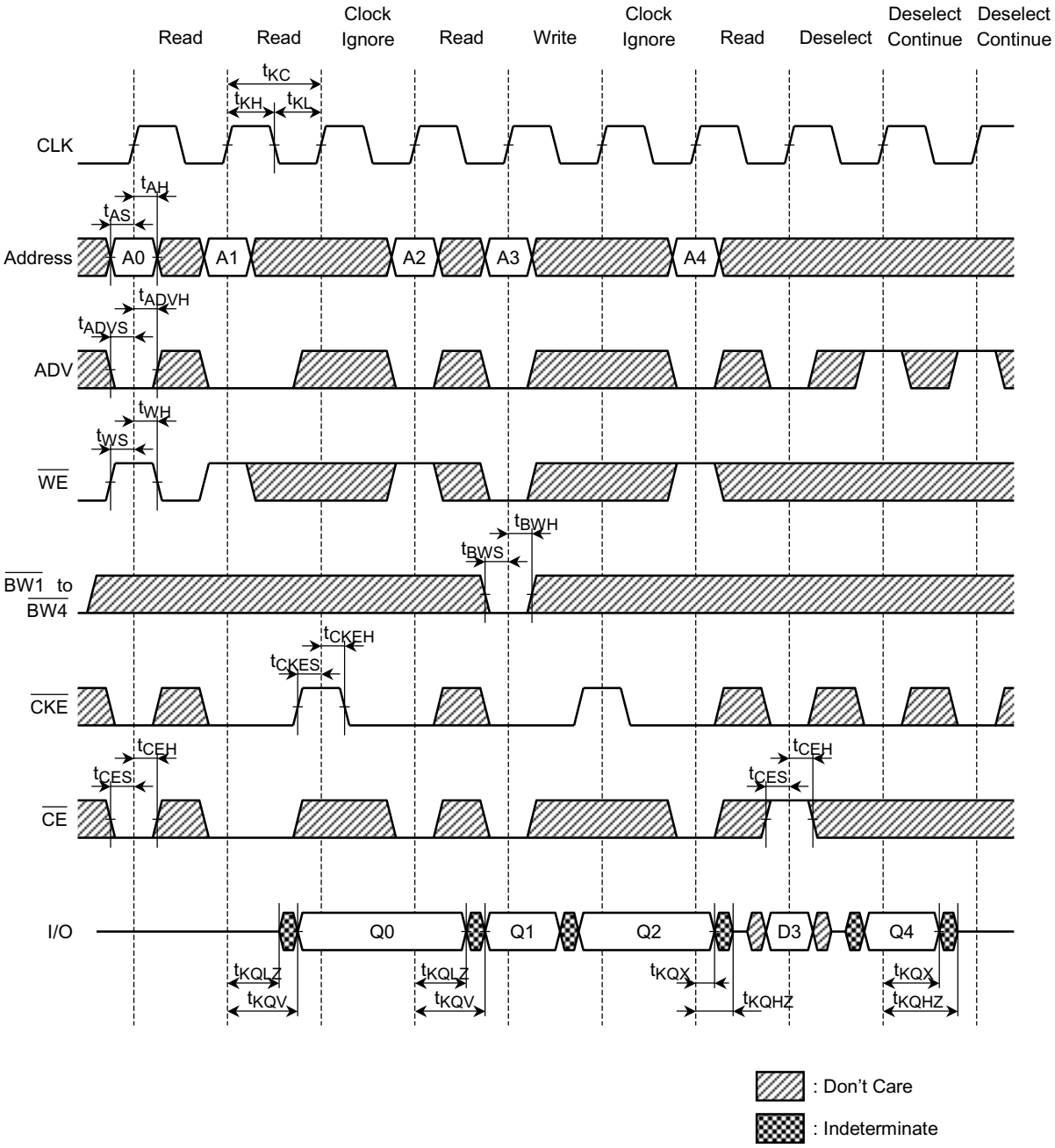
(2) WRITE CYCLE



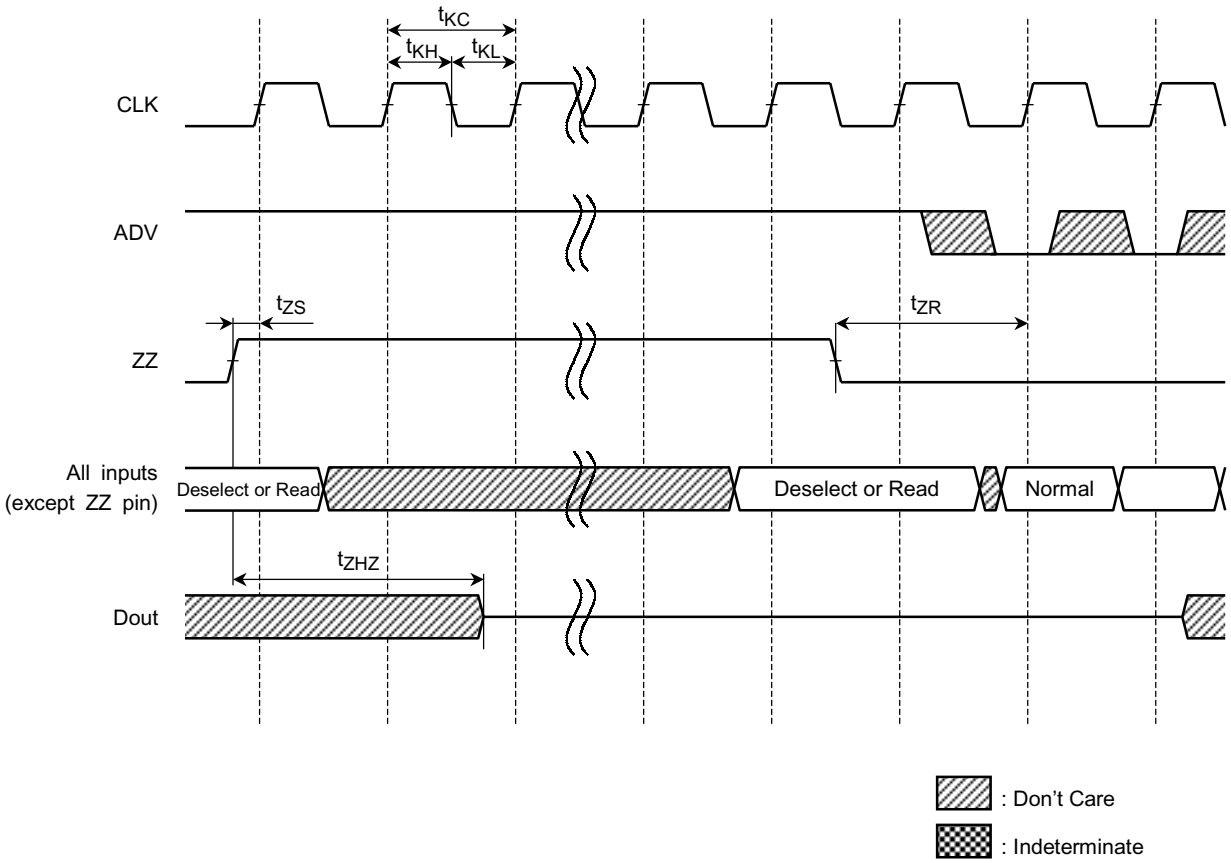
(3) WRITE/READ CYCLE



(4) CLOCK IGNORE/DESELECT CYCLE



(5) SNOOZE CYCLE

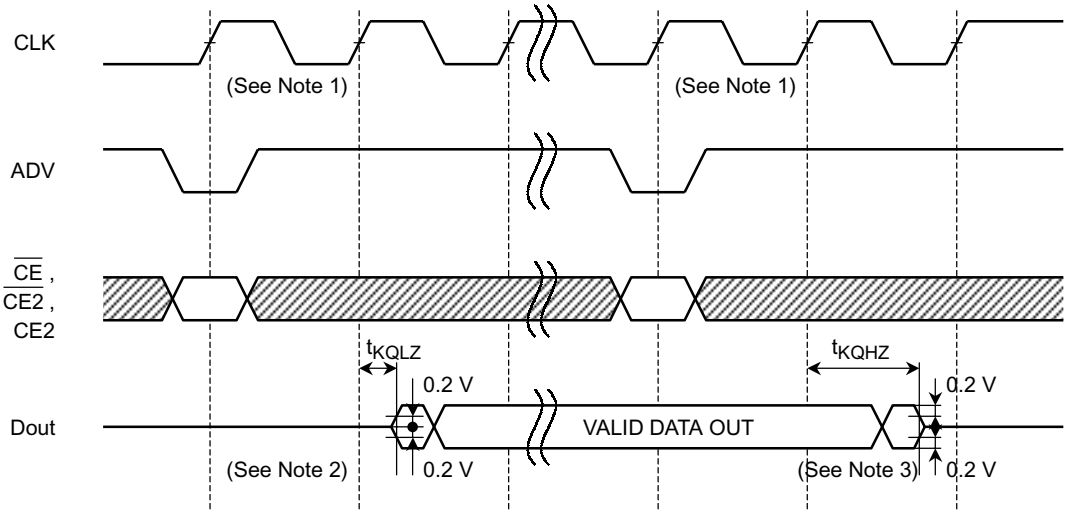


Notes: 1. The 2 cycles immediately prior to a Snooze brought about by the ZZ pin must be Read or Deselect cycles.
2. Memory data is retained during Snooze cycles.

Notes: 1. Do not apply opposite data polarity to the I/O pins when they are in the output state.

2. Output enable and output disable times are specified as follows using the output load shown in Fig.1.

(A) t_{KQLZ} , t_{KQHZ}

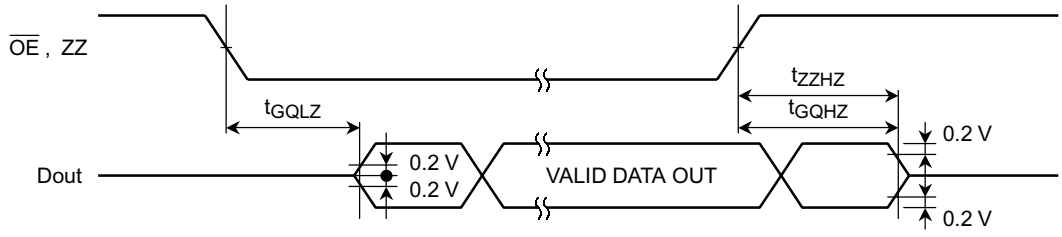


Notes: 1. Input states are defined in the Synchronous Input Truth Table.

2. If the device was previously deselected, when the device is selected, the output remains in a high impedance state in the present clock cycle regardless of $\overline{OE}$ because of the output enable delay register. Valid data appears in the second clock cycle when $\overline{OE}$ is low.

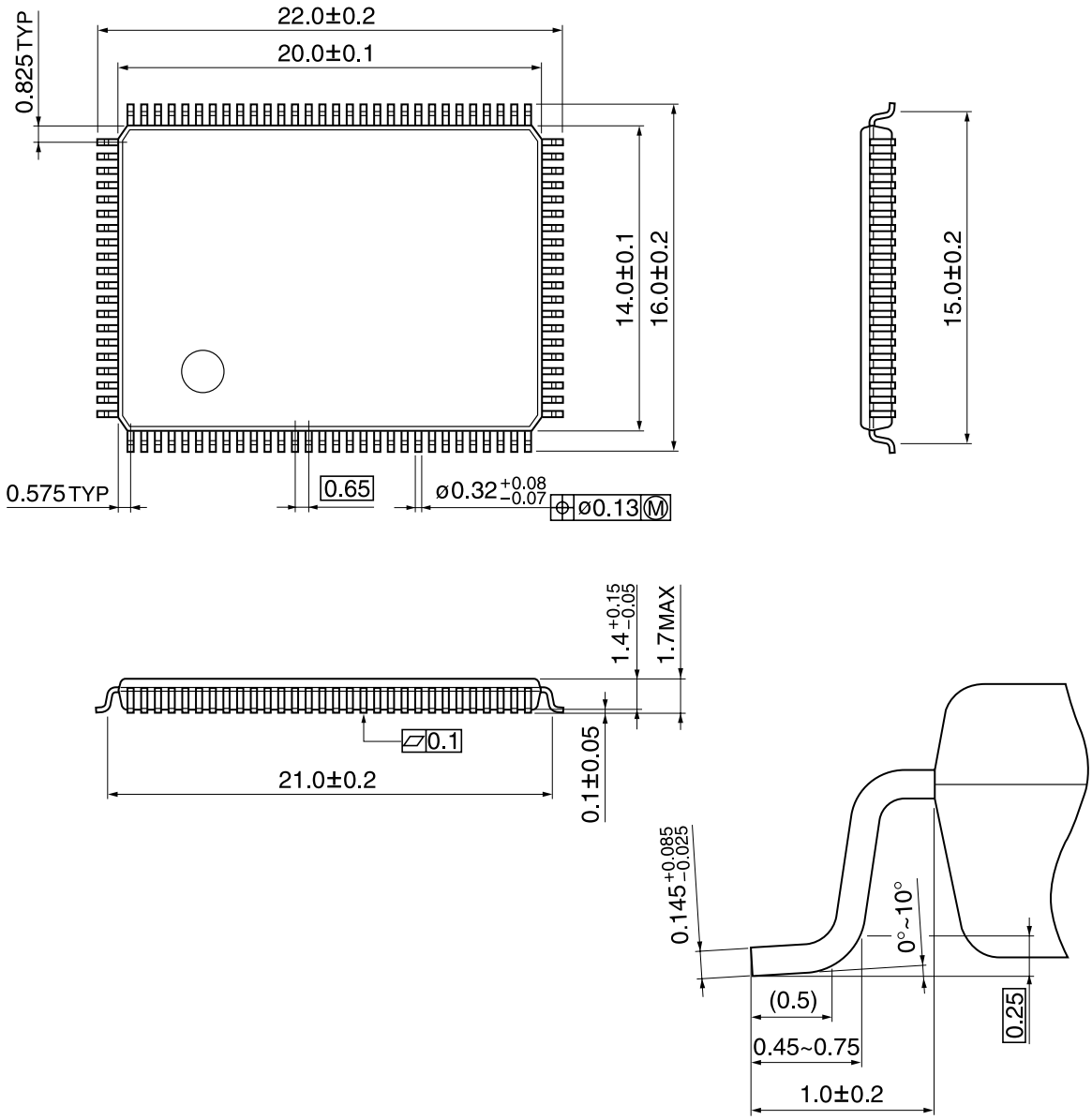
3. When the device is deselected, the output goes into a high impedance state in the next clock cycle regardless of $\overline{OE}$.

(B) t_{GQLZ} , t_{GQHZ} , t_{ZZHZ}



PACKAGE DIMENSIONS

LQFP100-P-1420-0.65B Unit: mm



Weight: g (typ)

Data sheet Revision History

Release Date	History
2002-09-30	1 . New Datasheet Release
2002-12-04	1. AC parameter change t_{KQV} (MAX) from 3.8 ns to 3.5 ns at 16 (167 MHz) 2. DC test condition change at I_{DDO1}
2003-01-08	1. AC parameter change t_{GQHZ} (MIN) from 1.5 ns to 0 ns 2. AC parameter change at snooze mode Add parameter : t_{ZS}, t_{ZR}, t_{ZHZ} Delete parameter : t_{ZZ}, t_{ZZR}, t_{ZZHZ}, t_{ZZLZ}

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