Honeywell
Digital Technologies

Radiation Hardened Static RAM Family

HC6167R (16K x 1), HC6116R (2K x 8) *Preliminary*

Family Features

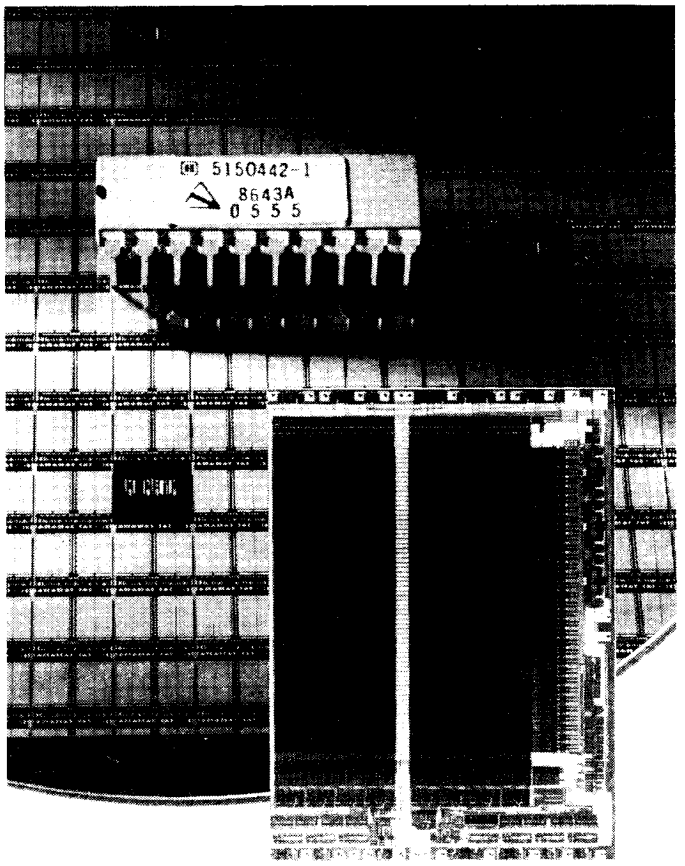
- TTL and CMOS Compatible
- Strategic Radiation Hardened
- 80ns Access (HC6116R); 105ns Access (HC6167R)
- RICMOS™ 1.2µm Minimum Feature Size Process
- Honeywell Class B and S Screening
- Full Military Temperature Range (-55°C to +125°C)
- Latchup Immune
- Low Operating/Standby Current
- Single +5V Power Supply
- Equal Address and Cycle Times

Family Description

The Honeywell RICMOS™ memory family consists of the HC6167R (16K x 1) and the HC6116R (2K x 8). Both products are capable of operating asynchronously.

The HC6167R features 105ns typical access times with a page mode capability offering 35ns typical access time. It is available in a 20-pin DIP, 24-pin flatpack and 20-pin leadless chip carrier.

The HC6116R achieves 80ns typical access times and requires approximately 5mA/MHz of operating current. It is available in a 24-pin flatpack and a 24-pin DIP.



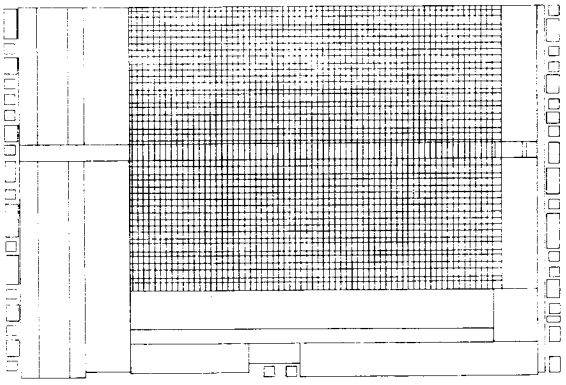
Radiation Hardness Levels

Radiation Environment	Hardness Level
Total Dose	> 0.5E6 Rads (Si)
Neutron	> 3E14 Neutrons/cm^2
Single Event Upset	< 1E-10 Errors/Bit/Day
Dose Rate • Short Pulse (Upset) • Long Pulse (Upset) • Short Pulse (Survival)	 > 1E9 Rads (Si)/Second > 5E8 Rads (Si)/Second > 1E12 Rads (Si)/Second
Latchup	None

Product Features

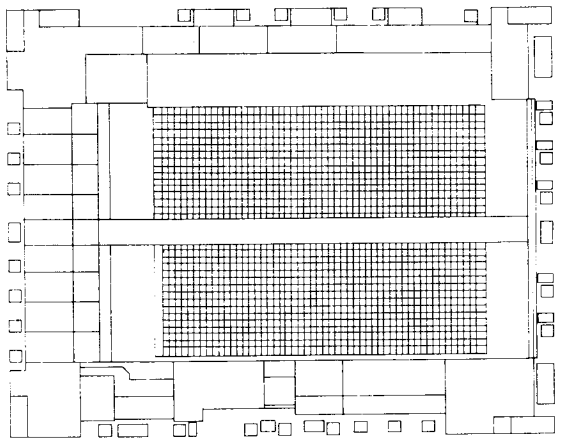
Features	HC6167R (16K x 1)	HC6116R (2K x 8)
Typical Power Dissipation	0.028W/MHz	0.035W/MHz
Operating Temperature (Case)	-55 to +125°C	-55 to +125°C
Process Technology	RICMOS™	RICMOS™
Minimum Geometry	1.5μm	1.2μm
Supply Voltage	5V +/- 0.5V	5V +/- 0.5V

Array Architecture



HC6167R (16K x 1) Array Organization

- 25 Input/Output Pads–multiple power and ground capability offers enhanced radiation hardness.
- Input Buffer Enable/Disable–reduces standby current.
- Page Mode Addressing–(addressing bits from different columns but from the same row) offers 35ns access time.



HC6116R (2K x 8) Array Organization

- 8 Bidirectional Data Input/Output Pads.
- Fully Static Operation–(no refreshing required).
- Fully Asynchronous Operation.

Radiation Hardened Characteristics

Total Ionizing Radiation Dose

The family meets all stated functional and electrical specifications after a total ionizing radiation dose of 0.5E6 Rads (Si) applied under specified operating conditions.

Transient Pulse Ionizing Radiation

The family is capable of writing, reading, and retaining stored data during and after a 20ns transient ionizing radiation pulse of over 1E9 Rads (Si)/second, applied under specified operating conditions. Additionally, the family will not be rendered permanently incapable of meeting any functional or electrical specification by a 20ns transient ionizing radiation pulse of over 1E12 Rads (Si)/second applied under recommended operating conditions. Note that the current conducted during a transient ionizing radiation pulse by the inputs, outputs and power supply may significantly exceed the normal operating values. The system design must accommodate these increases.

Neutron Radiation

The family meets all stated functional and electrical specifications after a total neutron fluence of over 3E14 neutrons/cm^2 , applied under recommended operating conditions, assuming an equivalent neutron energy of 1MeV.

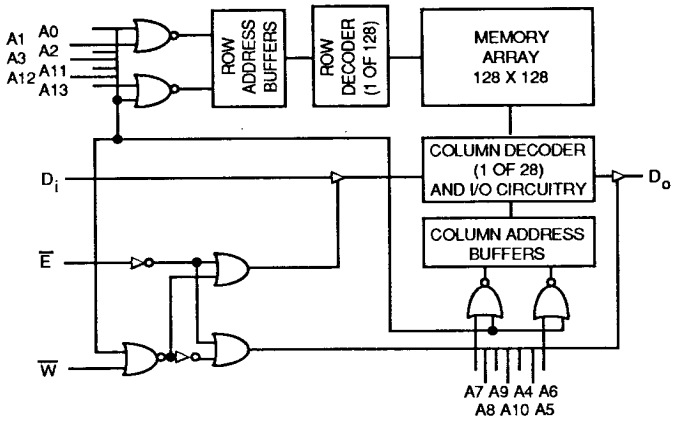
Soft Error Rate

The family incurs no more than 1 x 10^{-10} errors/bit/day when operated in an Adams' 10% worst case cosmic ray environment under recommended operating conditions. This environment is defined in Figure 1, curve C of the paper: J. H. Adams, Jr., "The Variability of Single Event Upset Rates in the Natural Environment" (IEEE Trans. Nucl. Sci. NS-30, 4475, 1983).

Latchup

The HC6167R will not latchup when exposed to any of the above radiation conditions applied under the specified operating conditions.

HC6167R Functional Diagram



HC6167R DC Characteristics

Parameter	Description	CMOS Levels		TTL Levels		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CCQSC}	CMOS-Level Static Quiescent Current		250		250	µA	V_{CC}=5.5V
I_{CCQST}	TTL-Level Static Quiescent Current		250		250	µA	V_{CC}=5.5V
I_{CCOP}	Operating Supply Current		5.5		5.5	mA	f=1MHz, V_{CC}=5.5V
I_{IN}	Input Leakage Current		+/-10		+/-10	µA	f=1MHz, V_{CC}=5.5V
I_{OZL}	Low-Level Output Leakage Current		-10		-10	µA	V_{IN} =5.5V, V_O =0V
I_{OZH}	High-Level Output Leakage Current		10		10	µA	V_{IN} =5.5V, V_O =5.5V
V_{DR}	Data Retention Voltage	2.5		2.5		V	V_{CC}=2.5V
I_{DR}	Data Retention Current		100		100	µA	V_{CC}=2.5V
V_{IL}	Low-Level Input Voltage				0.8	V	V_{CC}=4.5V
V_{IH}	High-Level Input Voltage			2.2		V	V_{CC}=4.5V
V_{OL}	Low-Level Output Voltage			0.4		V	V_{CC} =4.5V, I_{OL}=8mA
V_{OH}	High-Level Output Voltage				2.4	V	V_{CC} =4.5V, I_{OH}=-0.6mA
C_I	Input Capacitance		6.5		6.5	pF	Note (1)
C_O	Output Capacitance		8.0		8.0	pF	Note (1)

(1) Capacitances are package dependent. Data given is for a 28-pin flatpack.

HC6167R Read Cycle Characteristics

Parameter	Description	CMOS Levels		TTL Levels		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TAVAV1	Read Cycle Time	160		170		ns	
TAVQV	Address Valid to Data Valid Time		150		130	ns	
TSLQV	Select Low to Data Valid Time		160		170	ns	
TSHQZ	Select High to Data High-Z Time		25		25	ns	
TAVSL	Address Valid to Select Low Time	0		0		ns	

HC6167R Write Cycle Characteristics

Parameter	Description	CMOS Levels		TTL Levels		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TAVAV2	Write Cycle Time	155		165		ns	
TAVWL	Address Valid to Write Low Time (2)	10		10		ns	
TAVWH	Address Valid to Write High Time		140		150	ns	
TSLWL	Select Low to Write Low Time	0		0		ns	
TWLWH	Write Low to Write High Time		130		140	ns	
TWHSH	Write High to Select High Time	0		0		ns	
TWHAX	Write High to Address Don't Care Time (2)	15		15		ns	
TWLQZ	Write Low to Data High-Z Time		20		20	ns	
TWHDX	Write High to Data Don't Care Time	0		0		ns	
TWHWL	Write High to Write Low Time	25		25		ns	
TDVWL	Data Valid to Write Low Time	0		0		ns	

(2) Signal may be coincident with address edges, but total set-up and hold times (TAVWL+TWHAX) must equal TWHWL.
(3) All parameters are valid through 500kRad (Si) total dose irradiation.
(4) Test Conditions:
1) Rise and fall times<5ns; 2) CMOS input levels: V_{IL}=0.2V, V_{IH}=V_{CC} -0.4V; 3) TTL input levels: V_{IL}=0.4V, V_{IH}=2.4V; 4) V_{CC}=4.5V, T=-55 to +125°C; 5) Capacitive output loading is 50pF.

HC6167R Absolute Maximum Ratings (1)

Parameter	Description	Ratings		Units
		Min.	Max.	
V_{CC}	Positive Supply Voltage	-0.5	6.5 (2)	V
V_{PIN}	Voltage on Any Pin	-0.5 (3)	V_{DD}+0.5	V
T_{STORE}	Storage Temperature (Zero Bias)	-65	150	°C
P	Power Dissipation		0.5	W
I_{OUT}	DC or Average Output Current		25	mA

(1) Stresses in excess of those listed above may result in immediate permanent damage to the HC6167R. This is a stress rating only and operation at these or any other conditions outside the limits indicated in the operating sections of this specification are not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) During power initialization, V_{CC} may be as high as 7.0V momemtarily. The maximum allowable duration and frequency of this conditon remains TBD. V_{CC} may not exceed 7.0V at any time.
(3) The minimum pin voltage may be as low as -1.5V momentarily. The maximum allowable duration, frequency energy dissipation and current conduction of this condition remains TBD.

HC6167R Recommended Operating Conditions

Parameter	Description	Limits			Units
		Min.	Typ.	Max.	
V_{SS}	Reference Supply Voltage	0		0	V
V_{DD}	Positive Supply Voltage	4.5		5.5	V
V_{IH}	Input High Level	2.2		V_{DD}+0.3	V
V_{IL}	Input Low Level	V_{SS} -0.3		0.8	V
C_L	Output Load	Note (3)		Note (4)	pF
T_C	External Package Temperature	-55		125	°C

(1) The HC6167R meets all specifications over these operating conditions.
(2) Specifications contained in this document assume the use of all power and ground pads on chip.
(3) Output load can be reduced arbitrarily. However, for very light loads the output transition time can become very short (less than 1ns) and must be accommodated by the application design.
(4) Output load can be increased with a corresponding increase in read access time and power dissipation.

HC6116R DC Characteristics

Parameter	Description	CMOS Levels		TTL Levels		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CCQSC}	CMOS-Level Static Quiescent Current		.250		7	mA	V_{CC}=5.5V
I_{CCQST}	TTL-Level Static Quiescent Current		.250		7	mA	V_{CC}=5.5V
I_{CCOP}	Operating Supply Current		7		7	mA	f=1MHz, V_{CC}=5.5V
I_{IN}	Input Leakage Current		+/-5		+/-5	µA	V_{CC}=5.5V
I_{OZL}	Low-Level Output Leakage Current		-10		-10	µA	V_{IN}=5.5V,V_O=0V
I_{OZH}	High-Level Output Leakage Current		10		+10	µA	V_{IN}=5.5V,V_O=0V
V_{DR}	Data Retention Voltage	2.5		2.5		V	V_{CC}=2.5V
I_{DR}	Data Retention Current		0.05		TBD	mA	V_{CC}=2.5V
V_{IL}	Low-Level Input Voltage		V_{SS}+0.5		0.8	V	V_{CC}=4.5V
V_{IH}	High-Level Input Voltage	V_{DD}-0.5		2.0		V	V_{CC}=4.5V
V_{OL}	Low-Level Output Voltage				0.4	V	V_{CC}=4.5V, I_{OL}=8mA
V_{OH}	High-Level Output Voltage			2.5		V	V_{CC}=4.5V, I_{OH}=-0.4mA
C_I	Input Capacitance		11		11	pF	Note (1)
C_O	Input/Output Capacitance		12		12	pF	Note (1)

(1) Capacitances are package dependent. Data given is for a 24-pin flatpack.

HC6116R Read Cycle Characteristics

Parameter	Description	CMOS Levels		TTL Levels		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TAVAV1	Read Cycle Time	120		130		ns	
TAVQV	Address Valid To Data Valid Time		120		130	ns	
TSLQV	Select Low to Data Valid Time		100		110	ns	
TSHQZ	Select High to Data High-Z Time		30		30	ns	
TAVSL	Address Valid to Select Low Time	0		0		ns	
TSLQX	Select Low to Output Don't Care Time	2		2			
TOLQX	Output Enable Low to Output Don't Care Time	2		2			
TOHQZ	Output Enable High to Output High-Z Time		30		30		
TOLQV	Output Enable Low to Output Valid Time		30		30		
TAVQX	Output Hold After Address Change	2		2			

HC6116R Write Cycle Characteristics

Parameter	Description	CMOS Levels		TTL Levels		Units	Test Conditions
		Min.	Max.	Min.	Max.		
TAVAV2	Write Cycle Time	100		110		ns	
TAVWL	Address Valid to Write Low Time (2)	0		0		ns	
TAVWH	Address Valid to Write High Time		100		110	ns	
TSLWL	Select Low to Write Low Time	0		0		ns	
TWLWH	Write Low to Write High Time		80		80	ns	
TWHSH	Write High to Select High Time	0		0		ns	
TWHAX	Write High to Address Don't Care Time (2)	0		0		ns	
TWLQZ	Write Low to Data High-Z Time		30		30	ns	
TWHDX	Write High to Data Don't Care Time	0		0		ns	
TWHWL	Write High to Write Low Time	20		20		ns	
TDVWL	Data Valid to Write Low Time	0		0		ns	
TSLWH	Select Low to Write High Time		100		110	ns	
TDVWH	Data Valid to Write High Time	80		80		ns	
TWHQX	Write High to Output Don't Care Time	2		2		ns	

(2) Signal may be coincident with address edges, but total set-up and hold times (TAVWL+TWHAX) must equal TWHWL.
(3) All Parameters are valid thorugh 1MRad (Si) total dose irradiation.
(4) Test Conditions: (1) Rise and fall times<5ns; 2) CMOS input levels: V_{IL}=0.2V, V_{IH}=V_{CC} -0.4V; 3) TTL input levels: V_{IL}=0.4V, V_{IH}=2.4V; 4) V_{CC} 4.5V, T=-55 to +125°C; 5) Capacitive output loading is 50pF.
(5) Timing parameters represent a non-SEU-immune part.

HC6116R Absolute Maximum Ratings (1)

Parameter	Description	Ratings		Units
		Min.	Max.	
V_{CC}	Positive Supply Voltage	-0.5	6.5 (2)	V
V_{PIN}	Voltage on Any Pin	-0.5 (3)	V_{DD}+0.5	V
T_{STORE}	Storage Temperature (Zero Bias)	-65	150	°C
P	Power Dissipation		0.5	W
I_{OUT}	DC or Average Output Current		25	mA

(1) Stresses in excess of those listed above may result in immediate permanent damage to the HC6116R. This is a stress rating only and operation at these or any other conditions outside the limits indicated in the operating sections of this specification are not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) During power initialization, V_{CC} may be as high as 7.0V momentarily. The maximum allowable duration and frequency of this condition remains TBD. V_{CC} may not exceed 7.0V at any time.
(3) The minimum pin voltage may be as low as -1.5V momentarily. The maximum allowable duration, frequency, energy dissipation and current conduction of this condition remains TBD.

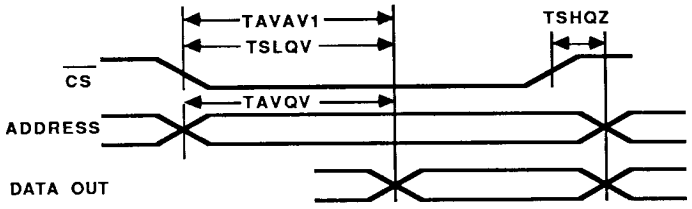
HC6116R Recommended Operating Conditions

Parameter	Description	Limits			Units
		Min.	Typ.	Max.	
V_{SS}	Reference Supply Voltage	0		0	V
V_{DD}	Positive Supply Voltage	4.5		5.5	V
V_{IH}	Input High Level	2.0		V_{DD}+0.3	V
V_{IL}	Input Low Level	V_{SS}-0.3		0.8	V
C_L	Output Load	Note (3)		Note (4)	pF
T_C	External Package Temperature	-55		125	°C

(1) The HC6116R meets all specifications over these operating conditions.
(2) Specifications contained in this document assume the use of all power and ground pads on chip.
(3) Output load can be reduced arbitrarily. However, for very light loads the output transition time can become very short (less than 1ns) and must be accommodated by the application design.
(4) Output load an be increased with a corresponding increase in read access time and power dissipation.

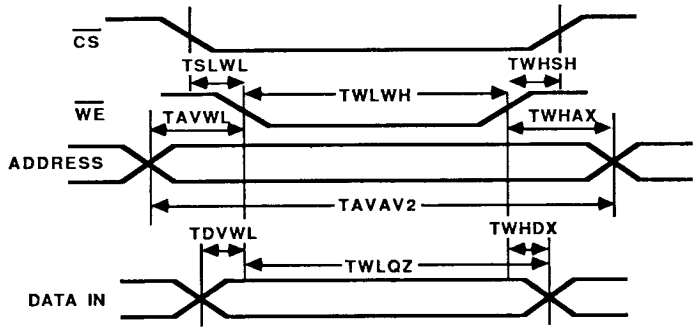
Read Cycle

During read cycles, the address must be stable at the same time that, or before, the chip select goes low. In other words, TAVSL has a minimum value of 0. The data out will then be valid TSLQV time units after the chip select goes low. The data out will move to a high-Z state, at most, TSHQZ time units after the chip select goes high. The address must remain stable until the data out pin goes to a high-Z state.



Write Cycle

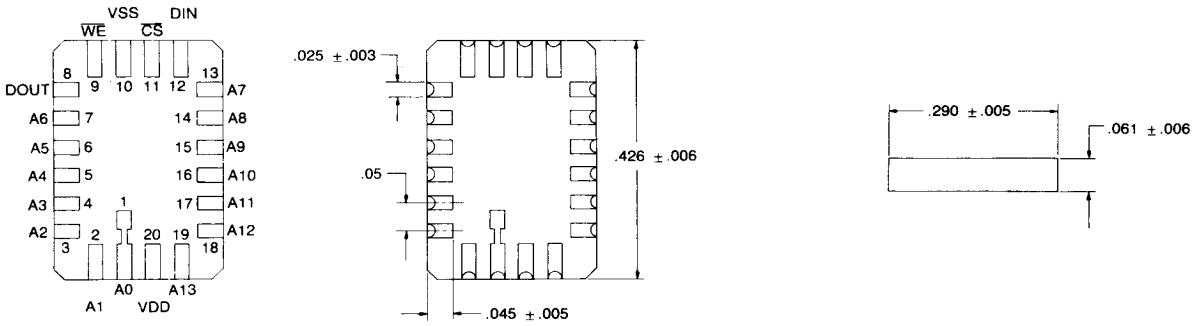
To write data in to the HC6167R and the HC6116R, the chip select must go low before the write enable goes low by at least TSLWL time units. The address must be stable at least TAVWL time units before the write enable goes low, and the data to be written must be stable at least TDVWL time units before the write enable goes low. The write pulse width must be at least TWLWH time units in duration, and the chip select can go high no fewer than TWHSH time units after the write enable goes high. The data being written must remain valid TWHDX time units after the write enable goes high, and the address must be stable for TWHAX time units after the write enable goes high. TDVWH equals TDVWL plus TWLWH. TWHWL equals TWHAX plus TAVWL.



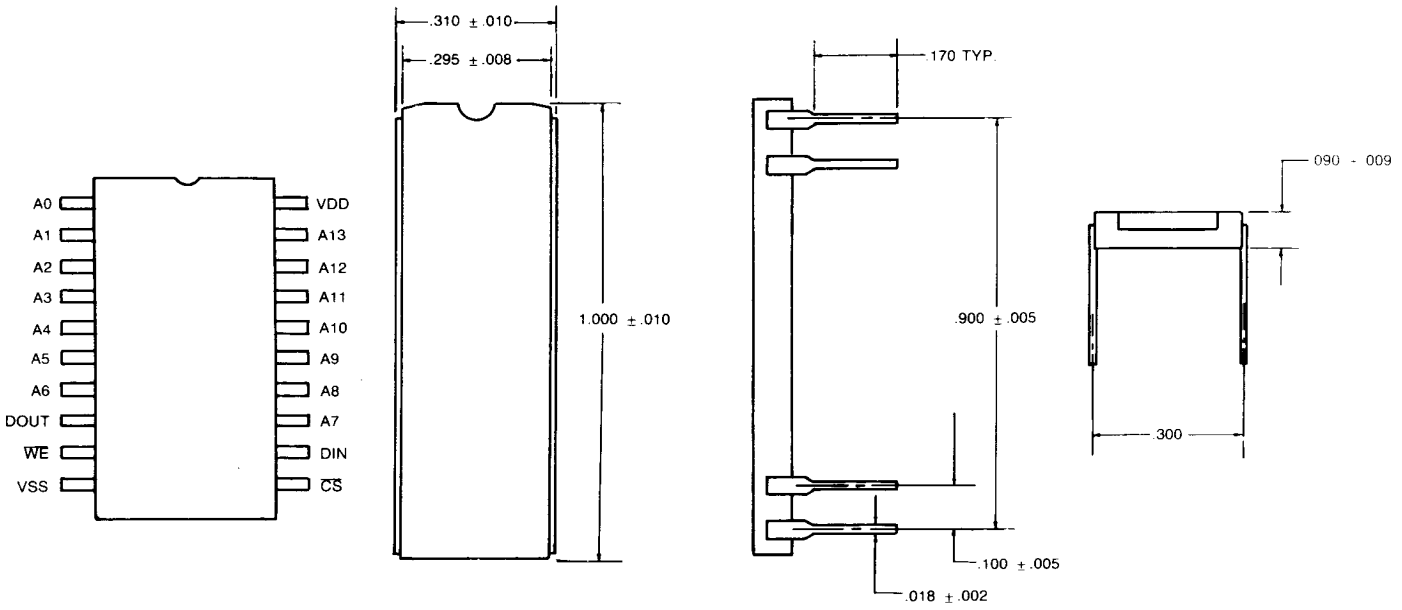
High-Performance Packaging Options

Package \ Product	HC6167R (16K x 1)	HC6116R (2K x 8)
20-Pin DIP	X	
24-Pin Flatpack	X	X
20-Pin Leadless Chip Carrier	X	
24-Pin DIP		X

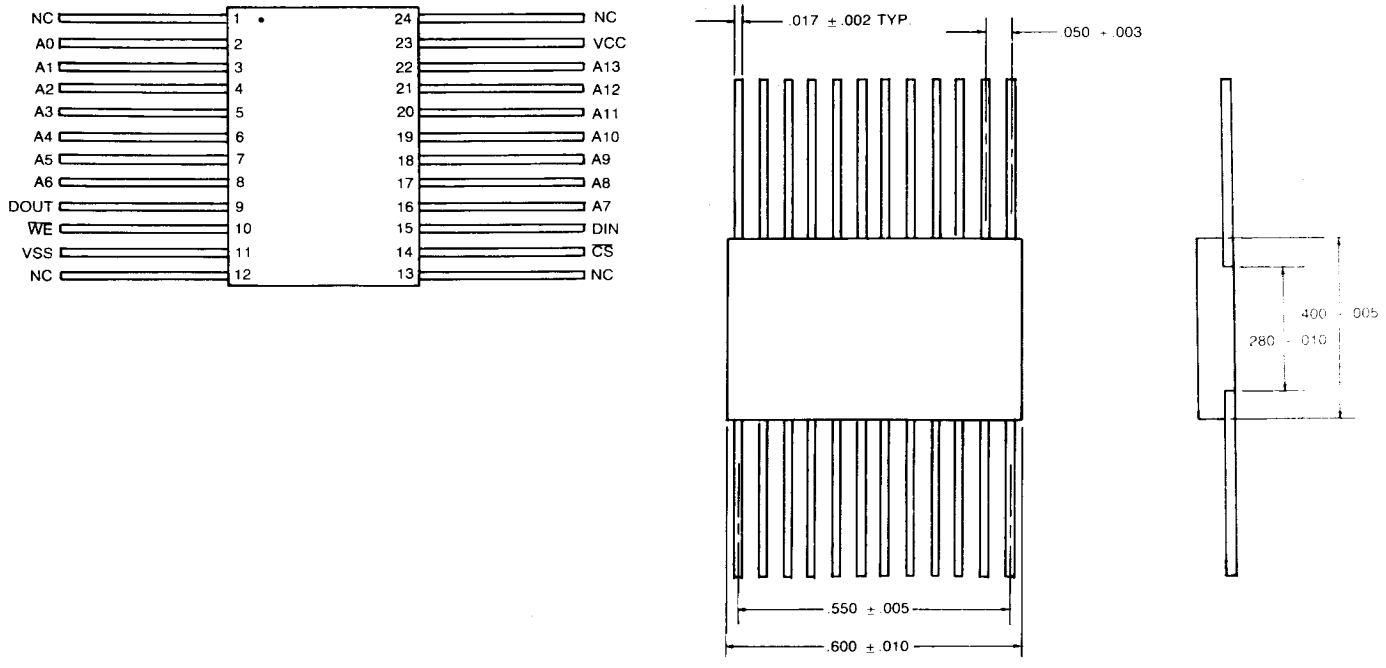
HC6167R In a 20-Pin Leadless Chip Carrier



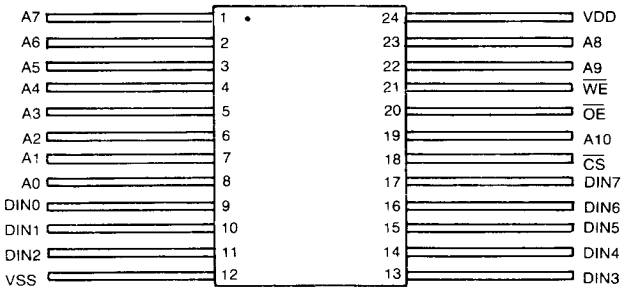
HC6167R in a 20-Pin DIP

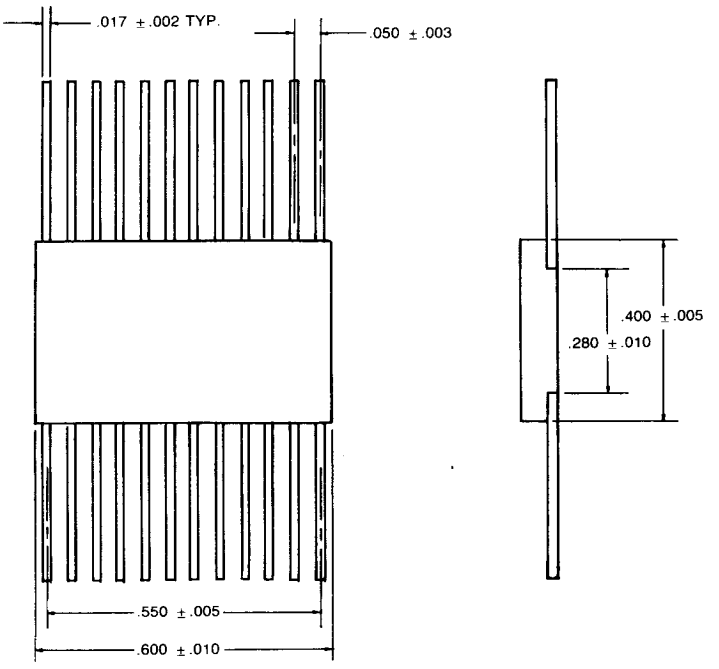


HC6167R in a 24-Pin Flatpack

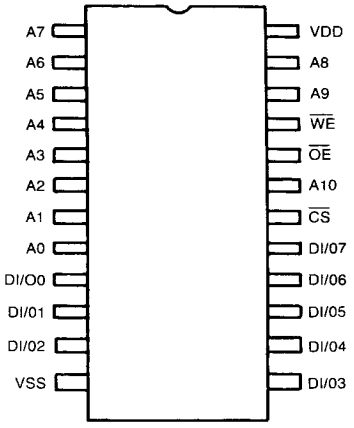


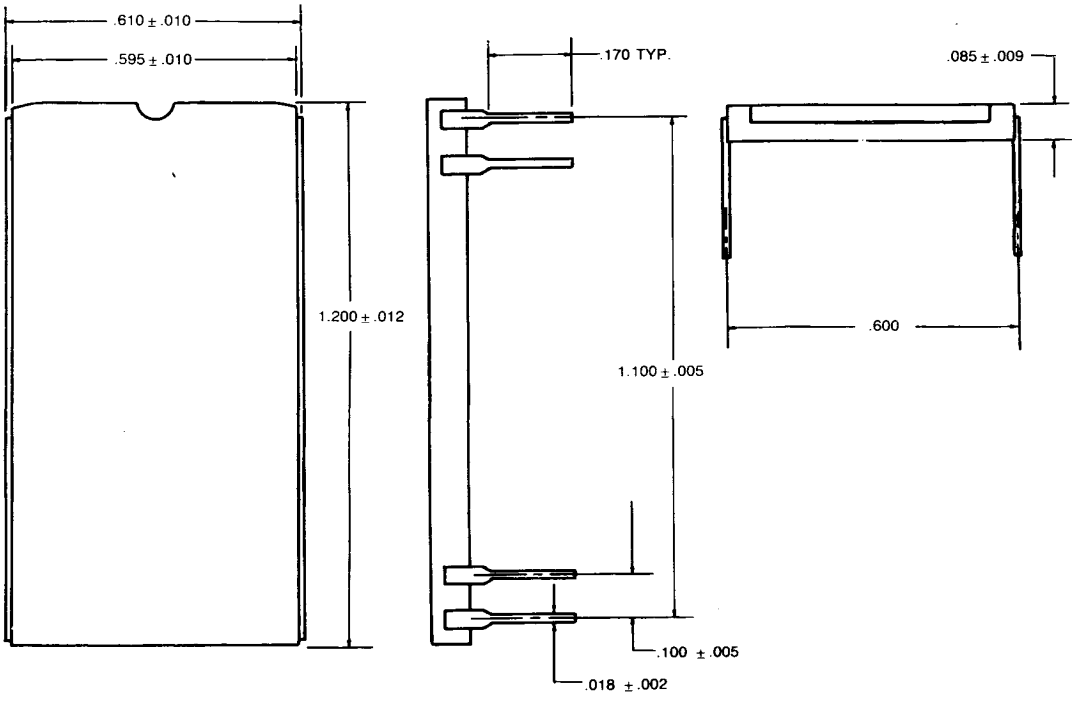
HC6116R in a 24-Pin Flatpack





HC6116R in a 24-Pin Dip





Military Standard Screening Specifications

Procedure	Prototype 25°C	Honeywell-B Tactical	Honeywell-S Space
Wafer Processing	X	X	X
SEM-Modified M2018			X
Wafer Probe	X	X	X
Presaw Visual - Mod M2010, B		X	X
Wafer Saw	X	X	X
Die Visual - Mod M2010, B		X	X
Assembly, Die & Wire Bond Check	X	X	X
Non-Destructive Bond Pull - M2023			X
Pre-Cap Visual - Mod M2010, B		X	X
Q.A. Gate Pre-Cap Visual		X	X
Clean, Bake, Lid Seal	X	X	X
Package Marking	X	X	X
Stabilization Bake, M1008, C		X	X
Temperature Cycle, M1010, C		X	X
Const. Accel - Mod M2001, E		X	X
PIND - M2020, A			X
Radiography - M2012, Y Axis			X
Lead Trim			X
Electrical Test, DC, Function, 25°C		X	X
Static Burn-In M1015, A-E			48 Hours
Electrical Test, DC, Function, 25°C			X
P.D.A.			Limit = 10%
Dynamic Burn In - M1015, A-E		160 Hours	240 Hours
Electrical Test, AC, DC, Function, +25°C	X	X	X
P.D.A.		Limit = 5%	Limit = 3%, 5%
Electrical Test, AC, DC, Function, -55°C, +125°C		Q.A. Witness	Q.A. Witness
Leak - M1014, Fine-B, Gross-C		X	X
QCI Modified - M5005			X
External Visual - M2009		X	X
Q.A. Gate - External Visual - M2009		X	X
Q.A. Gate - Plant Clearance		X	X

Note: SRAMs are available screened to any program-specific screening flow. Consult Honeywell.

For more information on Radiation Hardened Products contact:

Honeywell Inc.
SSED
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
(303) 577-3574

Together, we can find the answers.

Honeywell