Q18843

T-46-07-12

National Semiconductor

74ACTQ18843
18-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The 'ACTQ18843 bus interface latch contains eighteen non-inverting D-type latches with TRI-STATE outputs. The 'ACTQ18843 is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths. The device is byte controlled. Latch Enable (LE), Output Enable ($\overline{OE}$), Preset ($\overline{PRE}$), and Clear ($\overline{CLR}$) are common to each byte and can be shorted together for full 18-bit operation.

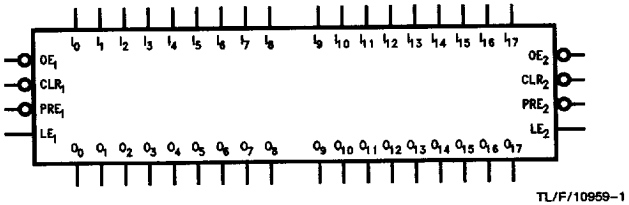
The 'ACTQ18843 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Broadside pinout allows for easy board layout
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Separate control logic for each byte
- Extra data width for wider address/data paths or buses carrying parity
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output loading specs for both 50 pF and 250 pF loads
- 18-bit version of 'ACTQ843

Ordering Code: See Section 8

Logic Symbol



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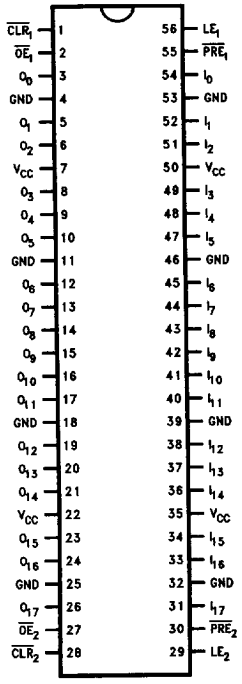
Connection Diagram

Pin Assignment for SSOP



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Functional Description

The 'ACTQ18843 consists of eighteen D-type latches with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of each other. The control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. The flip-flops are transparent to the Latch Enable (LE_n) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE_n LOW-to-HIGH transition, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}_n$) is LOW. When $\overline{OE}_n$ is HIGH, the bus output is in the high impedance state. In addition to the LE_n and $\overline{OE}_n$ pins, the 'ACTQ18843 has a Clear ($\overline{CLR}_n$) pin and Preset ($\overline{PRE}_n$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}_n$ is LOW, the outputs are LOW if $\overline{OE}_n$ is LOW. When $\overline{CLR}_n$ is HIGH, data can be entered into the latch. When $\overline{PRE}_n$ is LOW, the outputs are HIGH if $\overline{OE}_n$ is LOW. Preset overrides $\overline{CLR}_n$.

Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$\overline{CLR}_n$	Clear (Active Low)
$\overline{PRE}_n$	Preset (Active Low)
LE_n	Latch Enable
I_0–I_{17}	Inputs
O_0–O_{17}	Outputs

Function Table (Note 1)

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	I_n	Q	O_n	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Note 1: The table represents the logic for one byte. The two bytes are independent of each other and function identically.

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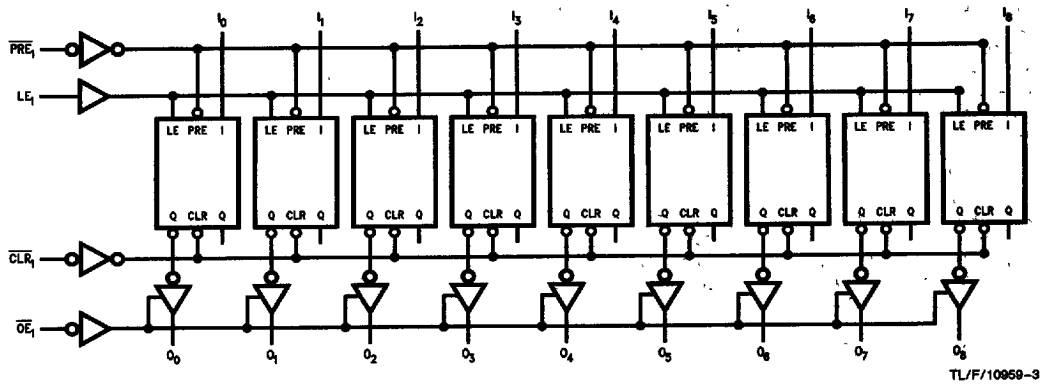
Logic Diagram

Byte 1 (0:8)



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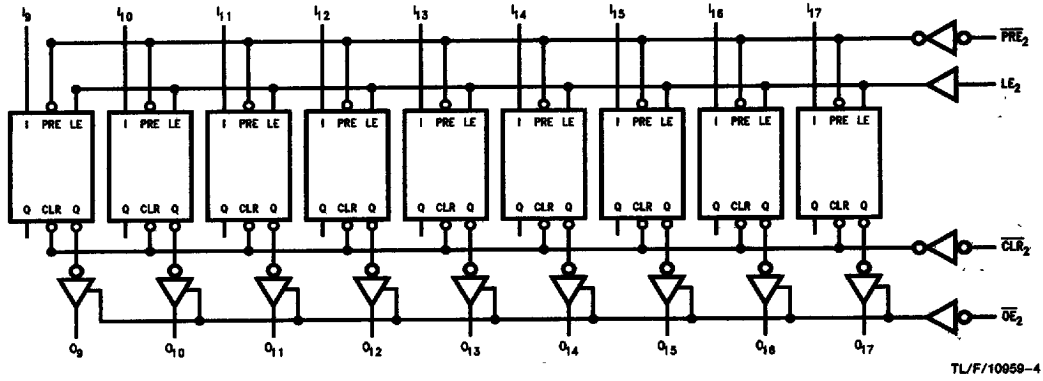
Byte 2 (9:17)



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin	±50 mA
Junction Temperature PDIP/SOIC	+140°C
Storage Temperature	−65°C to +150°C
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Note 2: For qualification information please refer to the NSC SSOP Qualification Handbook.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate dV/dt	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ T_A = +25°C	74ACTQ T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.44		I_{OL} 24 mA
V_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} −2.1V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}					−75	mA	V_{OHD} = 3.85V Min

*All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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DC Electrical Characteristics for ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8		V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.8		V	*Figures 2-12, 13* (Notes 2, 3)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 1.0	V_{OH} + 1.5		V	*Figures 2-12, 13* (Notes 1, 3)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 1.0	V_{OH} − 1.8		V	*Figures 2-12, 13* (Notes 1, 3)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0		V	(Notes 1, 4)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8		V	(Notes 1, 4)

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PHL} t_{PLH}	Propagation Delay I_n to O_n	5.0	5.0 5.2	6.0 6.4	9.0 9.0	4.2 4.5	9.5 9.5	ns	2-3, 4
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	5.0	5.8 6.2	6.4 7.5	9.0 9.5	5.0 5.6	9.5 10.5	ns	2-3, 4
t_{PLH}	Propagation Delay PRE to O_n	5.0	6.9	7.6	10.5	6.2	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay CLR to O_n	5.0	5.9	7.2	10.5	5.1	11.0	ns	2-3, 4
t_{PZL} t_{PZH}	Output Enable Time	5.0	4.6 4.3	6.3 6.3	9.0 9.0	4.1 3.9	9.5 9.5	ns	2-5, 6
t_{PLZ} t_{PHZ}	Output Disable Time	5.0	3.0 3.5	4.2 4.8	5.6 6.0	2.6 3.0	11.5 11.5	ns	2-5, 6

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF Typ	Guaranteed Minimum	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
t_s	Setup Time, HIGH or LOW, Input to LE	5.0		3.0	3.0	ns	2-7
t_h	Hold Time, HIGH or LOW, Input to LE	5.0		1.5	1.5	ns	2-7
t_w	LE Pulse Width, HIGH or LOW	5.0		4.0	4.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_w	$\overline{CLR}$ Pulse Width, HIGH or LOW	5.0		4.0	4.0	ns	2-4
t_w	$\overline{PRE}$ Pulse Width, HIGH or LOW	5.0		4.0	4.0	ns	2-4
t_{rec}	Recovery Time, $\overline{PRE}$ to LE	5.0		6.0	6.0	ns	2-4, 7
t_{rec}	Recovery Time, $\overline{CLR}$ to LE	5.0		6.0	6.0	ns	2-4, 7

*Voltage Range 5.0 is 5.0V ±0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ $T_A = -40°C$ to $+85°C$, V_{CC} = Com, $C_L = 50$ pF, 16 Outputs Switching (Note 2)			74ACTQ $T_A = -40°C$ to $+85°C$, V_{CC} = Com, $C_L = 250$ pF (Note 3)		54ACTQ T_A = Mil, V_{CC} = Mil, $C_L = 250$ pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay	7.2 6.3	8.3 7.2	9.5 8.5	7.5 7.0	13.5 12.5			ns
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	7.5 7.4	8.2 7.5	9.0 8.0	7.9 7.8	13.0 15.0			ns
t_{PLH}	Propagation Delay PRE to O_n	7.0	8.0	9.5	7.0	12.0			ns
t_{PHL}	Propagation Delay CLR to O_n	7.0	7.6	9.0	7.5	12.5			ns
t_{PZH} t_{PZL}	Output Enable Time	5.4 5.3	6.5 6.4	7.3 7.4	(Note 4)		(Note 4)		ns
t_{PHZ} t_{PLZ}	Output Disable Time	3.6 3.2	4.5 4.0	5.4 5.2	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output								ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output								ns
t_{OSHZ} (Note 1)	Pin to Pin Skew LE to Output								ns
t_{OSLH} (Note 1)	Pin to Pin Skew LE to Output								ns
t_{OSLH} (Note 1)	Pin to Pin Skew PRE to Output								ns
t_{OSHL}	Pin to Pin Skew CLR to Output								ns
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output								ns
t_{OST} (Note 1)	Pin to Pin Skew LE to Output								ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

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Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	95	pF	V_{CC} = 5.0V