CT1487M & CT1589M SERIES

MIL-STD-1553
Low Power Single and Dual Transceiver

2nd EDITION

FEATURES

- Available in ±15 V (CT1487M) and ±12 V (CT1589M) versions
- AC interstage coupling prevents static burnout
- Receiver filtered to improve S/N ratio of system
- Dissipates only 1.3 watt total at 25% transmitting duty cycle (dual unit - 1.8 watts total). 100% duty cycle permissible at 125°C case temperature
- 20 mV typical output offset
- Meets MIL-STD-1553A/B
- Screened per Figure 8
- 24 pin double dip package or flat pack for single unit
- 36 pin double dip package or flat pack for dual unit
- TTL compatible

NOTE: All data shown is for a single transceiver unless otherwise noted. Dual transceivers are two completely independent units in a common package.

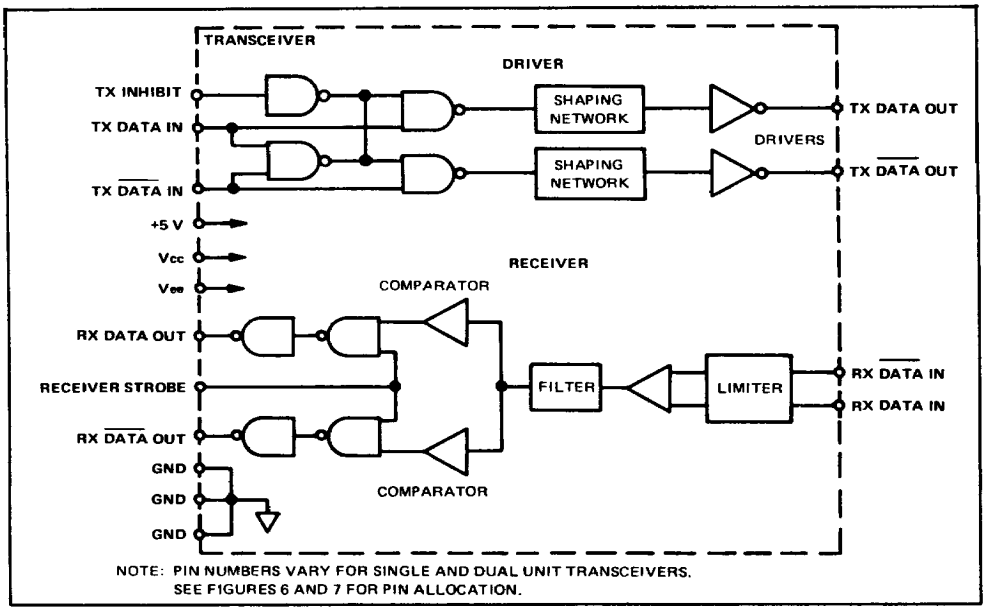


FIGURE 1. FUNCTIONAL DIAGRAM

GENERAL DESCRIPTION

The CT1487M/CT1589M family of single and dual transceivers is a second generation series incorporating monolithic bipolar devices for improved reliability and producibility. For thermal considerations, the drive stage transistors are "off" the bipolar array. Input/output signals are compatible with both MIL-STD-1553A and B systems.

DETAILED DESCRIPTION

RECEIVER DESCRIPTION The Receiver section accepts bi-phase differential data at the input and produces two TTL signals at the output. The outputs are RX DATA OUT and RX $\overline{\text{DATA}}$ OUT and represent positive and negative excursions, respectively, of the input beyond a predetermined threshold. See Figure 2 for receiver logic waveforms.

The positive and negative thresholds are designed for optimum word error rate. The receiver begins to detect Data Bus signals (1 MHz, sinusoidal) that exceed 0.9 volt nominal peak-to-peak when used with the specified transformer. See Figure 4 for typical input/output connections.

If the RECEIVER STROBE input is LOW, the RX DATA OUT and RX $\overline{\text{DATA}}$ OUT are inhibited. If unused, a 2K-ohm pullup to +5V is recommended.

NOTE: See ORDERING INFORMATION for units with inverted outputs. (Pg 7)

DRIVER DESCRIPTION The Driver section accepts complementary TTL data at the input. When coupled to the Data Bus with the specified transformer (isolated on the Data Bus side with two 55-ohm fault isolation resistors and loaded by two 70-ohm terminations plus additional receivers), the Data Bus signal produced is 6.8 volts nominal peak-to-peak (at point A, Figure 4).

When both TX DATA IN and TX $\overline{\text{DATA}}$ IN inputs are both held LOW or held HIGH, the driver output becomes a high impedance and is removed from the line. In addition, an overriding TX INHIBIT input provides for removal of the driver output from the line. A HIGH applied to the TX INHIBIT input takes priority over the condition of the data inputs and disables the driver. See Figure 3 for driver logic waveforms.

TX DATA IN and TX $\overline{\text{DATA}}$ IN inputs must be complementary waveforms of 50% average duty cycle and with less than 15 ns skew between them.

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

	CT1487M	CT1589M
Power supply voltage (V_{cc})	-0.3 to +18.0 V	-0.3 to +18.0 V
Power supply voltage (V_{ee})	+0.3 to -18.0 V	+0.3 to -18.0 V
Power supply voltage (V_{ccl})	-0.3 to +7.0 V	-0.3 to +7.0 V
Logic input voltage (RECEIVER STROBE, INHIBIT, TX $\overline{\text{DATA}}$ IN, TX DATA IN)	-0.3 to +5.5 V	-0.3 to +5.5 V
Receiver differential input (RX DATA IN, RX $\overline{\text{DATA}}$ IN)	±20 V (40 V p-p)	±20 V (40 V p-p)
Receiver input voltage (RX DATA IN or RX $\overline{\text{DATA}}$ IN)	±15 V	±15 V
Driver output current (TX DATA OUT or TD $\overline{\text{DATA}}$ OUT)	+200 mA	+300 mA
Transmission duty cycle at T_c = 125°C	100%	100%
Operating case temperature range (T_c)	-55°C to +125°C	-55°C to +125°C

POWER AND THERMAL DATA, TOTAL HYBRID (DRIVER AND RECEIVER)

PARAMETER/CONDITION	SYMBOL	CT1487M				CT1589M					UNIT
		MIN	TYP		MAX	MIN	TYP		MAX		
			S*	D*	S* D*		S*	D*	S*	D*	
Power supply voltages	V_{cc}	14.25	15		15.75	11.4	12		12.6		V
	V_{ee}	-14.25	-15		-15.75	-11.4	-12		-12.6		V
	V_{ccl}	4.5	5		5.5	4.5	5		5.5		V
Power dissipation of most critical (hottest) device in hybrid during continuous transmission (100% duty cycle)	P_c	Note 1	350		500	Note 1	350		500		mW
Thermal resistance, most critical device	θ_{jc}				60				60		°C/W
Junction to case temperature rise of most critical device at 100% duty cycle transmission	T_{jc}				30				30		°C
Total supply current "standby" mode, or transmitting at less than 1% duty cycle (e.g. 20 µs of transmission every 2 ms or longer interval)	I_{cc}		15	30	22 44		15	30	22	44	mA
	I_{ee}	Note 2	25	50	35 70	Note 2	25	50	35	70	mA
	I_{ccl}	Note 2	32	64	45 90	Note 2	32	64	45	90	mA
Total supply current transmitting at 1 MHz into a 35-ohm load at point A in Figure 4 — DUTY CYCLE 25%	$I_{cc}25$	Note 3	55	70	75 100	Note 3	70	85	95	120	mA
DUTY CYCLE 100%	$I_{cc}100$	Note 3	185	200	235 260	Note 3	224	240	290	315	mA

* S = single unit, D = dual unit (one unit transmitting)

NOTE 1: Decreases linearly to zero at zero duty cycle.
NOTE 2: I_{ee} and I_{ccl} limits do not change with mode of operation or duty cycle.
NOTE 3: Decreases linearly to applicable "standby" value at zero duty cycle.

ELECTRICAL CHARACTERISTICS, RECEIVER SECTION (See Figure 2)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Differential input impedance DC to 1 MHz	Z_{in}	9 K			ohms
Differential voltage range	V_{idr}	±20 V			V_{peak}
Input common mode voltage range	V_{icr}	±10 V			V_{peak}
Common mode rejection ratio (from point A, Figure 4)	CMRR	40			dB
STROBE characteristics					
(Logic "0" inhibits output)					
"0" input current (V_s = 0.4 V)	I_{il}			-1	mA
"1" input current (V_s = 2.7 V)	I_{ih}			40	μA
"0" input voltage	V_{il}			0.7	V
"1" input voltage	V_{ih}	2			V
Threshold characteristics (sine wave at 1 MHz)	V_{th1}	0.8		1.1	V_{p-p}
NOTE: Threshold voltages refer to point A, Figure 4.					
Filter characteristics 2 MHz	V_{th2}	1.5		8	V_{p-p}
(sine wave input) 3 MHz	V_{th3}	5			V_{p-p}
OUTPUT CHARACTERISTICS					
"1" state (I_{source} = 400 μA)	V_{oh}	2.5	3.4		
"0" state (I_{sink} = 4 mA)	V_{oh}			0.5	
NOTE: With receiver input below threshold both RX DATA OUT and RX $\overline{\text{DATA}}$ OUT remain in "0" state.					
Delay (average) from differential input zero crossings to RX DATA OUT and RX $\overline{\text{DATA}}$ OUT output 50% points	t_{DRX}		340	450	ns

ELECTRICAL CHARACTERISTICS, DRIVER SECTION (See Figure 3)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
"0" input current (V_{in} = 0.4 V)	I_{il}			-1	mA
"1" input current (V_{in} = 2.7 V)	I_{ih}			100	μA
"0" input voltage	V_{il}			0.7	V
"1" input voltage	V_{ih}	2			V
Delay from TX INHIBIT (0 → 1) to inhibited output impedance	t_{DXOFF}		150	225	ns
Delay from TX INHIBIT (1 → 0) to active output impedance	t_{DXON}		100	150	ns
Differential output noise	V_{noi}			10	mV_{p-p}
Differential output impedance (inhibited) at 1 MHz	Z_{oi}	8K			ohms
OUTPUT CHARACTERISTICS					
Differential output level at point B, Figure 4 (145-ohm load)	V_o	26	28	35	V_{p-p}
Rise and fall times (10%-90% of p-p output)	t_r	100	160	300	ns
Output offset at point A in Figure 4 (35-ohm load) 2.5 μs after mid-bit crossing of parity bit of last word of a 660 μs message	V_{os}		±20	±75	mV peak
Delay from 50% point of TX DATA IN or TX $\overline{\text{DATA}}$ IN to zero crossing of differential output	t_{DTX}		100	150	ns

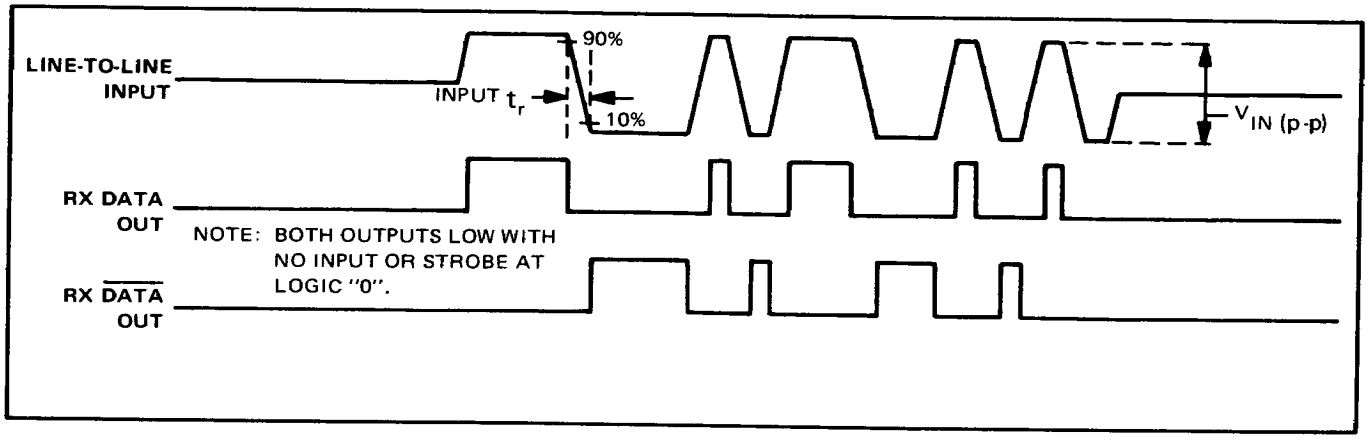


FIGURE 2. RECEIVER LOGIC WAVEFORMS
(FOR INVERTED DATA OUTPUT, SEE ORDERING INFORMATION)

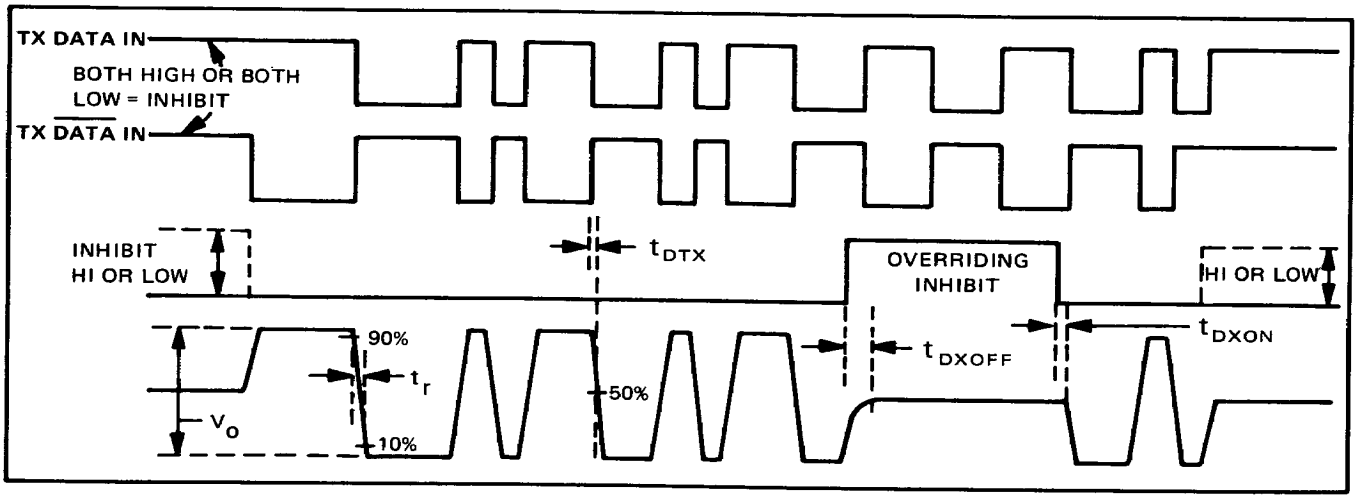
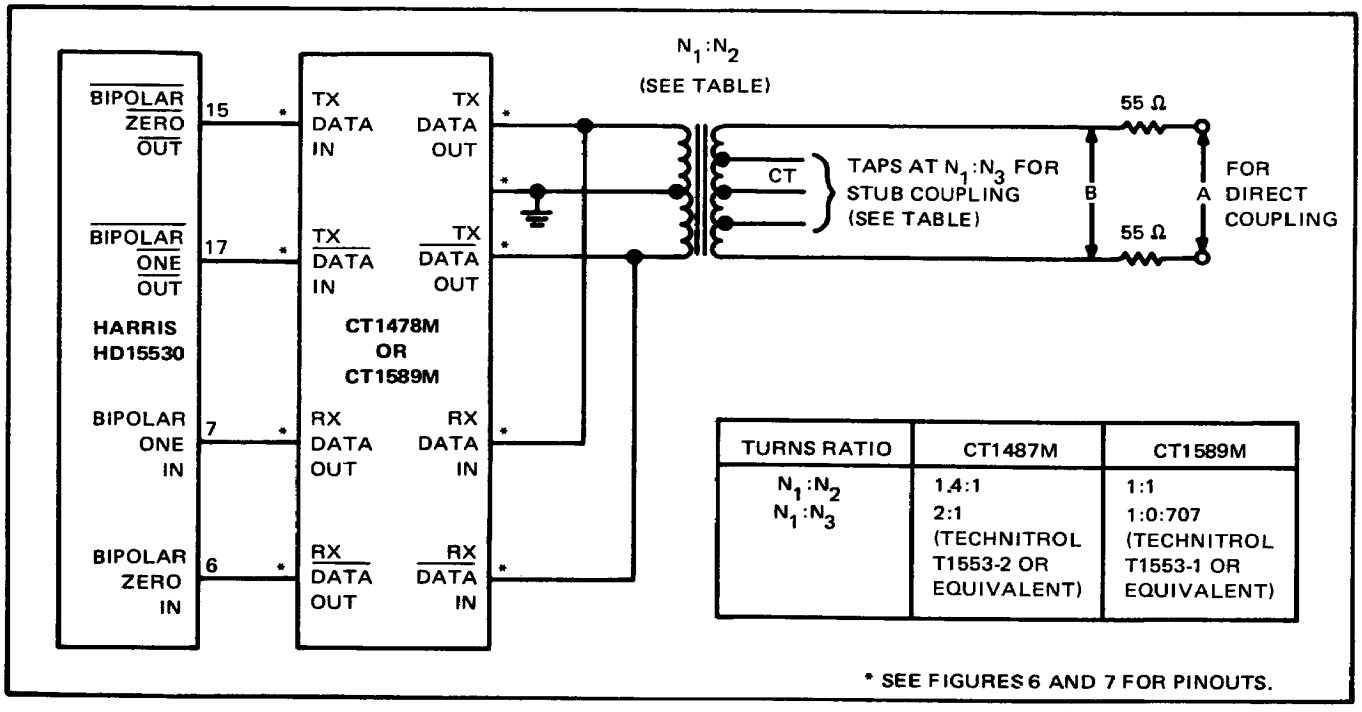


FIGURE 3. DRIVER LOGIC WAVEFORMS



TURNS RATIO	CT1487M	CT1589M
N_1:N_2	1.4:1	1:1
N_1:N_3	2:1 (TECHNITROL T1553-2 OR EQUIVALENT)	1:0:707 (TECHNITROL T1553-1 OR EQUIVALENT)

FIGURE 4. TYPICAL INPUT/OUTPUT CONNECTIONS

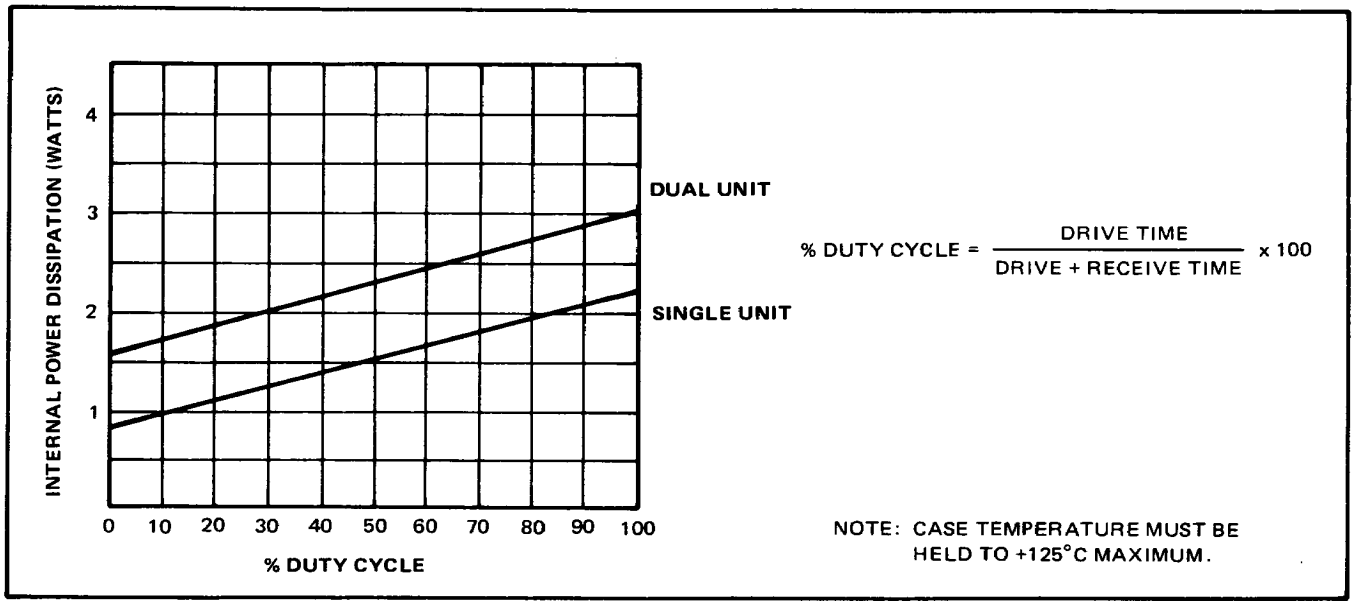
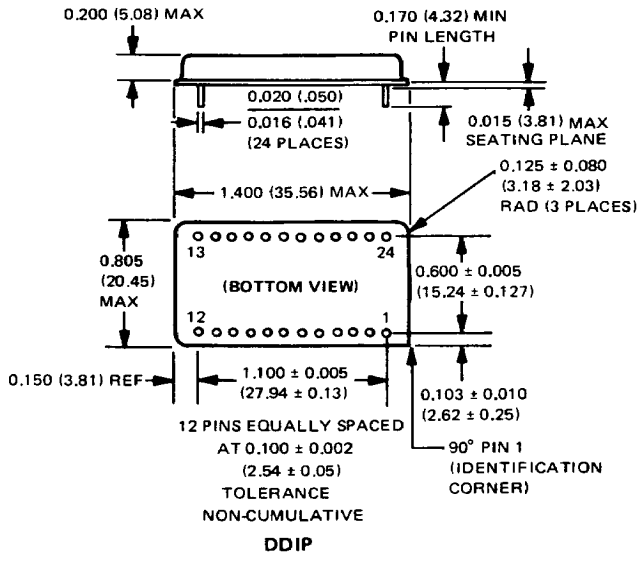
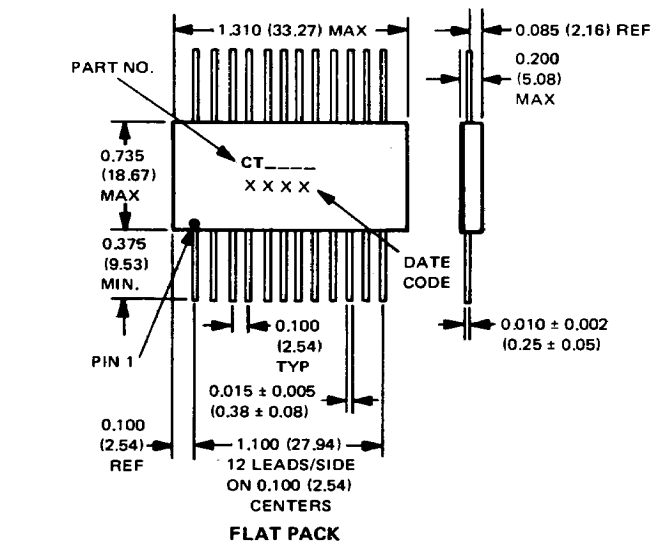


FIGURE 5. TYPICAL INTERNAL POWER DISSIPATION (TOTAL HYBRID)

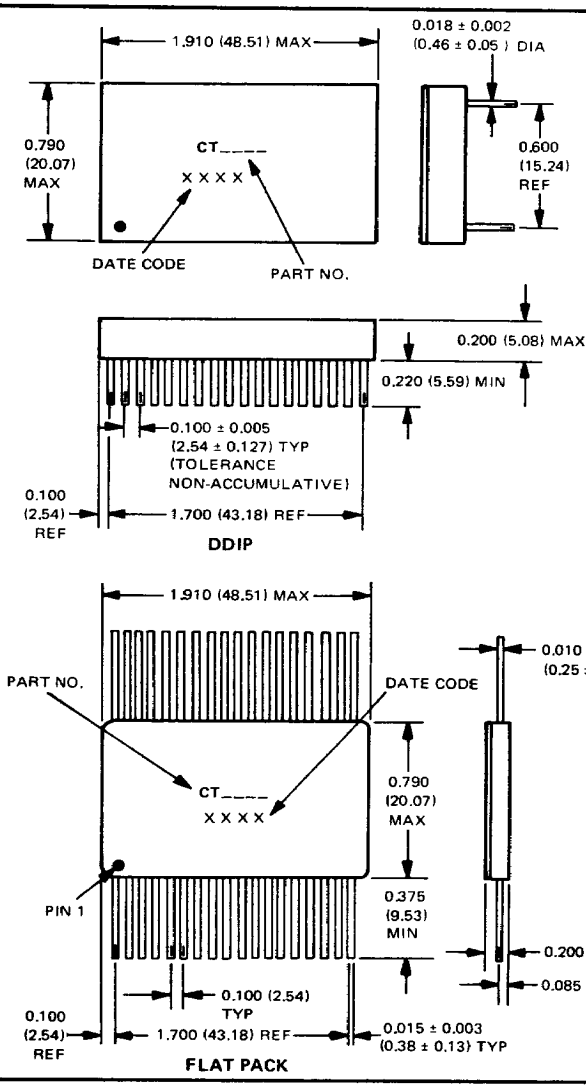


SINGLE UNIT (DDIP AND FLAT PACK)			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA OUT	13	Vcc
2	TX DATA OUT	14	N.C.
3	GND	15	RX DATA IN
4	N.C.	16	RX DATA IN
5	N.C.	17	N.C.
6	N.C.	18	GND
7	RX DATA OUT	19	Vee
8	STROBE	20	+5 V
9	GND	21	TX INHIBIT
10	RX DATA OUT	22	TX DATA IN
11	N.C.	23	TX DATA IN
12	N.C.	24	N.C.



NOTES:
1. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
2. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
3. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
4. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS OF MIL-STD-202E. METHOD 208C.

FIGURE 6. MECHANICAL OUTLINE AND PINOUTS (SINGLE UNIT)



DUAL UNIT (DDIP AND FLAT PACK)		
PIN	FUNCTION	CHANNEL
1	TX DATA OUT	1
2	TX $\overline{\text{DATA}}$ OUT	1
3	GND	
4	N.C.	
5	RX DATA OUT	1
6	STROBE	1
7	GND	
8	RX $\overline{\text{DATA}}$ OUT	1
9	N.C.	
10	TX DATA OUT	2
11	TX $\overline{\text{DATA}}$ OUT	2
12	GND	2
13	N.C.	2
14	RX DATA OUT	2
15	STROBE	2
16	GND	2
17	RX $\overline{\text{DATA}}$ OUT	2
18	N.C.	
19	Vcc	2
20	RX DATA IN	2
21	RX $\overline{\text{DATA}}$ IN	2
22	GND	
23	Vee	2
24	+5 V	2
25	TX INHIBIT	2
26	TX DATA IN	2
27	TX $\overline{\text{DATA}}$ IN	2
28	Vcc	1
29	RX DATA IN	1
30	RX $\overline{\text{DATA}}$ IN	1
31	GND	
32	Vee	1
33	+5 V	1
34	TX INHIBIT	1
35	TX DATA IN	1
36	TX $\overline{\text{DATA}}$ IN	1

NOTES:
1. GND PINS OF EACH SECTION SHOULD ALL BE CONNECTED EXTERNALLY.
2. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
3. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
4. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
5. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS OF MIL-STD-202E, METHOD 208C.

FIGURE 7. MECHANICAL OUTLINE AND PINOUTS (DUAL UNIT)

CT1487M/CT1589M SERIES			
TEST/INSPECTION	REQUIREMENT	METHOD MIL-STD-883	CONDITION
Internal Visual	100%	2017	N/A
Customer Pre-seal Inspection	When Specified	N/A	As Specified
Pre-seal Bake	24 Hrs @ 150 ±5°C	N/A	N/A
Seal/Mark	100%	---	---
Fine Leak	100%	1014	$1X10^{-7}$ cc/sec
Stabilization Cycle	100%	1008	C
Temperature Cycle	100%	1010	C
Centrifuge	Y1 Axis	2001	A
Pind Test	When Specified	2020	A or B as Specified
Fine Leak	100%	1014	$1X10^{-7}$ cc/sec
Gross Leak	100%	1014	N/A
Electrical Test	CTI ATP 100%	N/A	25°C
Burn-In	T_{CASE} = 125°C	1015	---
Final Test/Group A	CTI ATP 100%	---	+25°C, -55°C, +125°C Case
External Visual	100%	2009	---
Customer Inspection	As Required	---	---

FIGURE 8. TESTING AND SCREENING PROCEDURE

ORDERING INFORMATION

"Inverted Receiver Data Output" refers to the logic state of RX DATA OUT and RX $\overline{\text{DATA}}$ OUT when the bus is quiet. All part numbers with the "I" suffix produce logic "1" at the receiver outputs for quiet bus.

CT1487M - ±15 V Single Unit Plug-in Package
CT1487MFP - ±15 V Single Unit Flat Pack
CT1487MI - ±15 V Single Unit Plug-in Package, Inverted Receiver Data Outputs
CT1487MIFP - ±15 V Single Unit Flat Pack, Inverted Receiver Data Outputs
CT1487D - ±15 V Dual Unit Plug-in Package
CT1487DI - ±15 V Dual Unit Plug-in Package, Inverted Receiver Data Outputs
CT1487DF - ±15 V Dual Unit Flat Pack
CT1487DIFP - ±15 V Dual Unit Flat Pack, Inverted Receiver Data Outputs
CT1589M - ±12 V Single Unit Plug-in Package
CT1589MFP - ±12 V Single Unit Flat Pack
CT1589MI - ±12 V Single Unit Plug-in Package, Inverted Receiver Data Outputs
CT1589MIFP - ±12 V Single Unit Flat Pack, Inverted Receiver Data Outputs
CT1589D - ±12 V Dual Unit Plug-in Package
CT1589DFP - ±12 V Dual Unit Flat Pack
CT1589DI - ±12 V Dual Unit Plug-in Package, Inverted Receiver Data Outputs
CT1589DIFP - ±12 V Dual Unit Flat Pack, Inverted Receiver Data Outputs

CTI is a major supplier of standard products for MIL-STD-1553, McDonnell Douglas, NTDS, STANAG 4153 (Low Level Serial), and other data bus interface systems. Our standard components are screened to Figure 8. CTI is also a supplier of Custom Analog, Digital, and Power Hybrid products. For information about any of our products, please contact our factory or one of our local Sales Representatives.

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