4x128Kx32 Synchronous SRAM CARD EDGE DIMM

FEATURES

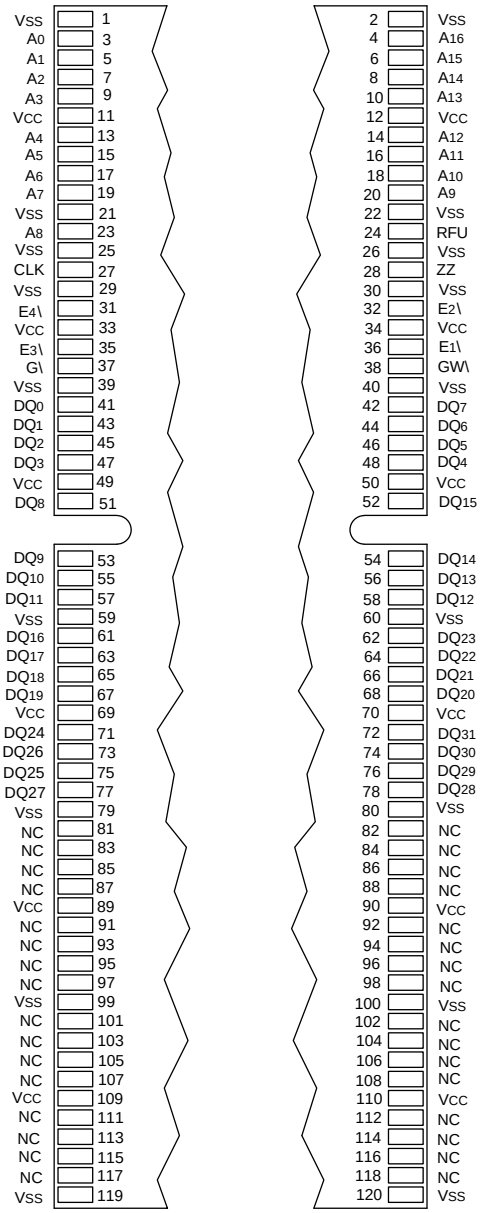
- 4x128Kx32 Synchronous
- Access Speed(s): T_{KHQV} = 9.5, 10, 11, 12, 15ns
- Flow-Through Architecture
- Clock Controlled Registered Bank Enables (E_1\, E_2\, E_3\, E_4\)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW\)
- Aysnchronous Output Enable (G\)
- Internally self-timed Write
- Gold Lead Finish
- 3.3V ±10%, -5% Operation
- Common Data Input/Output
- High Capacitance (30pF) drive, at rated Access Speed
- Single total array Clock
- Multiple Vcc and Vss

The EDI2GG432128VxxD is a Synchronous SRAM, 60 position Card Edge; DIMM (120 contacts) Module, organized as 4x128Kx32. The Module contains four (4) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Synchronous Only, Flow-Through, Early Write Device. This Module provides high performance, ultra fast access times at a cost per bit benefit over BiCMOS Asynchronous SRAM based devices. As well as improved cost per bit, the use of Synchronous or Synchronous Burst devices or modules can ease the memory subsystem design by reducing or easing the memory controller requirement.

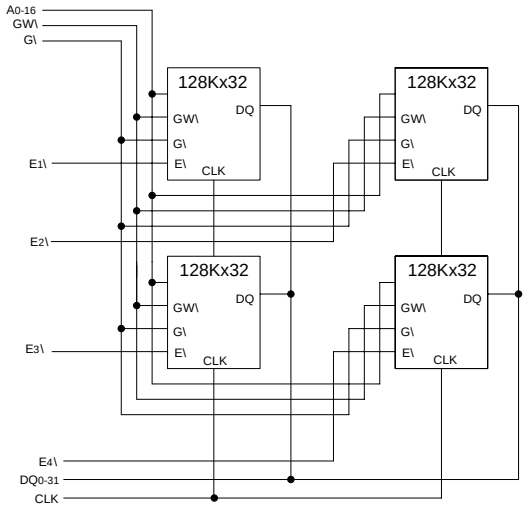
Synchronous operations are in relation to an externally supplied clock, registered address, registered global write, registered enables as well as an Asynchronous Output enable. All read and write operations to this module are performed on long words (double words) 32 bit operations.

Write cycles are internally self timed and are initiated by a rising clock edge. This feature relieves the designer the task of developing external write pulse width circuitry.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

DQ_{0-32}	Input/Output Bus
A_{0-16}	Address Bus
E_{1-4}\	Synchronous Bank Enables
CLK	Array Clock
GW\	Synchronous Global Write Enable
G\	Asynchronous Output Enable
Vcc	3.3V Power Supply
Vss	Ground
NC	No Connect

PIN DESCRIPTIONS

DIMM Pins	Symbol	Type	Description
3, 5, 7, 9, 13, 15, 17, 19, 20, 23, 18, 16, 14, 10, 8, 6,4	A_{0-16}	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A_0 and A_1, during burst and wait cycle.
38	GW\	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE\ and BWx\ lines and must meet the setup and hold times around the rising edge of CLK.
27	CLK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
36, 32	E1, E2\ E3\, E4\	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual bank andto gate ADSP\.
37	G\	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
Various	DQ_{0-32}	Input/Output	Data Inputs/Outputs: First byte is DQ_{0-7}, second byte is DQ_{8-15}, third byte is DQ_{16-23}, fourth byte is DQ_{24-31}, fifth byte is DQ_{32-39}, sixth byte is DQ_{40-47}, seventh byte is DQ_{48-55} and the eight byte is DQ_{56-64}.
Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground

SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1\	E2\	E3\	E4\	GW\	G\	CLK	DQ
Synchronous Write-Bank 1	L	H	H	H	L	H	↑	High-Z
Synchronous Read-Bank 1	L	H	H	H	H	L	↑	
Synchronous Write-Bank 2	H	L	H	H	L	H	↑	High-Z
Synchronous Read-Bank 2	H	L	H	H	H	L	↑	
Synchronous Write-Bank 3	H	H	L	H	L	H	↑	High-Z
Synchronous Read-Bank 3	H	H	L	H	H	L	↑	
Synchronous Write-Bank 4	H	H	H	L	L	H	↑	High-Z
Synchronous Read-Bank 4	H	H	H	L	H	L	↑	
Snooze Mode	X	X	X	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
Vin	-0.5V to Vcc +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

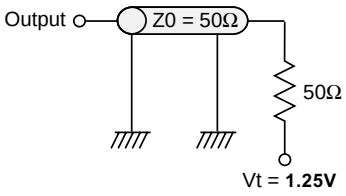
Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.14	3.3	3.6	V
Supply Voltage	V_{SS}	0.0	0.0	0.0	V
Input High	V_{IH}	2.2	3.0	V_{CC} +0.3	V
Input Low	V_{IL}	-0.3	0.0	0.8	V
Input Leakage	I_{LI}	-2	1	2	µA
Output Leakage	ILo	-2	1	2	µA
Output High (I_{OH} = -4mA)	V_{OH}	2.4	-	-	V
Output Low (I_{OL} = 8mA)	V_{OL}	-	-	0.4	V

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

Description	Symbol	Typ	9.5	10	11	Max 12	Max 15	Units
Power Supply Current	I_{CC1}	0.78	*	1.1	1.0	1.0	1.0	A
Power Supply Current Device Selected,No Operation	Icc	325	*	760	760	500	500	mA
Snooze Mode	I_{CCZZ}	80	*	120	120	120	120	mA
CMOS Standby	I_{CC3}	200	*	360	360	360	360	mA
Clock Running-Deselect	I_{CCK}	300	*	550	500	380	350	mA

*TBD

AC TEST CIRCUIT



AC Output Load Equivalent

AC TEST CONDITIONS

Parameter	I/O	Unit
Input Pulse Levels	Vss to 3.0	V
Input and Output Timing Levels	1.25	V
Output Test Equivalencies	See figure, at left	

READ CYCLE TIMING PARAMETERS

Description	Sym	9.5ns Min	9.5ns Max	10ns Min	10ns Max	11ns Min	11ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Clock Cycle Time	t_{KHKH}	*	*	12		12		15		20		ns
Clock High Time	t_{KHKL}	*	*	5		5		5		6		ns
Clock Low Time	t_{KLKH}	*	*	5		5		5		6		ns
Clock to Output Valid	t_{KHQV}	*	*		10		11		12		15	ns
Clock to Output Invalid	t_{KHQX1}	*	*	3		3		3		3		ns
Clock to Output Low-Z	t_{KHQX}	*	*	2		2		2		2		ns
Output Enable to Output Valid	t_{GLQV}	*	*		5		5		5		6	ns
Output Enable to Output Low-Z	t_{GLQX}	*	*	0		0		0		0		ns
Output Enable to Output High-Z	t_{GHQZ}	*	*		5		5		5		6	ns
Address Setup	t_{AVKH}	*	*	2.5		2.5		2.5		2.5		ns
Bank Enable Setup	t_{EVKH}	*	*	2.5		2.5		2.5		2.5		ns
Address Hold	t_{KHAX}	*	*	1.0		1.0		1.0		1.0		ns
Bank Enable Hold	t_{KHEX}	*	*	1.0		1.0		1.0		1.0		ns

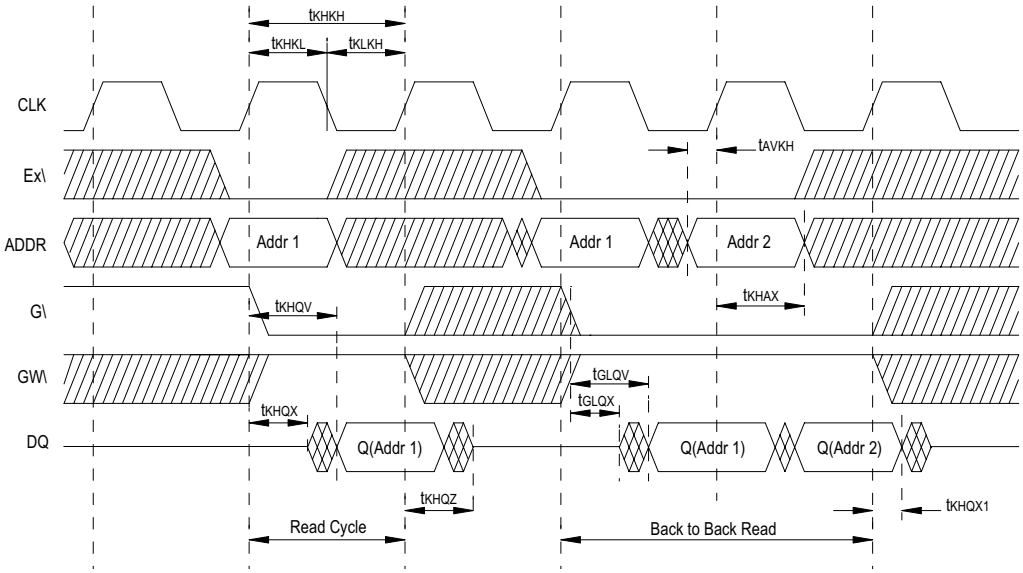
**TBD*

WRITE CYCLE TIMING PARAMETERS

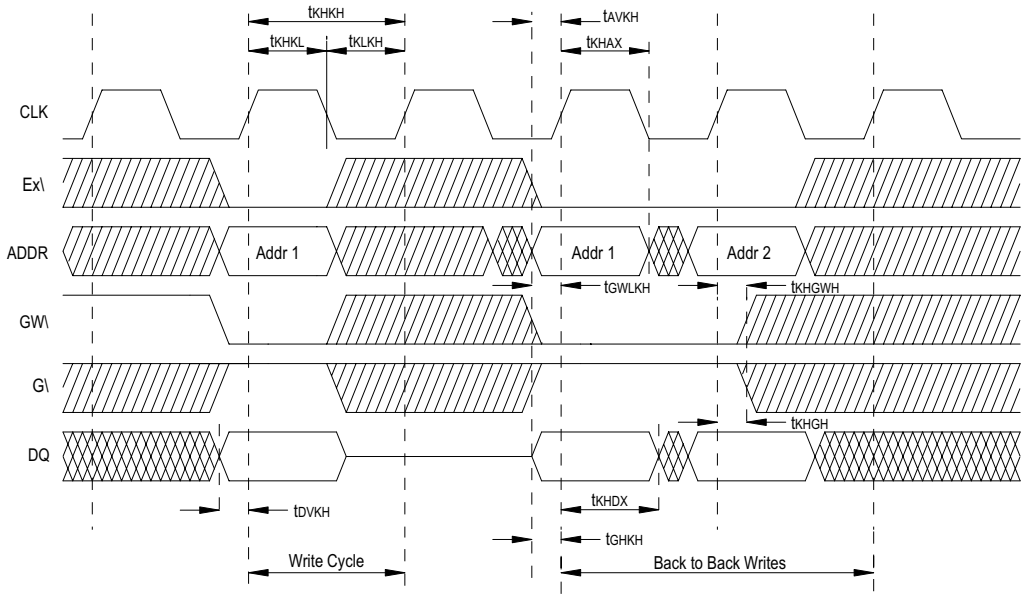
Description	Sym	9.5ns Min	9.5ns Max	10ns Min	10ns Max	11ns Min	11ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Clock Cycle Time	t_{KHKH}	*	*	12		12		15		20		ns
Clock High Time	t_{KHKL}	*	*	5		5		5		6		ns
Clock Low Time	t_{KLKH}	*	*	5		5		5		6		ns
Address Setup	t_{AVKH}	*	*	2.5		2.5		2.5		2.5		ns
Address Hold	t_{KHAX}	*	*	1.0		1.0		1.0		1.0		ns
Bank Enable Setup	t_{EVKH}	*	*	2.5		2.5		2.5		2.5		ns
Bank Enable Hold	t_{KHEX}	*	*	1.0		1.0		1.0		1.0		ns
Global Write Enable Setup	t_{WVKH}	*	*	2.5		2.5		2.5		2.5		ns
Global Write Enable Hold	t_{KHWX}	*	*	1.0		1.0		1.0		1.0		ns
Data Setup	t_{DVKH}	*	*	2.5		2.5		2.5		2.5		ns
Data Hold	t_{KHDX}	*	*	1.0		1.0		1.0		1.0		ns

**TBD*

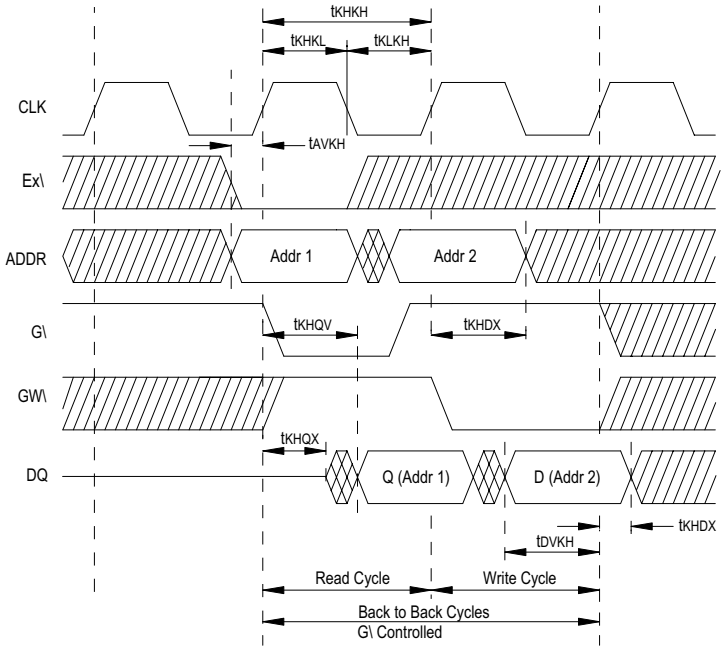
SYNCHRONOUS READ CYCLE



SYNCHRONOUS WRITE CYCLE

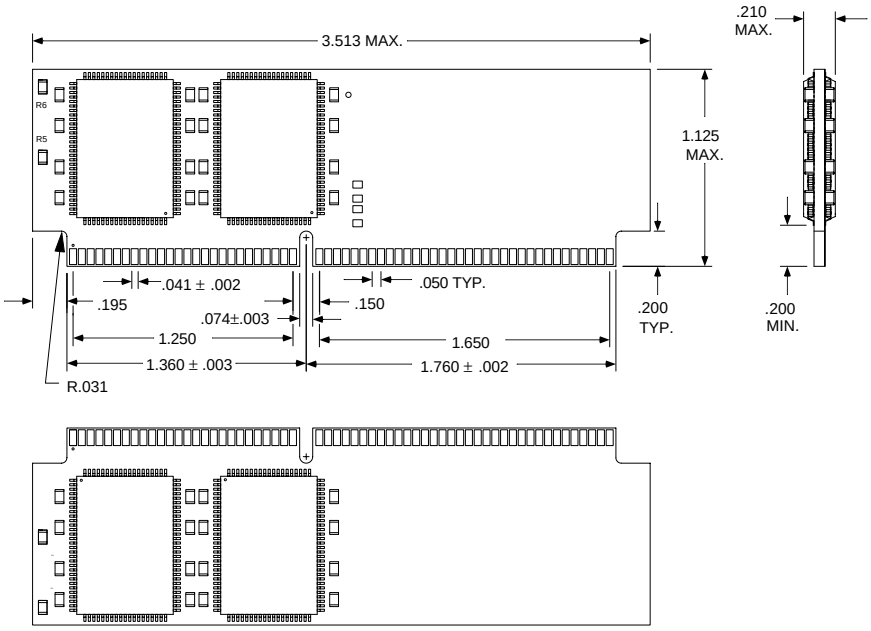


SYNCHRONOUS READ/WRITE CYCLE



PACKAGE DESCRIPTION: 120 LEAD CARD EDGE DIMM

Package No. 413



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Part Number	Organization	Voltage	Speed (ns)	Package
EDI2GG432128V95D*	4x128Kx32	3.3	9.5	120 Card Edge DIMM
EDI2GG432128V10D*	4x128Kx32	3.3	10	120 Card Edge DIMM
EDI2GG432128V11D	4x128Kx32	3.3	11	120 Card Edge DIMM
EDI2GG432128V12D	4x128Kx32	3.3	12	120 Card Edge DIMM
EDI2GG432128V15D	4x128Kx32	3.3	15	120 Card Edge DIMM

**Consult Factory for Availability*