ESS Technology, Inc.

ES978
Expansion Audio Mixer
Data Sheet

DESCRIPTION

The ES978 is an Expansion Audio Mixer for use in a docking station. The concept of docking is explained in the Theory of Operation section. The ES978 provides audio resources to an expansion unit with which a portable unit using the ES187x *Audio***Drive®** solution is docked.

The ES978 eliminates the need for bulky discrete components in a docking station. The master volume control of the ES978 is slaved to the ES187x mixer when the two are docked. Separate record and playback mixers allow for full-duplex operation between the ES187x-based portable and the ES978-based docking station.

A four-wire expansion analog bus and a two-wire serial control bus connect the ES187x and the ES978. This connection is used for a hot-docking interface. The two-wire digital status and data communication between the ES978 and ES187x supports register shadowing.

The ES978 offers several advantages, such as a digital joystick interface which reduces host overhead for the dual game port, a selectable interface for either the ES689/ES69x wavetable or an I²S Zoom Video for MPEG audio, as well as 8 general-purpose inputs and 8 general-purpose outputs for flexible board design. These general-purpose I/Os can be slaved with the corresponding pins of the ES187x.

Advanced power management supports automatic power-down. As long as the ES187x portable unit and the ES978 docking station are connected, power-down states on both units are executed concurrently. Whenever the docking station is not connected, the ES978 remains in power-down mode.

The ES978 is available in an industry standard 100-pin Plastic Quad Flat Pack (PQFP) package.

FEATURES

Interfaces to ES187x *Audio***Drive® Chip**

- No bus interface required
- Simple hot-docking interface
- Supports shadowing of registers between the ES978 and ES187x
- Supports two pairs of on-chip analog differential signals for audio I/O with portable audio mixer and a 2-pin serial control bus
- High integration eliminates the need for discrete components in the docking station

Inputs and Outputs

- Supports up to 8 general-purpose inputs and 8 general-purpose outputs
- Selectable interface for either the ES689/ES69x wavetable or I²S Zoom Video
- MIDI serial port compatible with MPU-401 UART mode
- ESS high-performance digital dual game port with hardware timing

Mixer Features

- 5-channel stereo mixer: line, auxiliary A (CD audio), auxiliary B, input from ES187x portable unit, a selectable input from either the ES689/ES69x wavetable or the I²S Zoom Video, plus a mono input for a microphone
- Programmable 6-bit logarithmic master volume control
- Three-button hardware volume control with switch inputs for master volume up, down, and mute
- Symmetrical record and playback mixers for simultaneous full-duplex operation

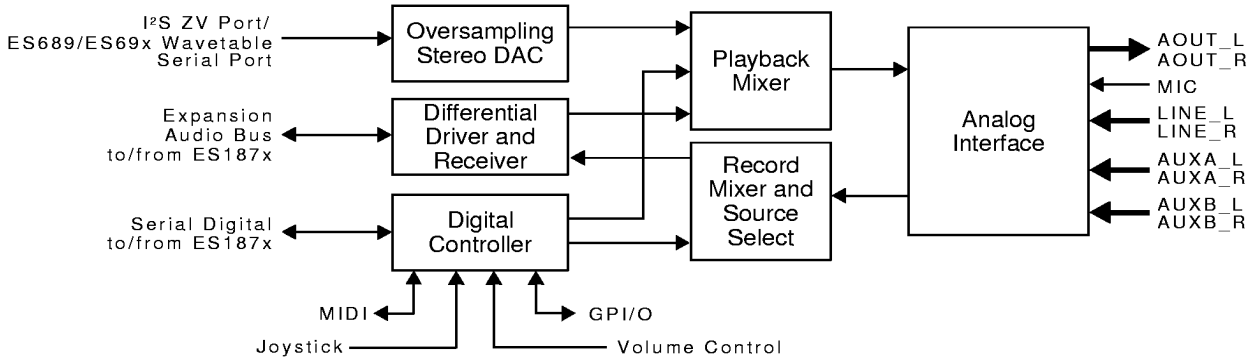


Figure 1 ES978 Simplified Block Diagram

CONTENTS

FIGURES

TABLES

PINOUT

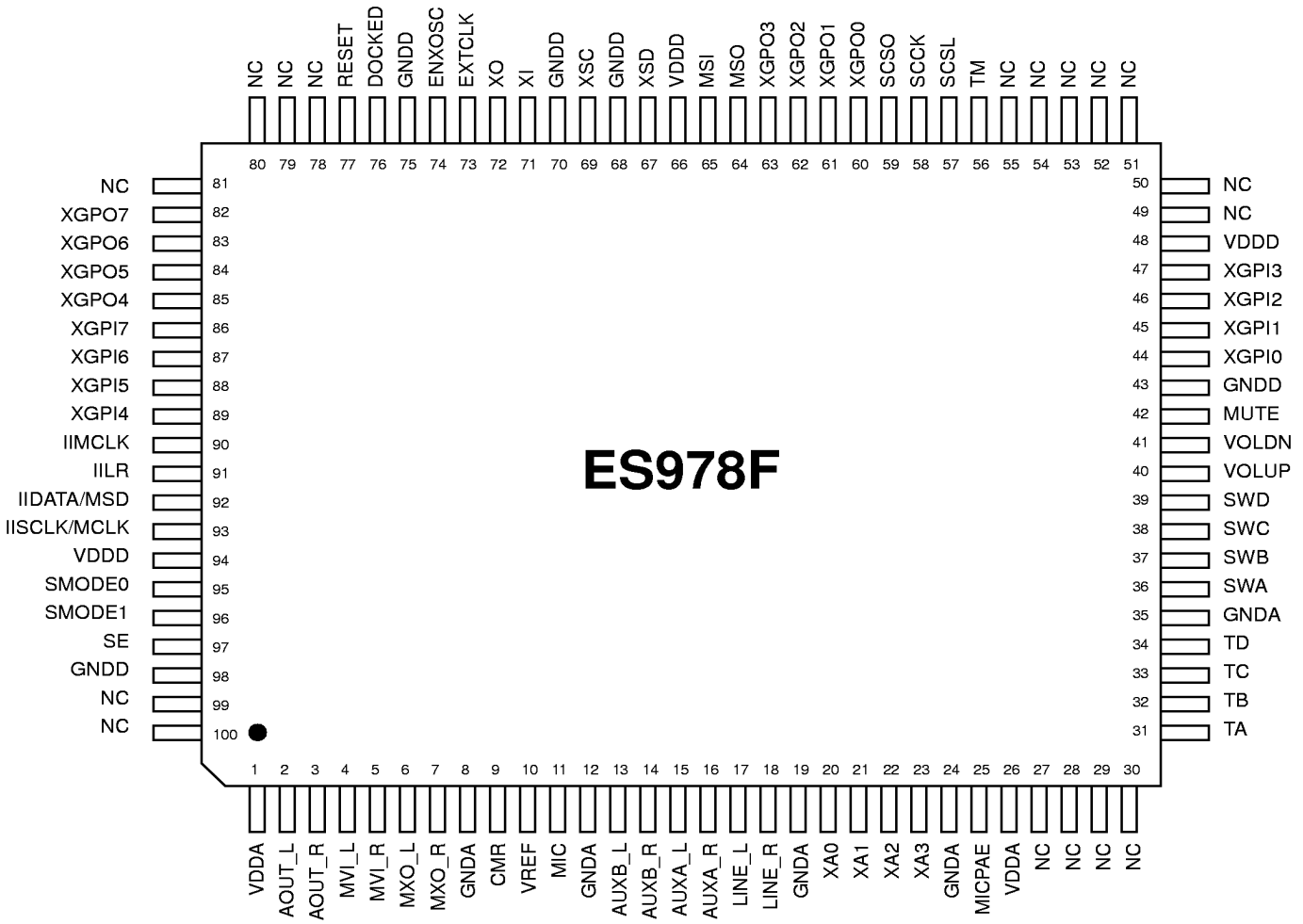


Figure 2 ES978 Pinout

PIN DESCRIPTION

Name	Number	I/O	Definition
VDDA	1, 26	I	Analog power supply, 4.75 - 5.25 V. Must be greater than or equal to (VDDD - 0.3 V).
AOUT_L	2	O	Analog output from master volume. This pin can drive a 10k ohm load.
AOUT_R	3	O	Analog output from master volume. This pin can drive a 10k ohm load.
MVI_L	4	I	Master volume input left signal. Normally coupled to MXO_L. This pin has an internal 100k ohm pull-up to CMR.
MVI_R	5	I	Master volume input right signal. Normally coupled to MXO_R. This pin has an internal 100k ohm pull-up to CMR.
MXO_L	6	O	Playback mixer output left. Normally AC-coupled to MVI_L.
MXO_R	7	O	Playback mixer output right. Normally AC-coupled to MVI_R.
GNDA	8, 12, 19, 24, 35	I	Analog ground.
CMR	9	I/O	2.25 V buffered common mode reference output.
VREF	10	I/O	2.25 V reference generator.
MIC	11	I	Mic input to +26 dB internal preamp. 50k ohm pull-up to CMR.
AUXB_L	13	I	Auxiliary B input left. 80k ohm pull-up to CMR.
AUXB_R	14	I	Auxiliary B input right. 80k ohm pull-up to CMR.
AUXA_L	15	I	Auxiliary A (CD) input left. 80k ohm pull-up to CMR.
AUXA_R	16	I	Auxiliary A (CD) input right. 80k ohm pull-up to CMR.
LINE_L	17	I	Line input left. 80k ohm pull-up to reference output buffer signal (CMR).
LINE_R	18	I	Line input right. 80k ohm pull-up to CMR.
XA[3:0]	23:20	I/O	Bidirectional differential receiver/transmitters. Expansion audio bus. These are analog signals that are DC-coupled to the corresponding XA[3:0] pins of the ES187x.
MICPAE	25	I	Microphone preamp enable signal. Connect to VDDA to enable internal preamp. Connect to GNDA to enable bypass preamp.
T(A-D)	31:34	I/O	Joystick timer inputs.
SW(A-D)	36:39	I	Joystick switch inputs. These pins have internal pull-ups to VDDD and change state based on modifications to the resistance values of the potentiometer within the joystick.
VOLUP	40	I	Active-low volume-up input transmitted to the ES187x. This pin has an internal pull-up to VDDD.
VOLDN	41	I	Active-low volume-down input transmitted to the ES187x. This pin has an internal pull-up to VDDD.
MUTE	42	I	Active-low mute input transmitted to the ES187x. This pin has an internal pull-up to VDDD.
GNDD	43, 68, 70, 75, 98	I	Digital ground.
XGPI [7:0]	86:89, 47:44	I	General-purpose inputs. These inputs can be read by the host processor or slaved to the GPO[7:0] outputs of the ES187x.
VDDD	48, 66, 94	I	Digital power supply (4.5 - 5.5 V).
TM	56	NC	Test pin; leave unconnected.
SCSL	57	NC	Test pin; leave unconnected.
SCCK	58	NC	Test pin; leave unconnected.
SCSO	59	NC	Test pin; leave unconnected.

Name	Number	I/O	Definition
XGPO [7:0]	82:85, 63:60	O	General-purpose outputs. These outputs can be written by the host processor or slaved to the GPI[7:0] inputs of the ES187x. Driven to zero during reset, or when the ES978 is undocked.
MSO	64	O	MIDI serial output.
MSI	65	I	MIDI serial input. MSI has an internal pull-up to VDDD.
XSD	67	I/O	Bidirectional expansion audio serial interface data line.
XSC	69	I	Expansion audio serial interface clock/sync. This pin has an internal pull-down to GNDD.
XI	71	I	14.31818 MHz external crystal input. This pin should be left unconnected when ENXOSC = 0.
XO	72	O	14.31818 MHz external crystal output. This pin should be left unconnected when ENXOSC = 0.
EXTCLK	73	I	This clock can be used in place of a crystal when ENXOSC = 0. This signal is driven by a 14.31818 MHz TTL level clock input .
ENXOSC	74	I	Active-high external oscillator enable signal. Connect this pin to VDDD to enable the oscillator. Connect to GNDD when using an external clock source, or to power down the oscillator.
DOCKED	76	I	Asserted-high when the ES978 is docked to the ES187x. This pin has an internal pull-down to GNDD. External logic must assure that this signal is asserted as long as the expansion unit is docked to the portable.
RESET	77	I	Active-high power-on reset. Reset should be asserted until the crystal oscillator is stable.
IIMCLK	90	I	Oversampling clock for the I²S interface. This pin has an internal pull-down to GNDD and is left unconnected in ES689/ES69x mode.
IILR	91	I	Active-high left/right channel select signal for the I²S interface. This pin has an internal pull-down to GNDD and is left unconnected in ES689/ES69x mode.
IIDATA	92	I	Dual purpose pin. IIDATA is serial data for I²S interface. This pin has an internal pull-down to GNDD.
MSD		I	MSD is serial data for the ES689/ES69x interface. This pin has an internal pull-down to GNDD.
IISCLK	93	I	Dual purpose pin. IISCLK is a serial shift clock for I²S interface. This pin has an internal pull-down to GNDD.
MCLK		I	MCLK is a serial shift clock for the ES689/ES69x interface. This pin has an internal pull-down to GNDD.
SMODE [1:0]	96:95	I	Select mode of serial port input to internal DAC:
SE	97	I	Active-high serial port enable. Connect to VDDD to enable serial port inputs to the internal DAC. This pin has an internal pull-down to GNDD.
NC	27:30, 49:55, 78:81, 99:100	NC	No connection.

SMODE		MODE
1	0	
0	0	Auto Detect Mode. The ES978 automatically detects among I²S oversampling modes: x256, x384, or x512.
0	1	I²S x256 oversampling
1	0	I²S x384 oversampling
1	1	ES689/ES69x

MIXER SCHEMATIC BLOCK DIAGRAM

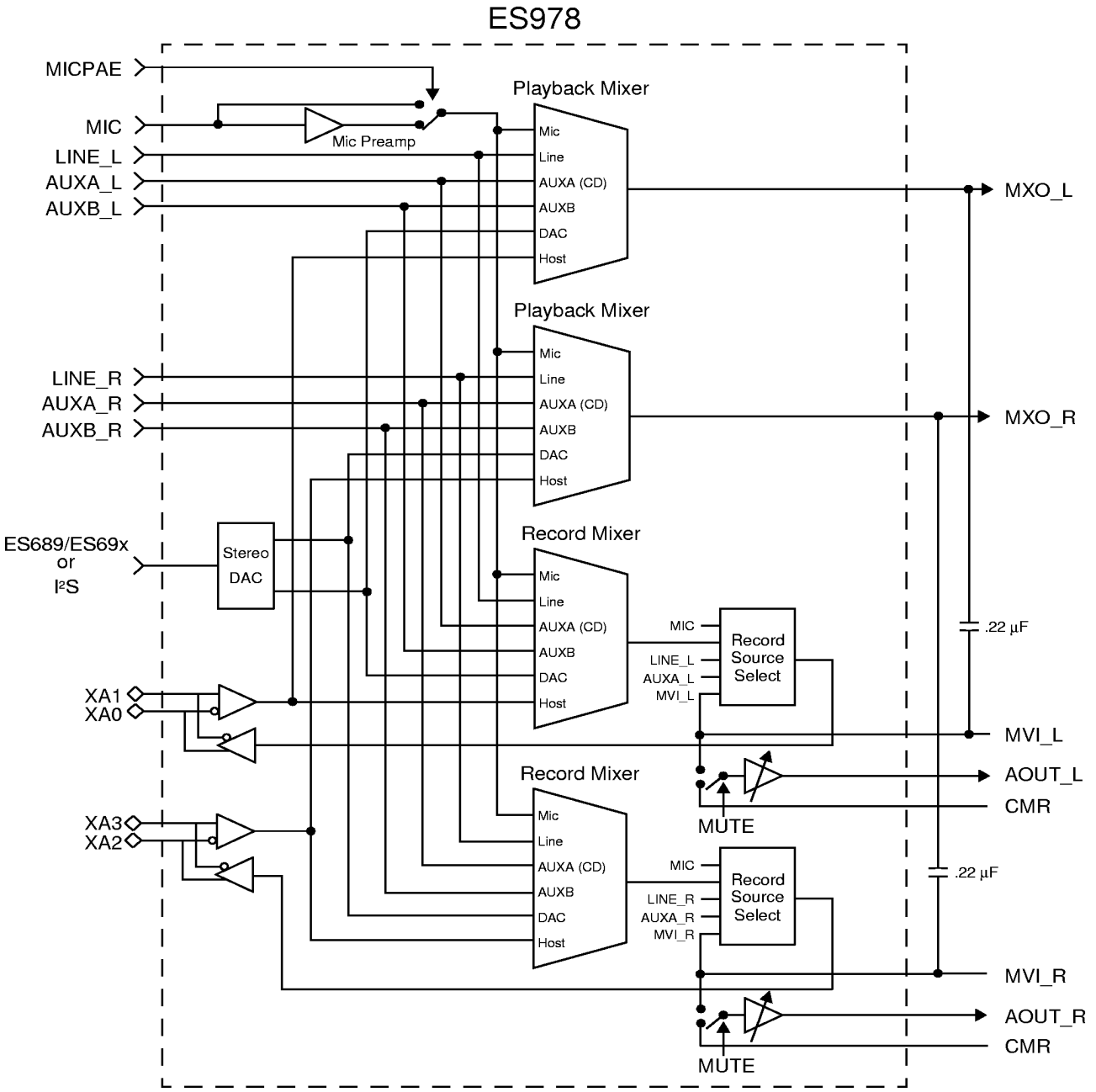


Figure 3 Mixer Schematic Block Diagram

FUNCTIONAL BLOCK DESCRIPTION

This section describes each section of the block diagram shown in Figure 1. A detailed functional block diagram is shown in Figure 3.

Oversampling Stereo DAC

The state of the SMODE[1:0] pins determines the type of input received by the oversampling stereo DAC. The DAC input can be one of two types: an I²S ZV serial port interface which supports MPEG audio, or an ES689/ ES69x wavetable interface which supports a wavetable music synthesizer.

In I²S ZV serial interface mode, MPEG audio signals are transferred from the ES187x to the ES978 at a maximum sample rate of 50 kHz.

In ES689/ES69x wavetable interface mode, the serial clock and data are generated by an ES689/ES69x wavetable music synthesizer.

Three oversampling rates are supported; x256, x384, and x512. The SMODE[1:0] configuration pins determine which interface mode and oversampling rate are being used. The x512 oversampling mode is a third choice in auto-detect mode only, and cannot be manually selected.

Differential Driver and Receiver

This block contains a 4-wire analog interface which uses the XA[3:0] pins to transfer information between the ES187x and the ES978. Analog data is transferred using one of four modes. These modes are explained further in “Expansion Audio Interface – Analog” on page 12.

Digital Controller

The Digital Controller portion of the ES978 handles the following functions:

- **ES187x Serial Digital Interface** – A 2-wire digital interface transmits serial data between the ES187x and the ES978. The XSC serial clock input handles clocking and frame synchronization, while the XSD input transfers serial data. Refer to “Expansion Audio Interface – Digital” on page 11 for more information.
- **MIDI Interface** – Two pins are reserved for Musical Instrument Digital Interface (MIDI) serial data I/O. MIDI is an asynchronous serial protocol for musical instrument interconnection which operates at 31.25 kbps. The MSI pin is the MIDI serial receive pin and has an internal pull-up resistor. MSO is the MIDI transmit pin.

  MIDI data received at the MSI pin of the ES978 is de-serialized and transmitted to the ES187x, where it is placed in the MPU-401 receive FIFO.

  The data placed in the ES187x transmit FIFO is transferred to the ES978 and subsequently transmitted onto the MSO output pin of the ES978.
- **Dual game ports and timer** – The ES978 includes eight pins for a dual joystick port. Four of these pins, SW(A-D), are inputs for the switches of the joysticks. The state of these switches is transmitted to the ES187x where they are read by the host processor.

  The remaining four pins, T(A-D), are “one-shot” digital timers that generate pulses of varying widths, where the width corresponds to the resistance of one of the joystick potentiometers. Normally, the host processor is responsible for measuring the width of the pulse. However, when docked, the ES978 performs this function automatically and reports the pulse width information to the ES187x. In this manner the ES187x is continually updated with the state of the joystick inputs.
- **Hardware Volume Control** – Three pins are used to control volume. Sound output volume is altered through use of the Volume Up (VOLUP), Volume Down (VOLDN), and MUTE pins. The state of these three input pins is continually transmitted to the ES187x where each is logically AND'ed with the three corresponding pins of the ES187x.
- **General-Purpose I/O** – The ES978 has eight outputs: XPGO[7:0]. These outputs are either written by the host processor or slaved to the GPI[7:0] inputs of the ES187x. Each output has a 4 mA drive capability and a worst case latency of 140 microseconds.

  All eight outputs are reset (driven low) by power-on reset (RESET=1) and when undocked (DOCKED=0).

  The ES978 also has eight general-purpose inputs: XPGI[7:0]. These inputs do not have pull-ups and should be pulled low or high if not used. The state of these inputs is continually transmitted to the ES187x at a worst case latency of 150 microseconds. Within the ES187x, the state of these inputs can be polled by the host processor, and optionally used to set the level of corresponding general-purpose output pins of the ES187x.

Playback Mixer

The playback mixer has six inputs. One input, host audio, is the analog data from the ES187x.

- Mic In (mono)
- Host Audio (from ES187x)
- Line In
- Aux A (CD)
- Aux B
- DAC

The DAC input is the serial interface in either I²S Zoom Video or ES689/ES69x format. The SMODE[1:0] pins select the format.

The volume registers for the six inputs are continually transmitted from the ES187x.

Record Mixer and Record Source Select

The record mixer has the same six inputs as the playback mixer. However, the Host audio input is only used for testing purposes.

The ES1878 does not support separate volume controls for the record and playback mixers so they are not truly independent. Independent record and playback mixers will be available in future generations of the ES1878 which support separate volume controls.

The recording source can be selected from one of the five choices:

- Mic
- Line
- Aux A (CD)
- Record Mixer
- Playback Mixer (not supported by the ES1878)

Analog Interface

Analog output pins AOUT_L and AOUT_R are the outputs of the master volume control and are intended to be AC-coupled to an external power amplifier to drive stereo speakers in the expansion unit. These outputs can drive a 10k ohm load and are held at approximately the CMR reference voltage with an internal high-impedance resistor divider when the ES978 is powered-down.

The analog inputs contain internal pull-up resistors to CMR of 50k ohms or more and are intended to be AC-coupled to external analog sources. There are three stereo line-level inputs: LINE, AUXA, and AUXB. There is also a monophonic microphone input.

Bypass the reference voltage (VREF) to analog ground with a .1 μF capacitor. Bypass CMR to analog ground with a 10 μF capacitor in parallel with a .1 μF capacitor.

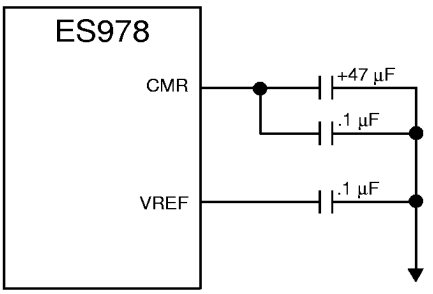


Figure 4 Reference Generator Pin Diagram

MVI_L should be AC-coupled to MXO_L. MVI_R should be AC-coupled to MXO_R. In general, all coupling capacitors should be .22 μF.

TYPICAL APPLICATION

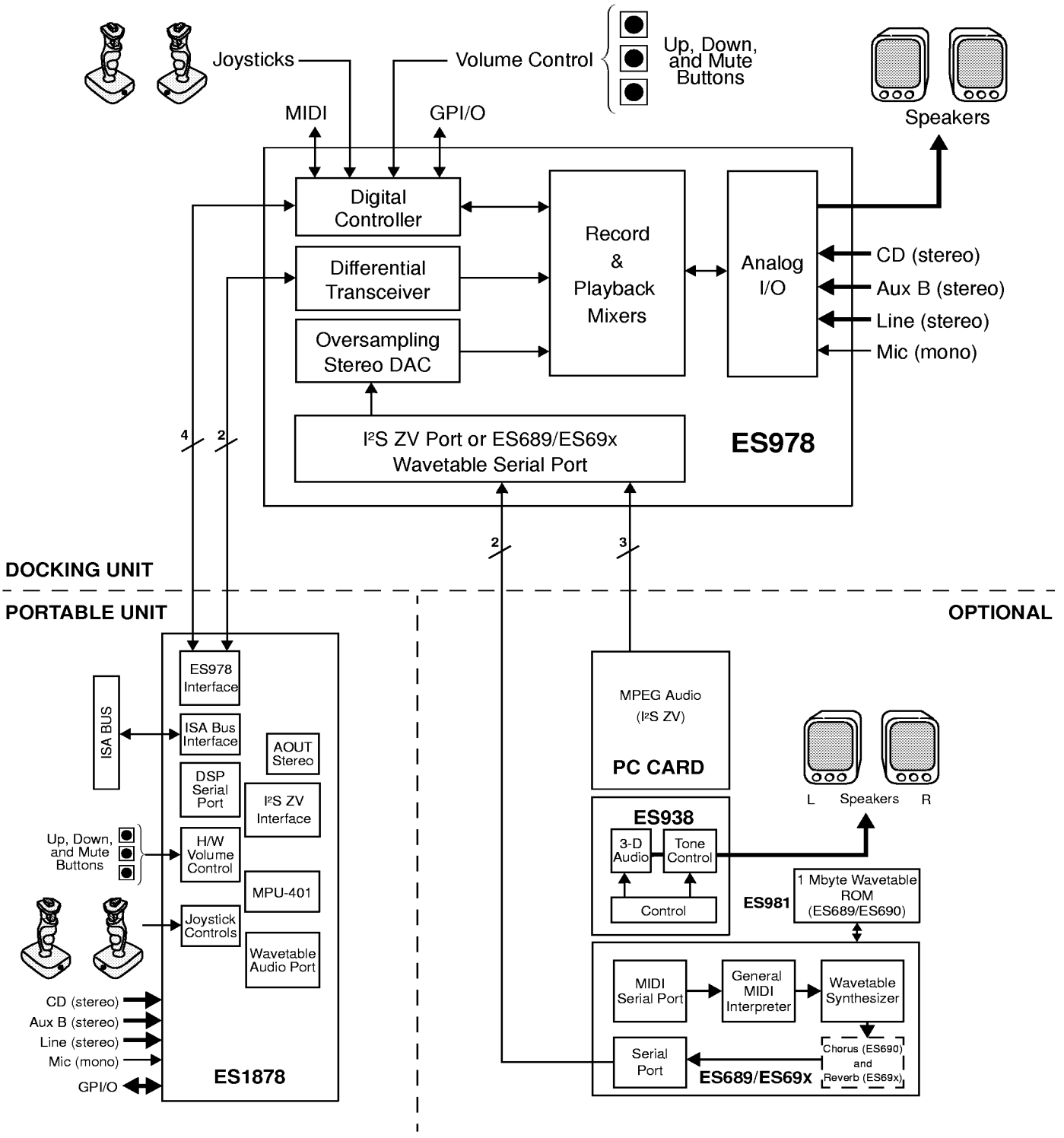


Figure 5 Typical Application

THEORY OF OPERATION

This section discusses the basic theory of operation for the ES978, including the ES187x interface, modes of operation, clock and expansion interface requirements, and power management.

Docking with the ES187x

The ES978 is a remote mixer incorporated into a docking station, also called an expansion unit. The docking station can be a module that the portable plugs into or a card containing an ES978 which is connected to the back of the portable unit. The communication between the portable and the docking station is done through a digital bus and an analog bus. When docked, both buses are connected. The assertion of the DOCKED signal indicates to each device that the other is present. The DOCKED signal is driven by external logic. This means that external logic must be able to detect when docking occurs.

When docked, the ES187x-based portable unit is in constant communication with the ES978-based docking station. A half-duplex, bidirectional serial link keeps each chip updated with the status of the other. For example, mixer registers located in the ES187x are transmitted to the ES978, whereas MIDI data received by the ES978 is transmitted to the ES187x.

Docking Status

In the docked state:

- The ES978 is powered-up.
- AOUT_L and AOUT_R are active.
- XA[3:0] are active.
- The MIDI output is active.
- All serial ports are enabled.

The docked state is determined by both of the following conditions being true:

- DOCKED input is high.
- The XSC serial clock input is running.

In the undocked state:

- The ES978 is powered-down.
- AOUT_L and AOUT_R are muted.
- XA[3:0] become inputs.
- The MIDI output is forced high.
- All serial ports are disabled.

The undocked state is determined by either of the following conditions being true:

- DOCKED input is low.
- The XSC serial clock input remains low for >128 clocks.

When changing state from undocked to docked, there is approximately a 100 millisecond period before the AOUT_L and AOUT_R outputs are enabled. During this time the internal registers are updated from the ES187x.

The 14.31818 MHz input clock (XI or EXTCLK) of the ES978 should be stable before the DOCKED input is asserted, unless RESET is also asserted.

Modes of Operation

Four analog pins are used to determine the operating mode. These four pins, XA[3:0], are configured as a pair of differential audio channels. These pins are DC-coupled to the corresponding XA[3:0] inputs on the ES187x. The ES187x uses these two audio channels in one of three ways:

1. stereo playback (the ES187x transmits to the ES978)
2. stereo record (the ES978 transmits to the ES187x)
3. mono full-duplex (one mono channel in each direction)

Playback Mode

In stereo playback mode sound data is transferred from the ES187x to the ES978, which drives the speakers in the docking station. Except when recording, expansion unit audio sources are mixed in the expansion unit within the ES978, and played through the speakers in the expansion unit. In most cases, speakers within the portable unit are programmed to be automatically muted when docked.

Each audio input can be programmed individually to respond to the docking station.

Record Mode

In record mode, sound data is transferred in the opposite direction from that in playback mode, from the ES978 to the ES187x in the portable unit. This data is then mixed with local sources by the ES187x before recording. The default for most applications is to have all speakers muted during recording.

Mono Full-Duplex Mode

In mono full-duplex mode, the record channel records from any analog input of either the ES187x or the remote ES978, any mix of the two, or from the FDXI input of the ES187x when using the serial port. The restrictions are that both record and playback are monophonic and synchronous, meaning that they have the same sample rate.

ES978 Clock Requirements

The ES978 requires a 14.32 MHz clock input which can be asynchronous with the ES187x clock. There are two ways to connect the clock in the ES978:

1. The 14.32 MHz clock input can be generated by connecting a crystal to XI and XO, connecting the ENXOSC pin high, and connecting the EXTCLK pin low. In this configuration the oscillator continues to run even when the ES978 is powered-down. The RESET pin should be driven high for 25 milliseconds or more in order for the oscillator to stabilize.
2. A TTL level clock signal is connected to EXTCLK and the ENXOSC pin is connected to ground. In this case XI and XO are left unconnected.

Expansion Audio Interface – Digital

Two pins are used to transmit serial data between the ES187x and ES978. The first signal, XSC, acts as a frame sync and shift clock. The bit clock rate is 3.58 MHz.

A typical frame consists of:

- Sync Period – 24 clocks wide
- Download Period – 144 clocks wide
- Turn-around Period – 8 clocks wide
- Upload Period – 80 clocks wide

For a total of 256 bit clocks/frame, which is equivalent to a 14 kHz frame rate.

Sync Period

In the sync period, XSC is low for 12 clocks, then high for 12 clocks.

Download Period

In the download period, data is transmitted serially from the ES187x to the ES978 through the XSD serial data signal. The XSC input functions as the bit shift clock. Data is shifted out of the ES187x on the falling edge of XSC. Data is shifted into the ES978 on the rising edge of XSC. The 144-clock period is required to shift eighteen 1-byte values as shown in Table 1.

Table 1 Download Period

Byte	Bits	Function
0	1:0 4:2 5 6 7	Mode of expansion analog interface Record source select Master output enable 1: MIDI loopback test 1: MIDI transmit signal (byte 1 contains MIDI data)
1	15:8	MIDI data (if bit 7 of byte 0 is high)
2	23:15	XGPO[7:0] data
3	31:24	Playback mixer – Host audio volume
4	39:32	Playback mixer – Line volume
5	47:40	Playback mixer – Mic volume
6	55:48	Playback mixer – Aux A (CD) volume
7	63:56	Playback mixer – Aux B volume
8	71:64	Playback mixer – I²S/ES689/ES69x volume
9	79:72	Reserved
10	87:80	Record mixer – Line volume
11	95:88	Record mixer – Mic volume
12	103:96	Record mixer – Aux A (CD) volume
13	111:104	Record mixer – Aux B volume
14	119:112	Record mixer – I²S/ES689/ES69x volume
15	126:120 127	Master volume left 1: Mute left
16	134:128 135	Master volume right 1: Mute right
17	143:136	CRC checksum

Turn-around Period

There are 8 clocks between the end of the download period and the start of the upload period.

Upload Period

In the upload period, data is transmitted serially in the opposite direction, from the ES978 to the ES187x through the XSD pin. Eighty clocks are required to serially transfer ten bytes of information. The last 8 bits are a checksum byte. Table 2 shows the type of information transferred during the upload period.

Table 2 Upload Period

Byte	Bits	Function
0	3:0 4 5 6 7	Joystick switch status VOLUP input status VOLDN input status MUTE input status 1: MIDI receive data following
1	15:8	MIDI receive data if bit 7 of byte 0 is set.
2	23:16	XGPI input state
3	31:24	Low byte joystick timer A
4	39:32	Low byte joystick timer B
5	47:40	Low byte joystick timer C
6	55:48	Low byte joystick timer D
7	59:56 63:60	High nibble joystick timer A High nibble joystick timer B
8	67:64 71:68	High nibble joystick timer C High nibble joystick timer D
9	79:72	CRC checksum

Together, the upload and download periods serve to continually update corresponding registers within each device. For example, pressing the VOLUP button in the expansion unit transmits the pin state to the ES187x where it is logically AND'ed with the same pin of the ES187x. The ES187x updates its copy of the master volume register. The ES978 will receive the new value along with the next download period of the next frame.

Expansion Audio Interface – Analog

Four analog pins, XA[3:0], define the expansion analog audio interface: These four signal pins can be used in one of five different modes. In each of these modes, the master always refers to the ES187x and the slave always refers to the ES978. The ES187x determines the current mode based on whether it is playing, recording, or using full-duplex mode.

- Mode 0 – Stereo Playback. Two differential pairs for left and right channels, transmitted from the master to the slave.
- Mode 1 – Stereo Record. Two differential pairs for left and right channels, transmitted from the slave to the master.
- Mode 2 – Monophonic Full-Duplex defines two differential pairs. One pair is for monophonic playback from master to slave, the second pair is for monophonic recording from slave to master. The mono playback signal is input to both the left and right host audio inputs of the playback mixer. The mono record signal is derived by averaging the left and right outputs of the record mixer.
- Mode 3 – Stereo Full-Duplex. The four signals are not used differentially (note that this mode is not supported by the ES187x).
- Mode 4 – Not Docked (DOCKED=0). Like MODE 0 except the analog outputs follow AOUT_L and AOUT_R rather than the output of the mixer.

After a mode change, the outputs are muted for about 50 milliseconds. Table 3 shows how XA[3:0] are used in each mode.

Table 3 Expansion Audio Interface Using XA[3:0]

Mode	XA0	XA1	XA2	XA3
0	-Left Play	+Left Play	-Right Play	+Right Play
1	+Left Record	-Left Record	+Right Record	-Right Record
2	-Play	+Play	+Record	-Record
3	Left Record	Left Play	Right Record	Right Play

I²S Serial Interface

The I²S serial interface in the ES978 is easily implemented. Three input pins shown in Figure 6, IIDATA, IISCLK, and IILR, are used for a serial interface between an external device and a stereo DAC within the ES187x. A fourth input, IIMCLK, is reserved for future devices that incorporate oversampling and should be left floating or connected to ground. IIDATA, IISCLK, and IILR can be left floating or connected to ground if the serial interface is not used.

Typical applications of the I²S serial interface are MPEG audio, or an ES689/ES69x wavetable synthesizer.

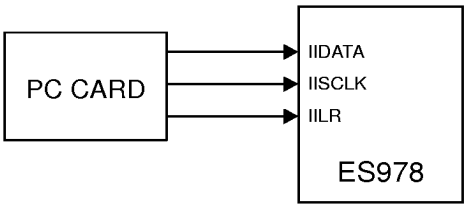


Figure 6 I²S Implementation in ES978

I²S Serial Interface Format Select

The serial interface is called the I²S interface, which supports two different formats: ES689/ES69x two-wire serial interface, or I²S. These formats can be configured by SMODE[1:0] pin selection:

SMODE		MODE
1	0	
0	0	Auto Detect Mode. The ES978 automatically detects among I²S oversampling modes: x256, x384, or x512.
0	1	I²S x256 oversampling
1	0	I²S x384 oversampling
1	1	ES689/ES69x

See also the ES1878 or ES1879 Data Sheets for detailed information on I²S implementation. When used in the ES689/ES69x format, MSD is the serial data and MCLK is the bit clock. The IILR input is not used and can be left floating or connected to ground.

I²S Serial Interface Timing

This section discusses the I²S serial interface signals. The signals when the port is configured for use with an ES689/ES69x wavetable synthesizer is defined in the Wavetable Interface section. Table 4 shows the three signals used for I²S and the fourth optional/reserved I²S pin.

Table 4 I²S Interface Pins

Pins	Descriptions
IISCLK *	The bit clock/shift clock. The maximum rate is 6.4 MHz. The minimum number of IISCLK periods per IILR period is 32. Any number greater than or equal to 32 is acceptable.
IILR	Sample synchronization signal. The maximum sample rate is 50 kHz.
IIDATA *	Serial data.
IIMCLK	Optional oversampling clock (reserved for future use).

* These pins are shared with other functions.

Within the ES187x, IILR and IIDATA are sampled on the rising edge of IISCLK. See Figure 7 and Figure 8 for detailed I²S timing.

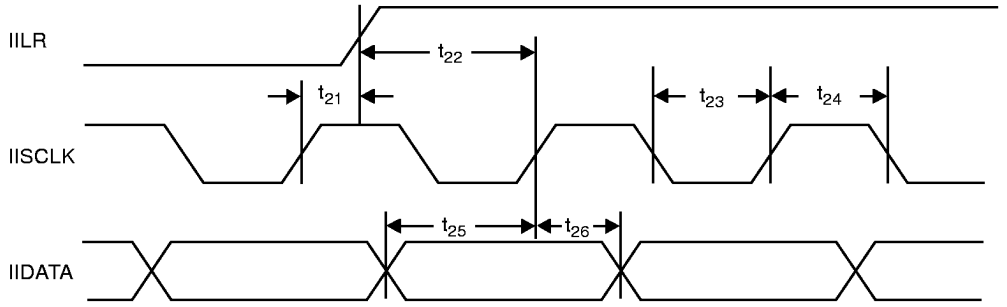
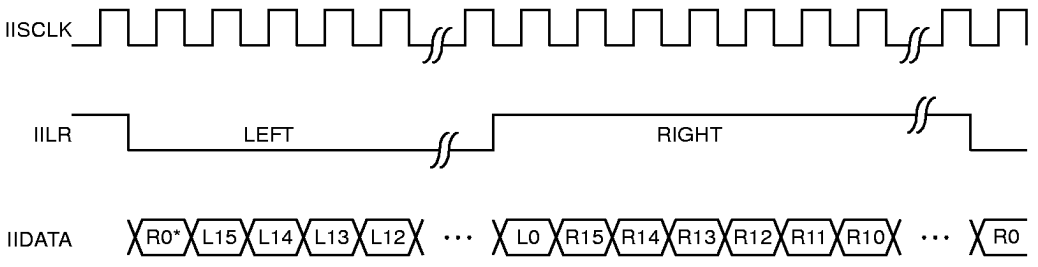


Figure 7 Serial Input Timing for I²S Interface



* Note: LSB of right channel, previous sample.

Figure 8 I²S Digital Input Format with 16 SCLK Periods

MPU-401 Interface

The MPU-401 port can interface with either MIDI or with ES938 3-D stereo sound effects signals. Refer to the ES938 Data Sheet for technical details on 3-D audio.

MIDI

The ES978 in the docking unit serializes MIDI output (MSO) obtained from the ES187x in the portable unit.

MIDI data can be received from either the MSI pin of the ES978 or from the MSI pin of the ES187x in the portable unit. In the unlikely event that MIDI data is received from both sources simultaneously, the data might be corrupted. Data received by the ES978 is transmitted back to the ES187x in the next upload frame and then placed in the MPU-401 receive FIFO.

Wavetable Interface

The ES978 contains a synchronous serial interface for connection to a wavetable music synthesizer.

Table 5 Wavetable Interface Pins

Pins	Descriptions
MCLK *	Serial clock from external ES689/ES69x music synthesizer (2.75 MHz). Input with pull-down.
MSD *	Serial data from external ES689/ES69x music synthesizer. When both MCLK and MSD are active, the stereo DACs normally used by the FM synthesizer are acquired for use by the external ES689/ES69x. The normal FM output is blocked. Input with pull-down.

* These pins are shared with other functions.

Game/Joystick Interface

The ES978 includes 8 pins for a dual joystick port. The digital game port address is decoded for timer pins TA, TB, TC, and TD, and for switch pins SWA, SWB, SWC, and SWD. The MIDI serial input and output also come from the game port connector in most applications.

Four of these eight pins, SW(A-D), are inputs for the switches of the joysticks. The remaining 4 pins, T(A-D), are “one-shot” timers that generate pulses of varying widths, where the width corresponds to the current resistance of one of the joystick potentiometers.

Normally, the host processor is responsible for measuring the width of the pulse. The ES187x in the portable unit can also do this automatically. The host processor reads the measured widths directly rather than having to do the timing itself. This is referred to as a “digital joystick.” In the ES187x, bit 1 of Vendor-Defined Card-Level register 29h determines whether the joystick port is a digital or analog joystick.

For digital joysticks, the host processor first writes any value to the joystick port, and then reads back seven separate values:

Table 6 Digital Joystick Read Values

Read #1	Low byte timer A
Read #2	Low byte timer B
Read #3	Low byte timer C
Read #4	Low byte timer D
Read #5	Bits 3:0 – Upper nibble timer A Bits 7:4 – Upper nibble timer B
Read #6	Bits 3:0 – Upper nibble timer C Bits 7:4 – Upper nibble timer D
Read #7	Bit 0 – switch A Bit 1 – switch B Bit 2 – switch C Bit 3 – switch D

The timer values reported range from 0 to FFFh (0-4095). The timer clock is 895 kHz.

When docked, a software programmable bit in the ES187x (bit 0 of Vendor-Defined Card-Level register 29h) causes the joystick connected to the ES978 to replace the one connected to the ES187x automatically.

Joystick/MIDI External Interface Connector

The joystick portion of the ES978 reference design is identical to that on a standard PC game control adaptor or game port. The PC-compatible joystick can be connected to a 15-pin D-sub connector. It supports all standard PC joystick compatible software.

If you need to support two joysticks, a joystick conversion cable is required. This cable uses a 15-pin D-sub male connector on one end and two 15-pin D-sub female connectors on the other end. All signals on this cable have direct pin-to-pin connection, except for pins 12 and 15. On the male connector, leave pins 12 and 15 without connection. On the female connector, connect pin 15 internally to pin 8, and connect pin 12 internally to pin 4. The dual joystick and MIDI port take up only one slot in your PC, leaving room for other cards. The dual joystick/ MIDI connector configuration is shown in Figure 9.

The MIDI Serial Interface Adaptor from the Joystick/MIDI connector is shown in Figure 10.

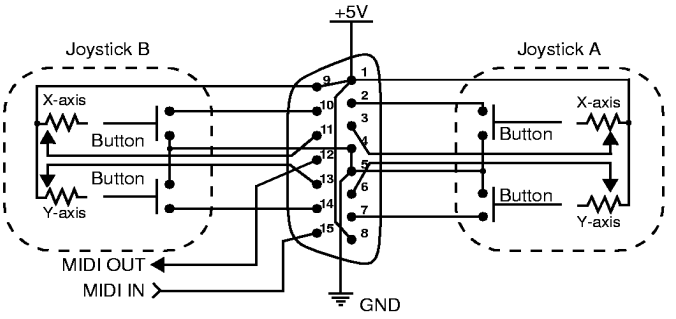


Figure 9 Dual Joystick/MIDI Connector

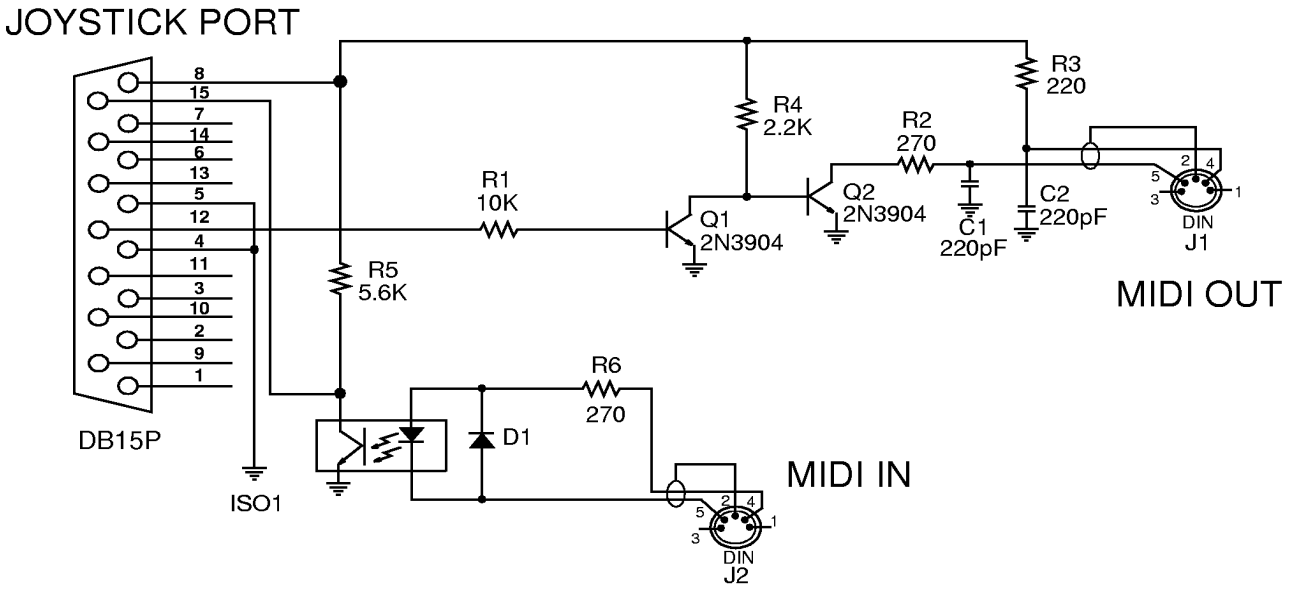


Figure 10 MIDI Serial Interface

Power Management

The ES978 is automatically powered-down when in the undocked state. It can also be powered down when docked if the clock input is suspended.

When powered-down, the analog outputs AOUT_L and AOUT_R are held at the reference voltage by high value resistor dividers. The XA[3:0] pins become inputs. The serial ports are disabled.

The ES187x is automatically powered up when the chip goes from an undocked state to a docked state. The clock inputs of both devices should be stable before the DOCKED input is asserted.

The crystal oscillator, consisting of the XI and XO pins, is powered-up and enabled whenever the ENXOSC input is high. To power down the crystal oscillator it is necessary to drive this input pin low.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Analog supply voltage	VDDA	-0.3 to 7.0	V
Digital supply voltage	VDDD	-0.3 to 7.0	V
Input voltage	VIN	-0.3 to 7.0	V
Operating temperature range	TA	0 to 70	Deg C
Storage temperature range	TSTG	-50 to 125	Deg C

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Thermal Characteristics

The ES978 was designed to operate at case temperatures between 0°C and +78°C.

Operating Conditions

The ES978 digital and analog characteristics operate under the following conditions:

VDDD	4.5 V to 5.5 V (5 volts ± 10%)
VDDA	4.75 V to 5.25 V (5 volts ± 5%)
TA	25 ° C

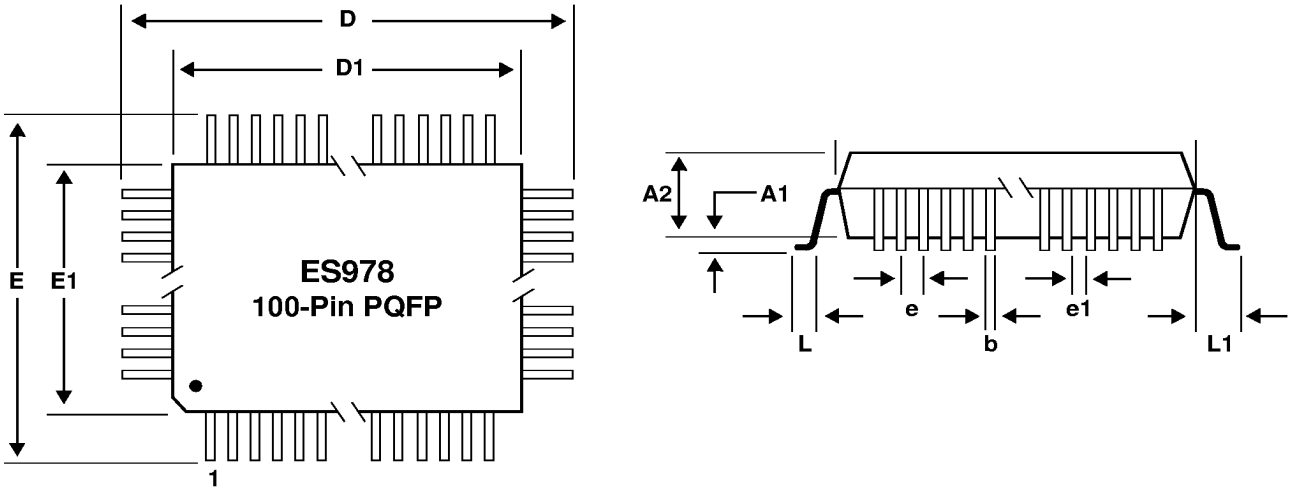
Table 7 Digital Characteristics

Parameter	Symbol	Min	Typ	Max	Unit (conditions)
Input high voltage: all inputs except XI	VIH1	2.0			volts (VDDD = min)
Input high voltage: XI	VIH2	3.0			volts (VDDD = min)
Input low voltage	VIL			0.8	volts (VDDD = max)
Output low voltage: all outputs except XSD	VOL1			0.4	volts (IOL = 4 mA, VDDD = min)
Output high voltage: all outputs except XSD	VOH1	2.4			volts (IOH = -3 mA, VDDD = max)
Output low voltage: XSD	VOL2			0.4	volts (IOL = 16 mA, VDDD = min)
Output high voltage: XSD	VOH2	2.4			volts (IOH = -12 mA, VDDD = max)
VDDD active	ICC1			10	milliamps (VDDD = 5 V)
VDDA active	ICC2			40	milliamps (VDDA = 5 V)
VDDD power-down	ICC3			50	microamps (ENXOSC = 0, all inputs static)
VDDA power-down	ICC4			50	microamps (IOH = -12 mA, VDDD = max)

Table 8 Analog Characteristics

Parameter	Pins	Min	Typ	Max	Unit (conditions)
Reference voltage	CMR, VREF		2.25		volts
Input Impedance	LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R	50k	80k	110k	ohms
	MIC	30k	50k	80k	ohms
	MVI_L, MVI_R	70k	100k	130k	ohms
Output impedance	AOUT_L, AOUT_R max load for full-scale output range		10k		ohms
Input voltage range	MIC	10		125	mVp-p
	LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R	0.5		VDDA-1.0	volts
Output voltage range	AOUT_L, AOUT_R full-scale output range	0.5		VDDA-1.0	volts
Mic preamp gain	MIC preamp		26		decibels

MECHANICAL DIMENSIONS

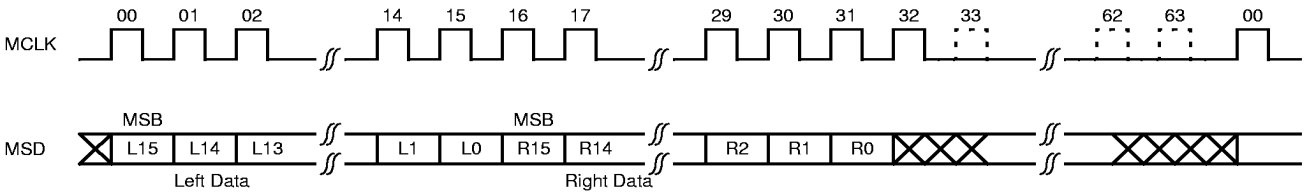


Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	23.65	23.90	24.15
D1	Package's outside, X-axis	19.90	20.00	20.10
E	Lead to lead, Y-axis	17.65	17.90	18.15
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.10	0.25	0.36
A2	Package thickness	2.57	2.71	2.87
b	Lead width	0.20	0.30	0.40
e	Lead pitch	-	0.65	-
e1	Lead gap	0.24	-	-
L	Foot length	0.65	0.80	0.95
L1	Lead length	1.88	1.95	2.02
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	30	-
-	Leads in Y-axis	-	20	-
-	Total leads	-	100	-
-	Package type	-	PQFP	-

Figure 11 Mechanical Dimensions

APPENDIX A: ES689/ES69x DIGITAL SERIAL INTERFACE

In order for the ES689/ES69x to interface with the ES978, both pins 96 and 95, SMODE[1:0], must be set high to select the wavetable mode (see table below). See the ES187x Data Sheet for further information on implementation.



Bit Clock Rate (MCLK): 2.75 MHz
Sample Rate: 42,968.75 Hz
MCLK Clocks per Sample: 33 clocks (+ 31 missing clocks)
MSD Format: 16 bits, unsigned (offset 8000h), MSB first

MSD changes after rising edge of MCLK. Hold time relative to MCLK rising edge is 0-25 nanoseconds.

SMODE		MODE
1	0	
0	0	Auto Detect Mode. The ES978 automatically detects among I²S oversampling modes: x256, x384, or x512.
0	1	I²S x256 oversampling
1	0	I²S x384 oversampling
1	1	ES689/ES69x

APPENDIX B: I²S ZV INTERFACE REFERENCE

(Excerpted from "PCMCIA Document Number 0135 – Release 010 1/15/96")

Overview

The following diagram shows the system level concept of the ZV Port. The diagram demonstrates how TV in a window could be achieved in a portable computer with a low cost PC Card. An MPEG or teleconferencing card could also be plugged into the PC Card slot.

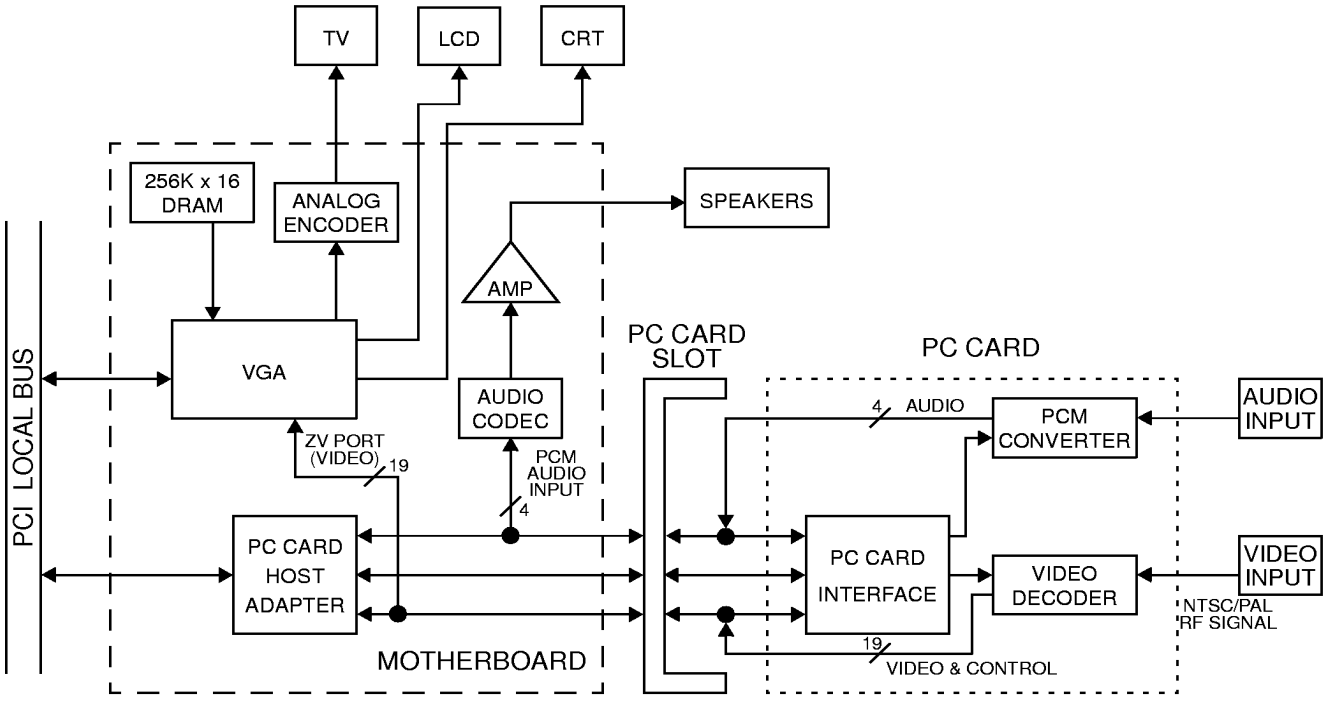


Figure 12 Example ZV Port Implementation

The Audio Interface

The ZV Port compliant PC Card sends audio data to the host computer using Pulse Code Modulation (PCM). The audio data is transferred using the serial I²S format. The audio circuitry in the host system is primarily a PCM DAC.

The PCM audio DAC is a complete stereo digital-to-analog system including digital-interpolation, delta-sigma digital-to-analog conversion, digital de-emphasis and analog filtering. Only the normal power supply decoupling components and one resistor and capacitor per channel for analog signal reconstruction are required.

The DAC accepts data at standard audio frequencies including 48 kHz, 44.1 kHz, 32 kHz, and 22 kHz. Audio data is input via the serial data input pin, SDATA. The Left/Right Clock (LRCLK) defines the channel and delineation of data. The Serial Clock (SCLK) clocks the audio data into the input data buffer. The Master Clock (MCLK) is used to operate the digital interpolation filter and the delta-sigma modulator.

Table 9 Common Clock Frequencies

LRCLK (kHz)	MCLK(MHz)	
	256x	384x
22	5.632	8.448
32	8.192	12.2880
44.1	11.2896	16.9344
48	12.2880	18.4320

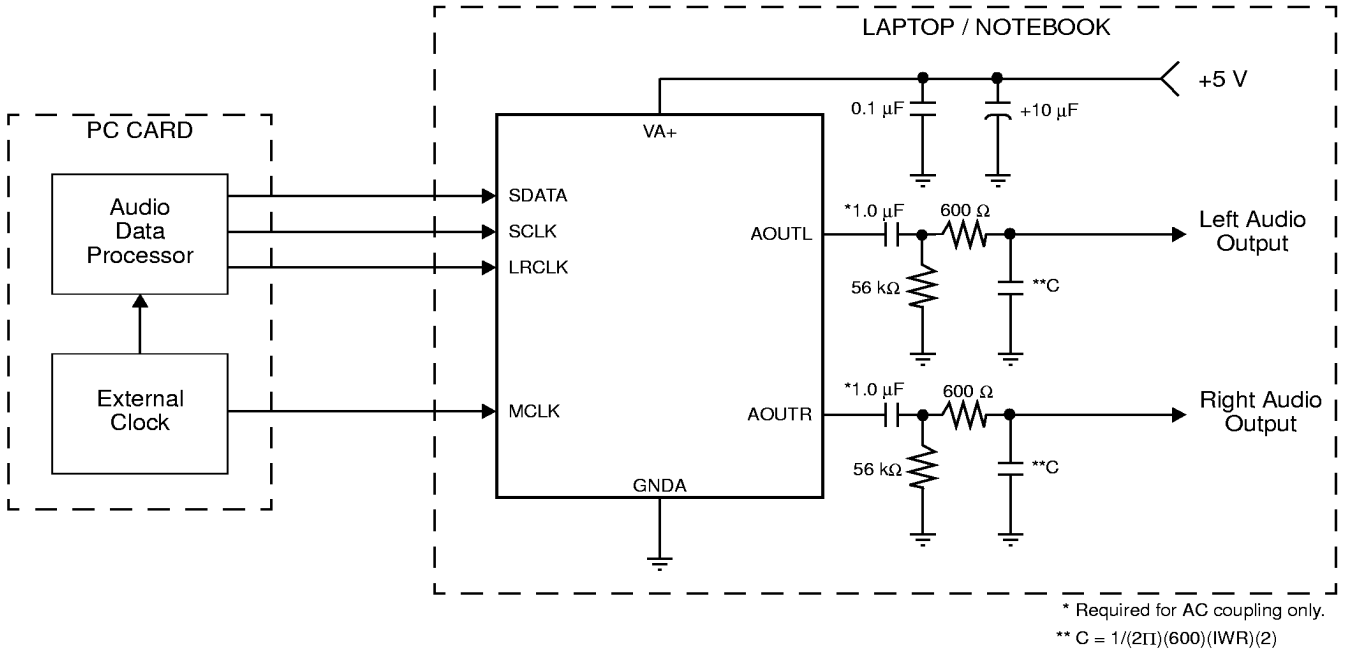


Figure 13 Typical ZV Port Audio Implementation

Audio Interface Timing

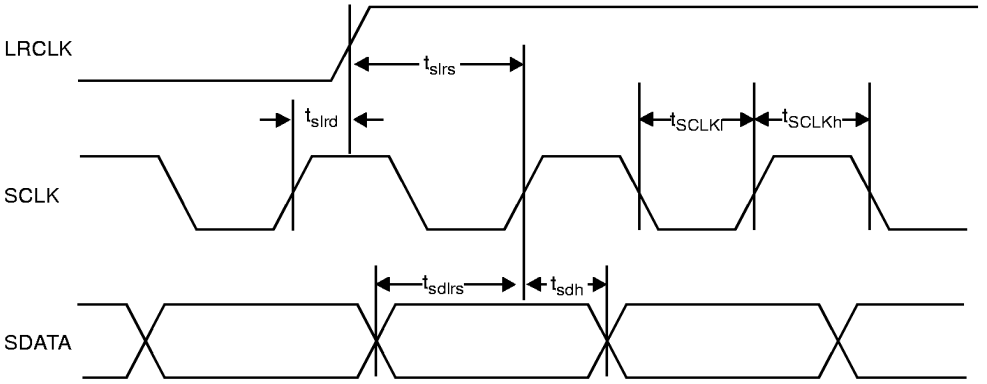


Figure 14 Audio Interface Timing

Table 10 AC Parameters for Audio Signals

Symbol	Parameter	Min
t_{slrd}	LRCLK delay	2 ns
t_{slrs}	LRCLK setup	32 ns
t_{SCLKl}	bit clock low	22 ns
t_{SCLKh}	bit clock high	22 ns
t_{sdlrs}	data setup	32 ns
t_{sdh}	data hold	2 ns

LRCLK

This signal determines which audio channel (left/right) is currently being input on the audio Serial Data input line. LRCLK is low to indicate the left channel and high to indicate the right channel. Typical frequency values for this signal are 48 kHz, 44.1 kHz, 32 kHz, and 22 kHz.

SCLK

This signal is the serial digital audio PCM clock.

SDATA

This signal is the digital PCM signal that carries the audio information. Digital audio data is transferred using the I²S format.

MCLK

This signal is the Master clock for the digital audio. MCLK is asynchronous to LRCLK, SDATA, and SCLK.

The MCLK must be either 256x or 384x the desired Input Word Rate (IWR). IWR is the frequency at which words for each channel are input to the DAC and is equal to the LRCLK frequency. The following table illustrates several standard audio word rates and the required MCLK and LRCLK frequencies. Typically, most devices operate with 384 Fs master clock.

The ZV Port audio DAC should support a MCLK frequency of 384 Fs. This results in the frequencies shown below.

LRCLK (kHz) Sample Frequency	SCLK (MHz) 32 x Fs	MCLK (MHz) 384x Fs
22	0.704	8.448
32	1.0240	12.2880
44.1	1.4112	16.9344
48	1.5360	18.4320

I²S Format

The I²S format is shown in Figure 15 below. The digital audio data is left channel-MSB justified to the high-to-low going edge of the LRCLK plus one SCLK delay.

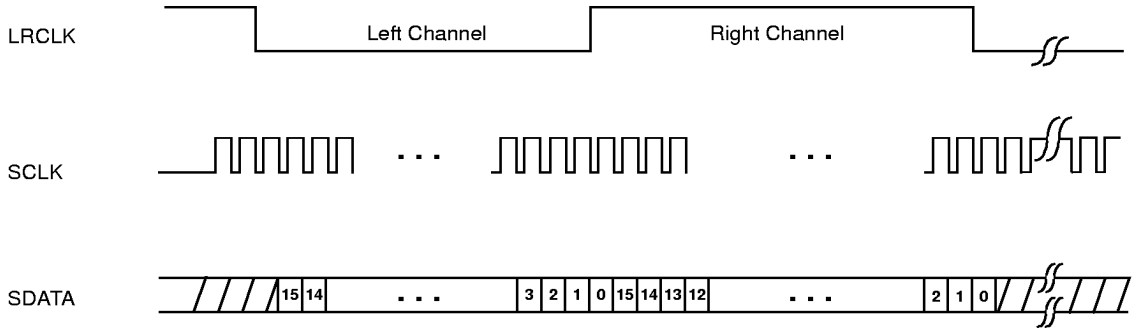


Figure 15 I²S Digital Input Format with 16 SCLK periods

ZV Port Pin Assignments

Table 11 shows the function of various PC Card signals when the ZV Port custom interface mode is set in the PC Card Host Adapter. PC Card signals not mentioned in the table below remain unchanged from the 16-bit PC Card I/O and Memory interface.

Table 11 ZV Port Interface Pin Assignments

PC Card Pin Number	I/O and Memory Interface Signal Name	I/O and Memory I/O[a]	ZV Port Interface Signal Name	ZV Port I/O[a]	Comments
8	A10	I	HREF	O	Horizontal Sync to ZV Port
10	A11	I	VSYNC	O	Vertical Sync to ZV Port
11	A9	I	Y0	O	Video Data to ZV Port YUV:4:2:2 format
12	A8	I	Y2	O	Video Data to ZV Port YUV:4:2:2 format
13	A13	I	Y4	O	Video Data to ZV Port YUV:4:2:2 format
14	A14	I	Y6	O	Video Data to ZV Port YUV:4:2:2 format
19	A16	I	UV2	O	Video Data to ZV Port YUV:4:2:2 format
20	A15	I	UV4	O	Video Data to ZV Port YUV:4:2:2 format
21	A12	I	UV6	O	Video Data to ZV Port YUV:4:2:2 format
22	A7	I	SCLK	O	Audio SCLK PCM Signal
23	A6	I	MCLK	O	Audio MCLK PCM Signal
24:25	A[5:4]	I	RESERVED	RFU	Put in three state by Host Adapter No connection in PC Card
26:29	A[3:0]	I	ADDRESS[3:0]	I	Used for accessing PC Card
33	IOIS16#	O	PCLK	O	Pixel Clock to ZV Port
46	A17	I	Y1	O	Video Data to ZV Port YUV:4:2:2 format
47	A18	I	Y3	O	Video Data to ZV Port YUV:4:2:2 format
48	A19	I	Y5	O	Video Data to ZV Port YUV:4:2:2 format
49	A20	I	Y7	O	Video Data to ZV Port YUV:4:2:2 format
50	A21	I	UV0	O	Video Data to ZV Port YUV:4:2:2 format
53	A22	I	UV1	O	Video Data to ZV Port YUV:4:2:2 format
54	A23	I	UV3	O	Video Data to ZV Port YUV:4:2:2 format
55	A24	I	UV5	O	Video Data to ZV Port YUV:4:2:2 format
56	A25	I	UV7	O	Video Data to ZV Port YUV:4:2:2 format
60	INPACK#	O	LRCLK	O	Audio LRCLK PCM Signal
62	SPKR#	O	SDATA	O	Audio PCM Data Signal

a. “I” indicates signal is input to PC Card, “O” indicates signal is output from PC Card

APPENDIX C: SCHEMATIC EXAMPLES

(With optional I²S Zoom Video Interface)

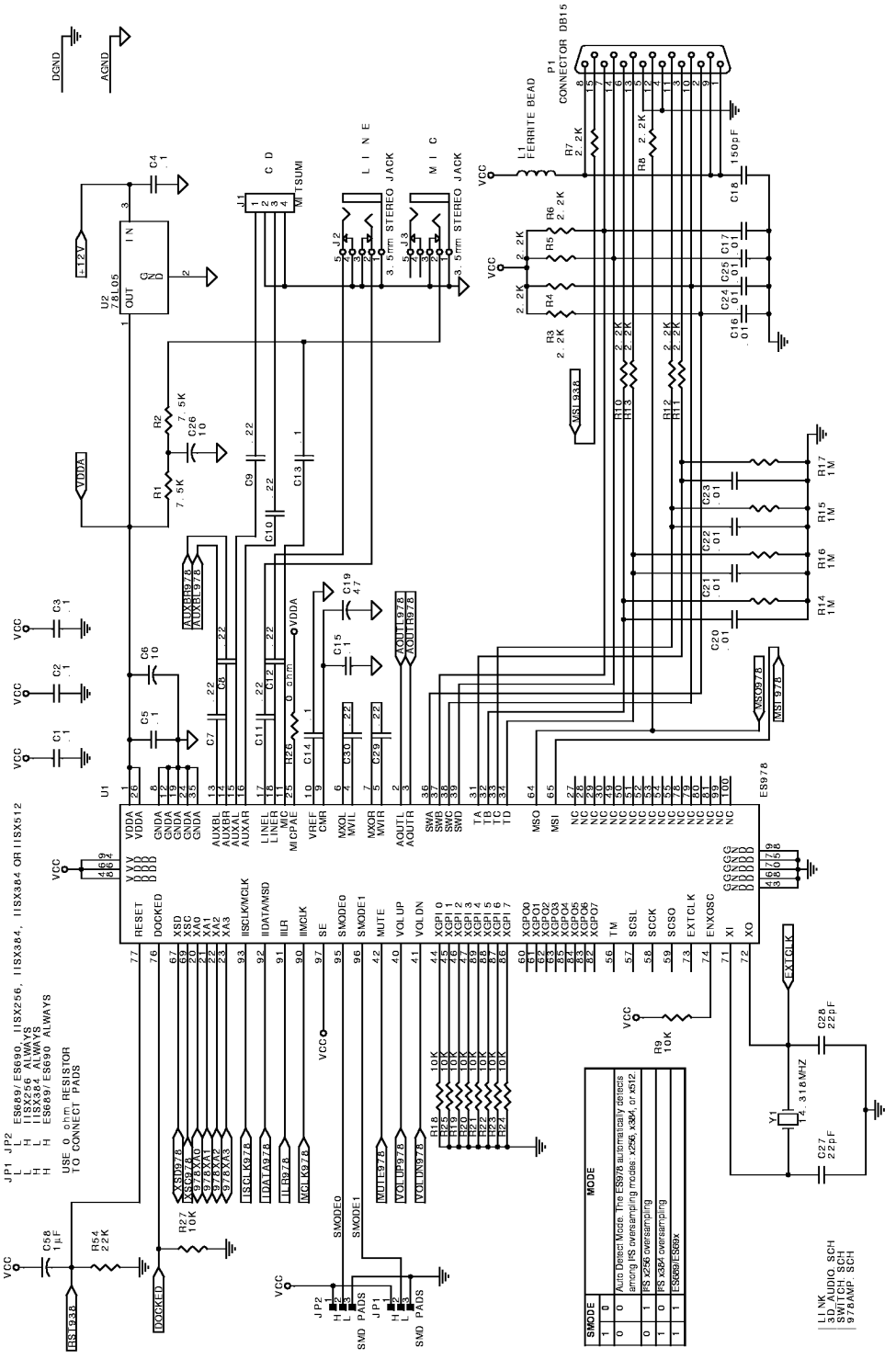


Figure 16 ES978 Schematic

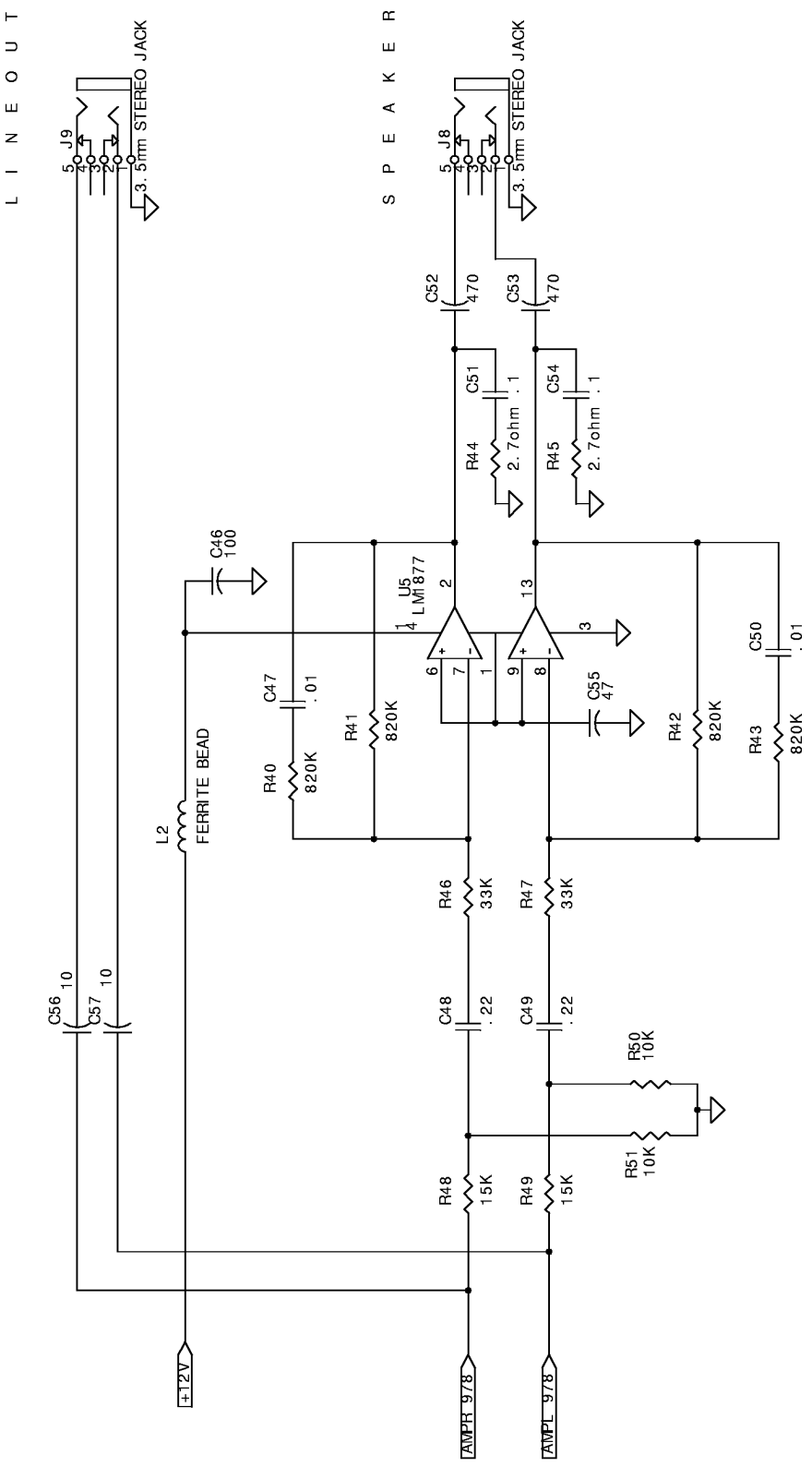


Figure 17 Amplifier Section

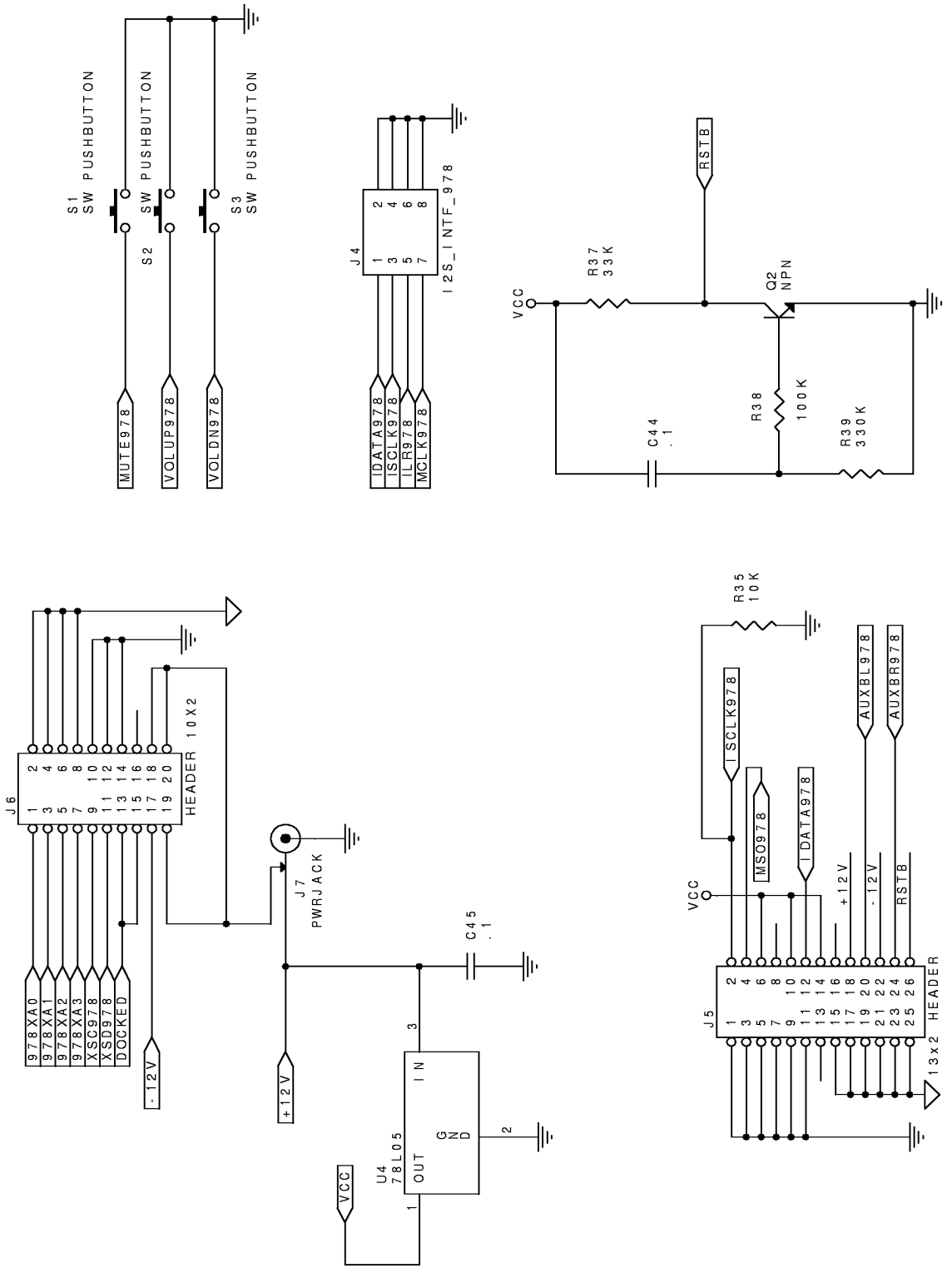


Figure 18 Switch and Connector Section

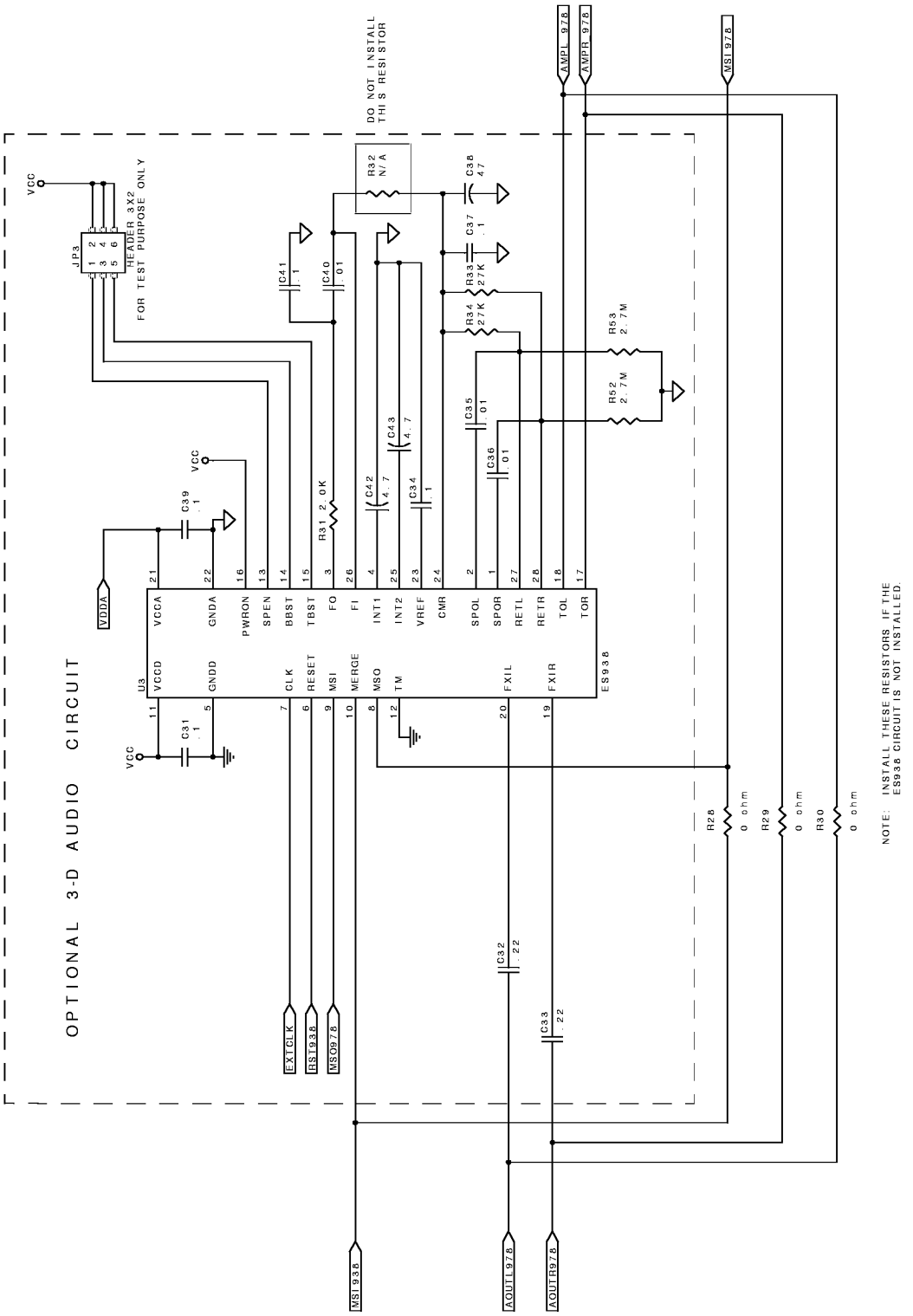


Figure 19 Optional ES938 3-D Audio Circuit

APPENDIX D: LAYOUT GUIDELINES

PCB Layout

Notebook, Motherboard, Pen-based, and PDA portable computers have the following similarity in PCB layout design:

1. Multi-layer (usually 4 to 8 layer).
2. Double-sided SMT.
3. CPU, corelogic (chip set), system memory, VGA controller, and video memory reside in the same PCB.

This is a very noisy environment for adding an audio circuit. The following are the guidelines for PCB layout for ESS *Audio***Drive®** chip application.

Component Placement

The audio circuit-related components must be grouped in the same area. The audio I/O jack and connector are considered audio-related components as well.

There are two possible placements for these audio components:

A grouped on one side of the PCB.

B separated on both sides of the PCB.

In Case B, audio component grouping will take less space.

Analog Ground Plane

Audio circuits require two layers of analog ground planes for use as shielding for all analog traces.

In component placement case A (Figure 20), the first layer of analog ground plane is on the analog component side, the second analog ground plane is on the inner layer, and the analog traces are embedded between these two planes.

In component placement case B (Figure 21), the analog ground planes are on both sides of the PCB, with the analog traces shielded in the middle.

Case A:

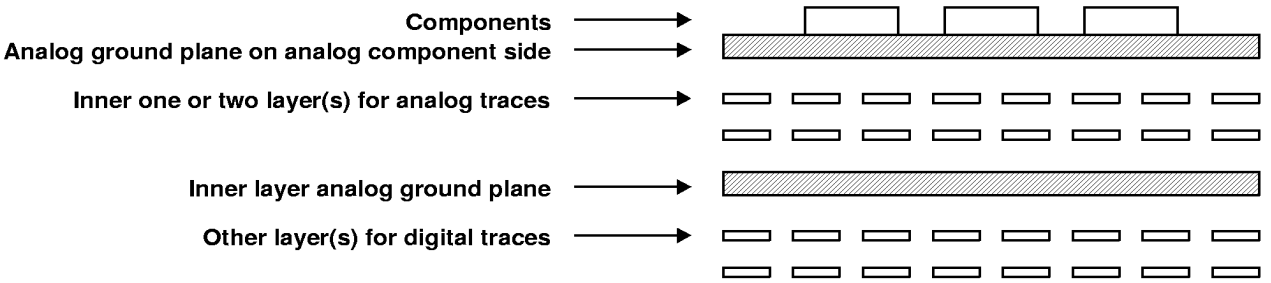


Figure 20 Analog Components on One Side of the PCB

Case B:

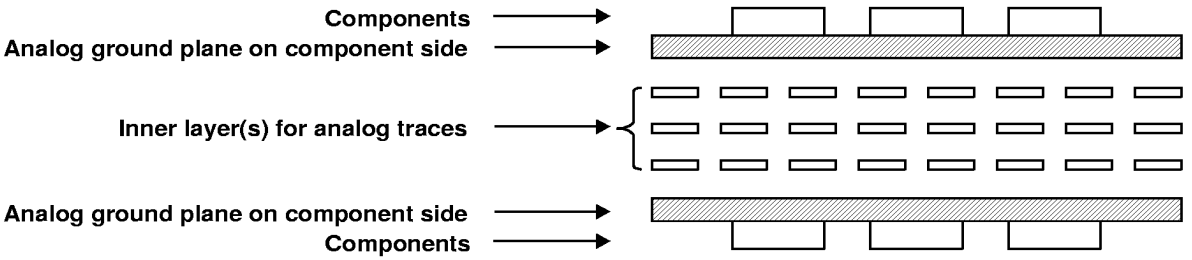


Figure 21 Analog Components on Both Sides of the PCB.

Special Notes

The analog traces should be places as short as possible.

The MIC-IN circuit is the most sensitive of the audio circuits, and requires proper and complete shielding.

APPENDIX E: ES978 BILL OF MATERIALS

Table 12 ES978 with ES938 Bill of Materials (BOM)

Item	Quantity	Reference	Part
1	17	C1,C2,C3,C4,C5,C13,C14,C15,C31,C34,C37,C39,C41,C44,C45,C51,C54	.1 µF
2	4	C6,C26,C56,C57	10 µF
3	12	C7,C8,C9,C10,C11,C12,C29,C30,C32,C33,C48,C49	.22 µF
4	13	C16,C17,C20,C21,C22,C23,C24,C25,C35,C36,C40,C47,C50	.01 µF
5	1	C18	150 pF
6	3	C19,C38,C55	47 µF
7	2	C27,C28	22 pF
8	2	C42,C43	4.7 µF
9	1	C46	100 µF
10	2	C52,C53	470 µF
11	1	C58	1.0 µF
12	2	JP2, JP1 (JP2 H and JP1 H)	0 ohm Resistor
13	1	JP3	3x2 HEADER
14	1	J1	MITSUMI
15	4	J2,J3,J8,J9	3.5 mm STEREO JACK
16	1	J4	4X2 HEADER I2S_INTF_978
17	1	J5	13x2 HEADER
18	1	J6	10x2 HEADER
19	1	J7	PWRJACK
20	2	L1,L2	FERRITE BEAD
21	1	P1	CONNECTOR DB15
22	1	Q2	NPN
23	2	R1,R2	7.5K
24	10	R3,R4,R5,R6,R7,R8,R10,R11,R12,R13	2.2K
25	13	R9,R18,R19,R20,R21,R22,R23,R24,R25,R27,R35,R50,R51	10K
26	4	R14,R15,R16,R17	1M
27	1	R26 (R28,R29,R30 Replace U3 of Item #43)	0 ohm
28	1	R31	2.0K
29	1	R32	N/A
30	2	R33,R34	27K
31	3	R37,R46,R47	33K
32	1	R38	100K
33	1	R39	330K
34	4	R40,R41,R42,R43	820K
35	2	R44,R45	2.7 ohm
36	2	R48,R49	15K
37	2	R52,R53	2.7M
38	1	R54	22K
39	3	S1,S2,S3	SW PUSHBUTTON
40	1	U1	ES978 PQFP-100

Table 12 ES978 with ES938 Bill of Materials (BOM) (Continued)

Item	Quantity	Reference	Part
41	2	U2,U4	78L05
42	1	U3	ES938 SSOP-28
43	1	U5	LM1877
44	1	Y1	14.318 MHz