

ZETEX SEMICONDUCTORS

ZVP2110

## P-channel enhancement mode vertical DMOS FET

### FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

### DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

### PRODUCT SUMMARY

Part No.	$BV_{DSS}$	$I_D$	$R_{DS(on)}$
ZVP2110A*	-100V	-0.23A	8Ω
ZVP2110B*	-100V	-0.60A	8Ω
ZVP2110C	-100V	-0.23A	8Ω
ZVP2110E	-100V	-0.23A	8Ω

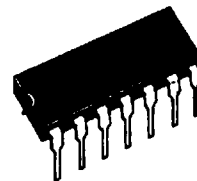
\*BS-CECC approved



E-LINE (TO-92)  
SUFFIX A or C



TO-39  
SUFFIX B



14 LEAD MOULDED DIL  
SUFFIX E

# ZVP2110

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## ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	DIL	Units
$V_{DS}$	Drain-source voltage	-100	-100	-100	V
$I_D$	Continuous drain current (@ $T_A = 25^\circ\text{C}$ )	-0.23	-0.23	-0.23	A
$I_D$	Continuous drain current (@ $T_C = 25^\circ\text{C}$ )	-	-0.60	-	A
$I_{DM}$	Pulsed drain current	-3	-3	-3	A
$V_{GS}$	Gate-source voltage	$\pm 20$	$\pm 20$	$\pm 20$	V
$P_D$	Max. power dissipation (@ $T_A = 25^\circ\text{C}$ )	0.7	0.7	0.85	W
$P_D$	Max. power dissipation (@ $T_C = 25^\circ\text{C}$ )	-	5	-	W
$T_J, T_{stg}$	Operating/storage temperature range	-55 to +150			$^\circ\text{C}$

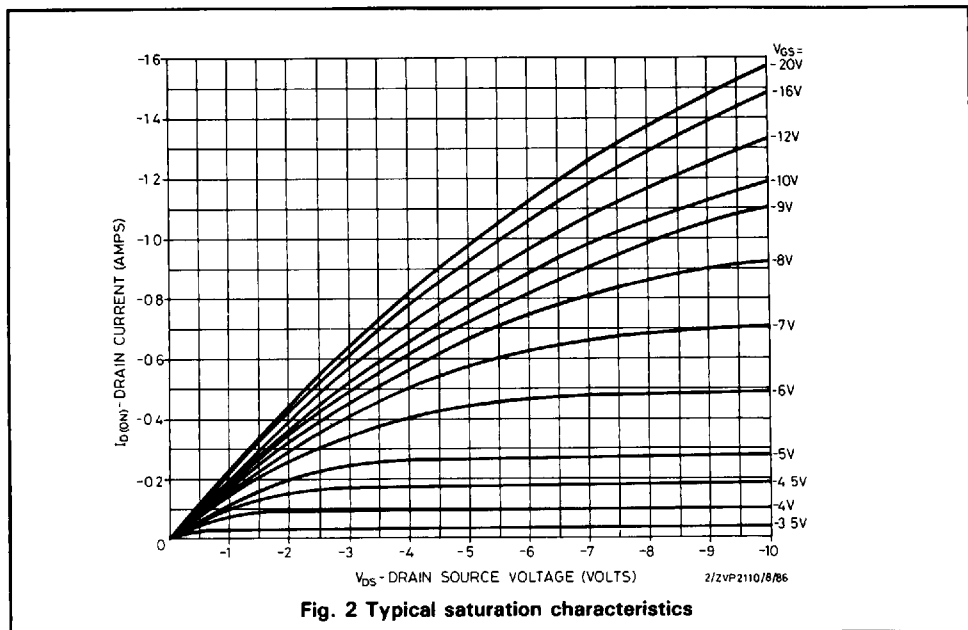
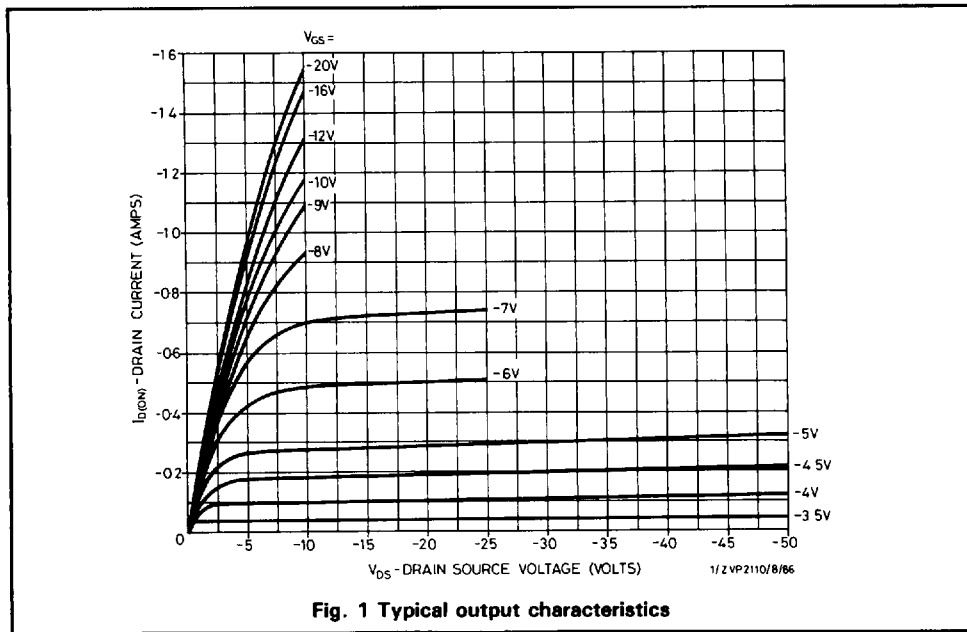
## ELECTRICAL CHARACTERISTICS (at $T = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
$BV_{DSS}$	Drain-source breakdown voltage	-100	-	V	$I_D = -1\text{mA}, V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate-source threshold voltage	-1.5	-3.5	V	$I_D = -1\text{mA}, V_{DS} = V_{GS}$
$I_{GSS}$	Gate body leakage	-	20	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
$I_{DSS}$	Zero gate voltage drain current	-	-1	$\mu\text{A}$	$V_{DS} = \text{Max. rating}, V_{GS} = 0\text{V}$
		-	-100	$\mu\text{A}$	$V_{DS} = 0.8 \times \text{Max. rating}$ $V_{GS} = 0\text{V}$ ( $T = 125^\circ\text{C}$ ) (2)
$I_{D(on)}$	On-state drain current (1)	-750	-	mA	$V_{DS} = -25\text{V}, V_{GS} = -10\text{V}$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	-	8	$\Omega$	$I_D = -375\text{mA}, V_{GS} = -10\text{V}$
$g_{fs}$	Forward transconductance (1) (2)	125	-	mS	$V_{DS} = -25\text{V}, I_D = -375\text{mA}$
$C_{iss}$	Input capacitance (2)	-	100	pF	} $V_{DS} = -25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
$C_{oss}$	Common source output capacitance (2)	-	35	pF	
$C_{rss}$	Reverse transfer capacitance (2)	-	10	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	-	7	ns	} $V_{DD} \approx -25\text{V}, I_D = -375\text{mA}$
$t_r$	Rise time (2) (3)	-	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	-	12	ns	
$t_f$	Fall time (2) (3)	-	15	ns	

(1) Measured under pulsed conditions. Width =  $300\mu\text{s}$ . Duty cycle  $\leq 2\%$ .

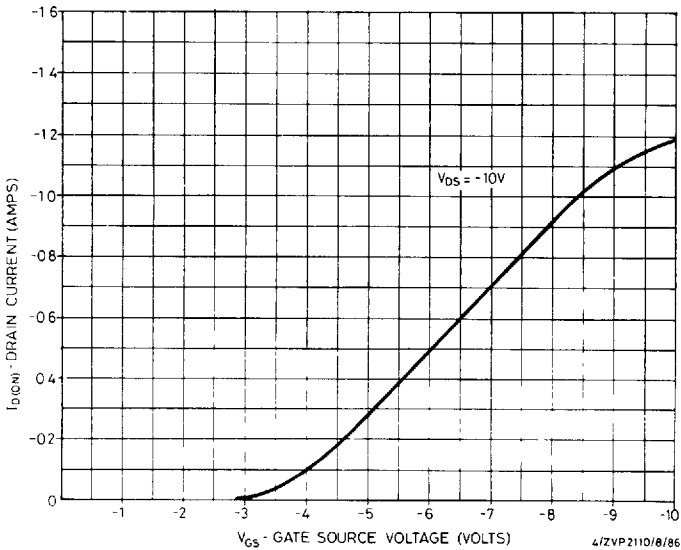
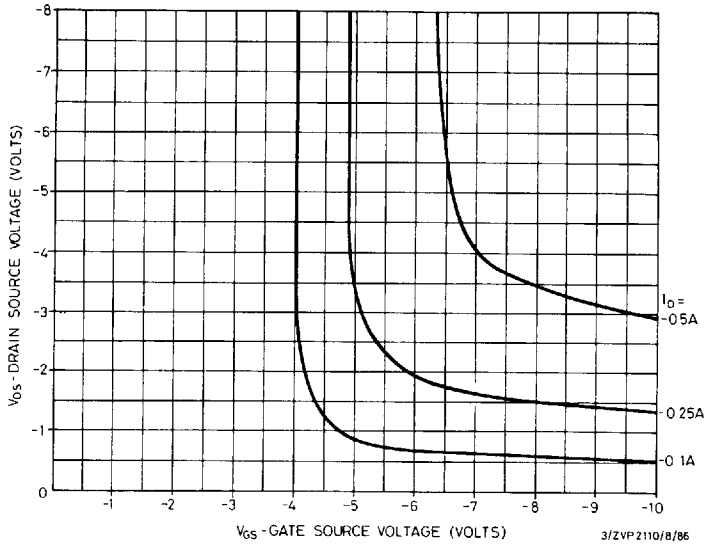
(2) Sample test.

(3) Switching times measured with  $50\Omega$  source impedance and  $< 5\text{ns}$  rise time on a pulse generator.



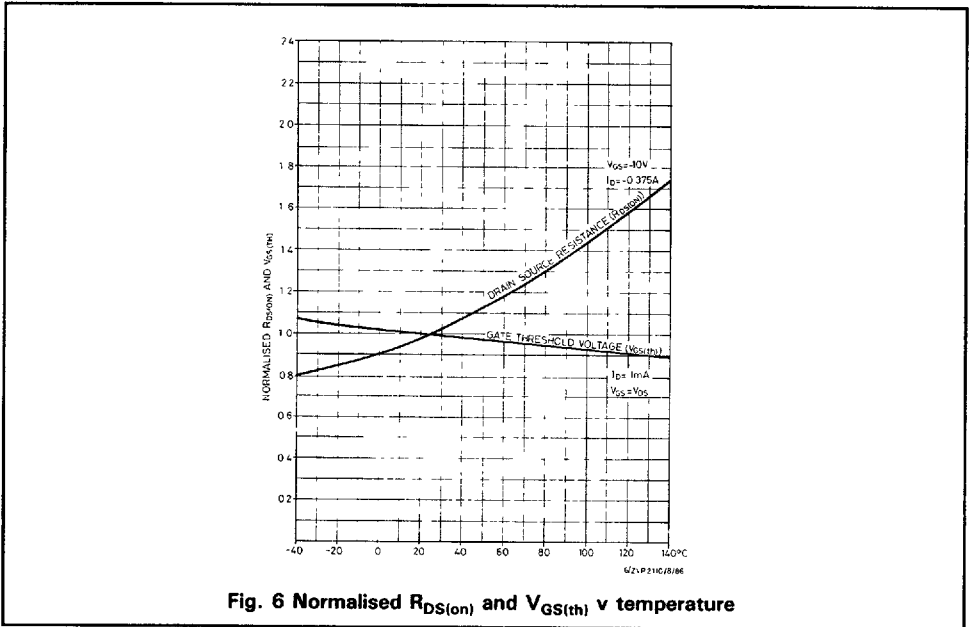
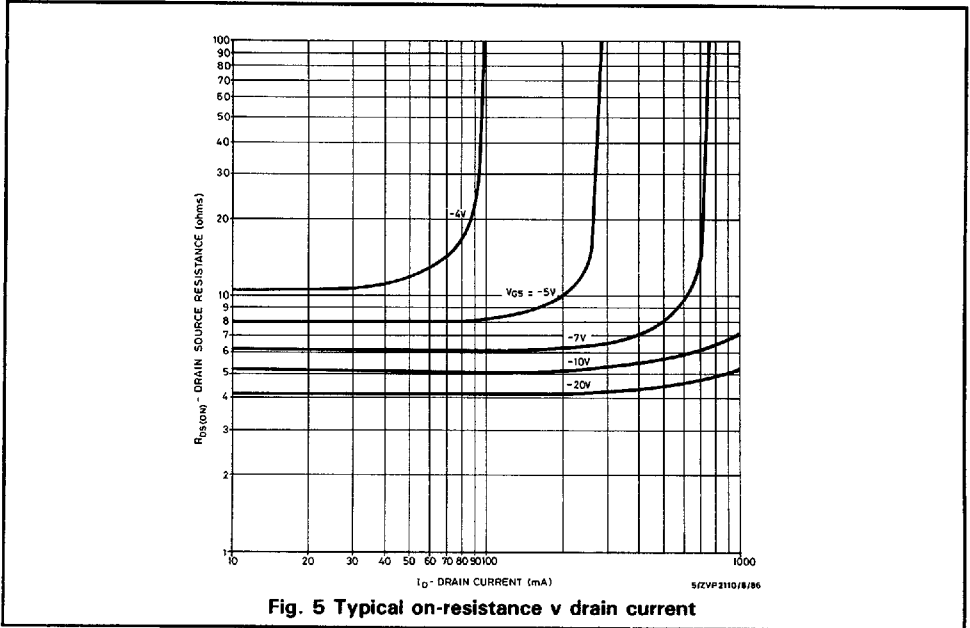
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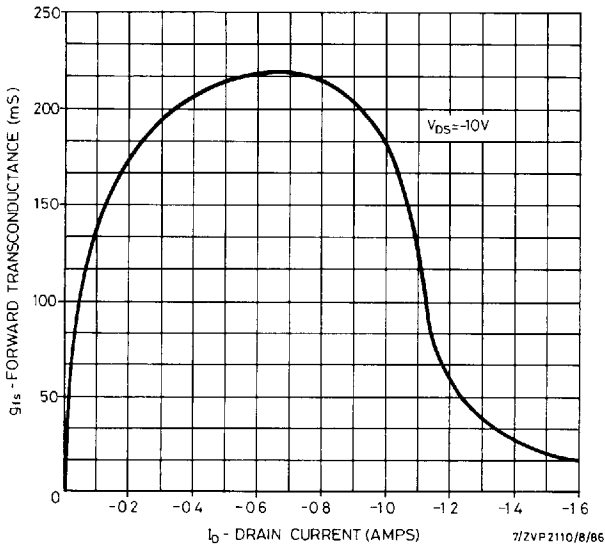


Fig. 7 Typical transconductance v drain current

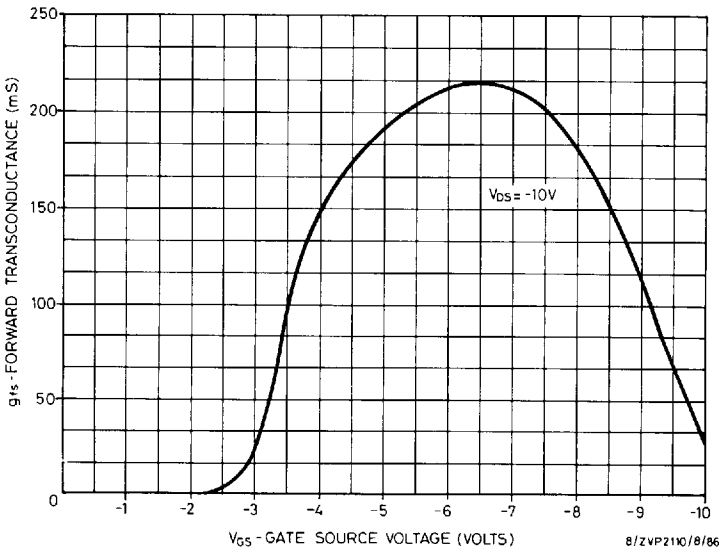


Fig. 8 Typical transconductance v gate-source voltage

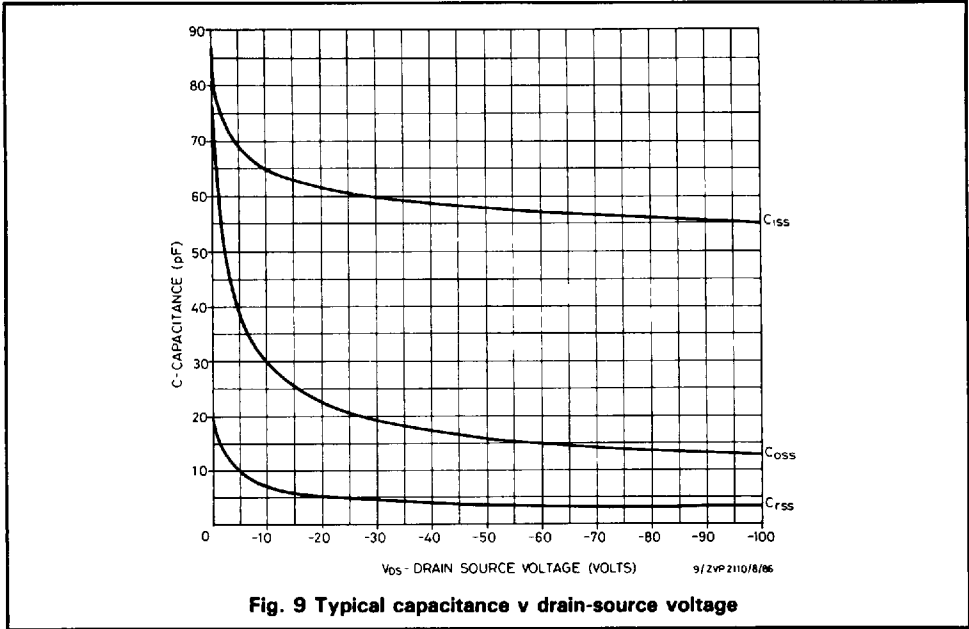


Fig. 9 Typical capacitance v drain-source voltage

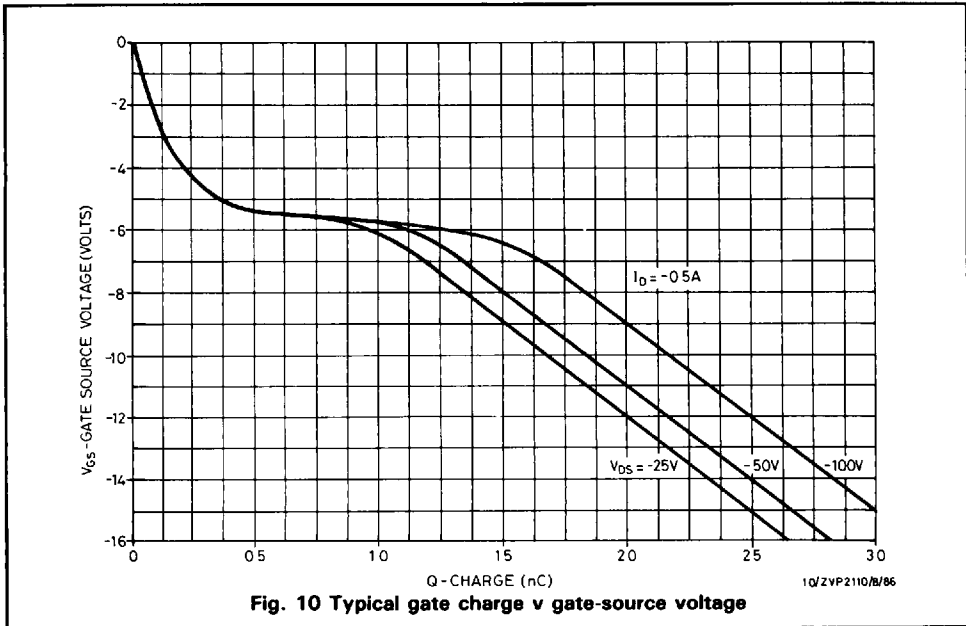


Fig. 10 Typical gate charge v gate-source voltage

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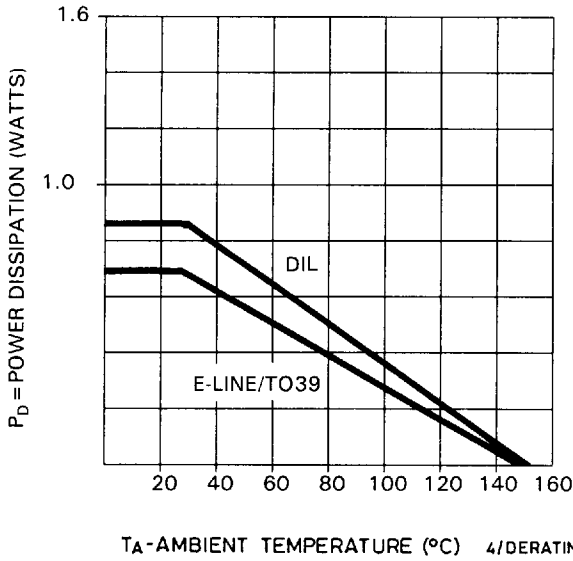


Fig. 11 Power v temperature derating curve (ambient)

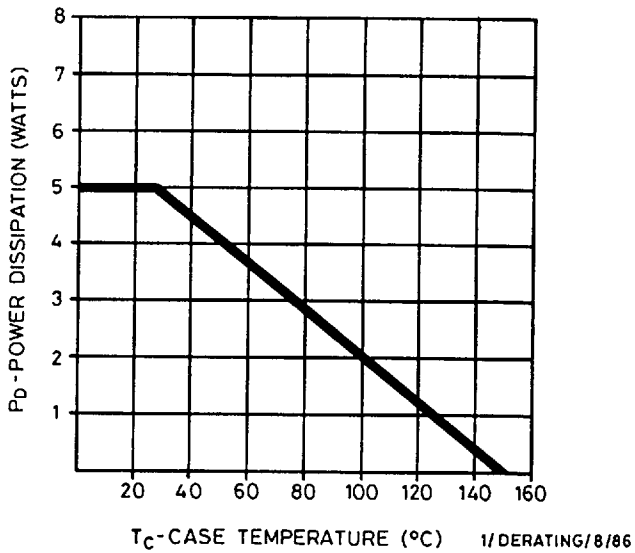


Fig. 12 Power v temperature derating curve (case)