freescale
飞思卡尔(深圳)功率半导体有限公司

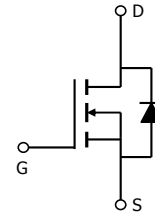**AOT10N65/AOTF10N65**
650V,10A N-Channel MOSFET

General Description

The AOT10N65 & AOTF10N65 have been fabricated using an advanced high voltage MOSFET process that is

designed to deliver high levels of performance and robustness in popular AC-DC applications.

By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be

adopted quickly into new and existing offline power supply designs.

Features

V_{DS}	750V@150℃
I_D (at V_{GS}=10V)	10A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 1Ω

RoHS Compliant

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	AOT10N65	AOTF10N65	Units
Drain-Source Voltage		V_{DS}	650		V
Gate-Source Voltage		V_{GS}	±30		V
Continuous Drain Current	T_C=25°C	I_D	10	10*	A
	T_C=100°C		6.2	6.2*	
Pulsed Drain Current [C]		I_{DM}	36		
Avalanche Current [C]		I_{AR}	3.4		A
Repetitive avalanche energy [C]		E_{AR}	173		mJ
Single pulsed avalanche energy [G]		E_{AS}	347		mJ
Peak diode recovery dv/dt		dv/dt	5		V/ns
Power Dissipation [B]	T_C=25°C	P_D	250	50	W
	Derate above 25°C		2	0.4	W/ °C
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		T_L	300		°C

Thermal Characteristics

Parameter	Symbol	AOT10N65	AOTF10N65	Units
Maximum Junction-to-Ambient [A,D]	$R_{\theta JA}$	65	65	°C/W
Maximum Case-to-sink [A]	$R_{\theta CS}$	0.5	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.5	2.5	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V, T$_J$=25°C	650			V
		I$_D$=250µA, V$_{GS}$=0V, T$_J$=150°C		750		
BV$_{DSS}$/∆TJ	Zero Gate Voltage Drain Current	ID=250µA, VGS=0V		0.75		V/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=650V, V$_{GS}$=0V			1	µA
		V$_{DS}$=520V, T$_J$=125°C			10	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±30V			±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=5V, I$_D$=250µA	3	4	4.5	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=5A		0.77	1	Ω
g$_{FS}$	Forward Transconductance	V$_{DS}$=40V, I$_D$=5A		13		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V		0.73	1	V
I$_S$	Maximum Body-Diode Continuous Current				10	A
I$_{SM}$	Maximum Body-Diode Pulsed Current				36	A
DYNAMIC PARAMETERS						
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=25V, f=1MHz	1095	1369	1645	pF
C$_{oss}$	Output Capacitance		95	118	145	pF
C$_{rss}$	Reverse Transfer Capacitance		8	10	12	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz	1.7	3.5	5.5	Ω
SWITCHING PARAMETERS						
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=520V, I$_D$=10A	22	27.7	33	nC
Q$_{gs}$	Gate Source Charge		6	7.4	9	nC
Q$_{gd}$	Gate Drain Charge		9	11.3	14	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=325V, I$_D$=10A, R$_G$=25Ω		30		ns
t$_r$	Turn-On Rise Time			61		ns
t$_{D(off)}$	Turn-Off DelayTime			74		ns
t$_f$	Turn-Off Fall Time			53		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=10A,dI/dt=100A/µs,V$_{DS}$=100V	255	320	385	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=10A,dI/dt=100A/µs,V$_{DS}$=100V	4.8	6	7.2	µC

A. The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25°C.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150°C, Ratings are based on low frequency and duty cycles to keep initial T$_J$=25°C.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I$_{AS}$=3.4A, V$_{DD}$=150V, R$_G$=25Ω, Starting T$_J$=25°C

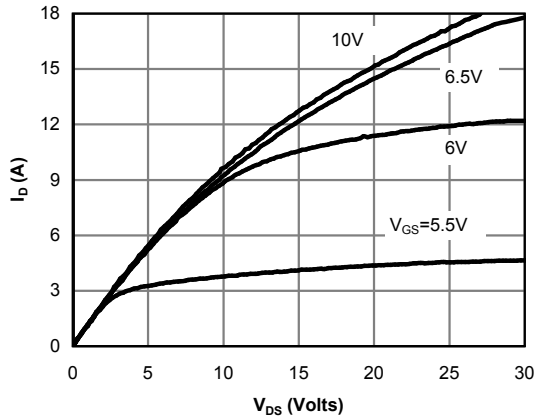## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
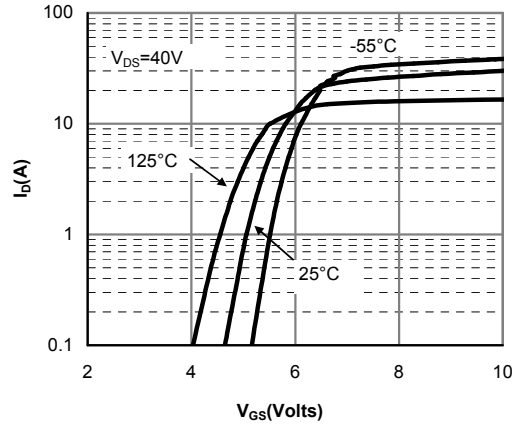
Fig 1: On-Region Characteristics

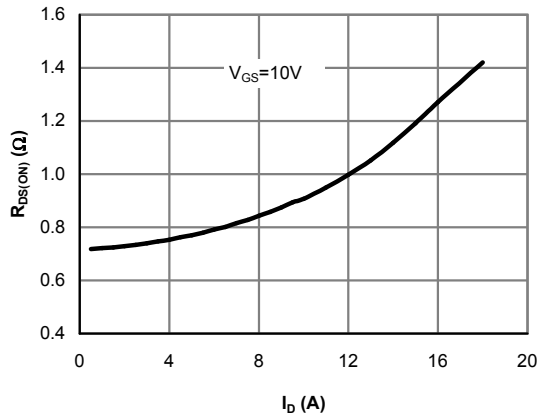Figure 2: Transfer Characteristics

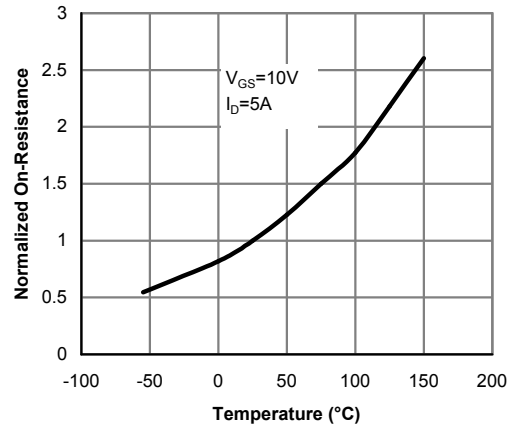Figure 3: On-Resistance vs. Drain Current and Gate Voltage

Figure 4: On-Resistance vs. Junction Temperature

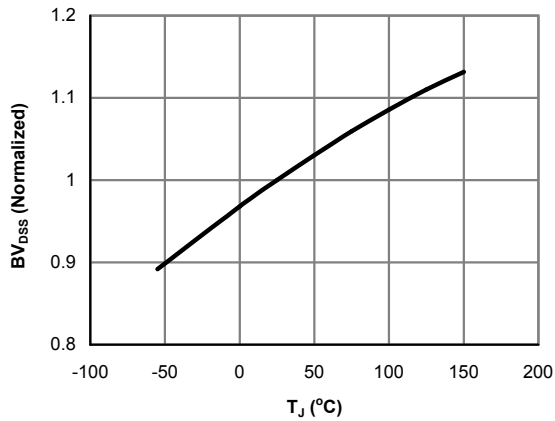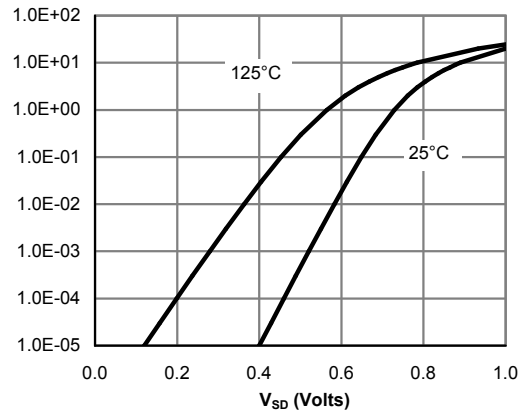Figure 5: Break Down vs. Junction Temperature

Figure 6: Body-Diode Characteristics (Note E)

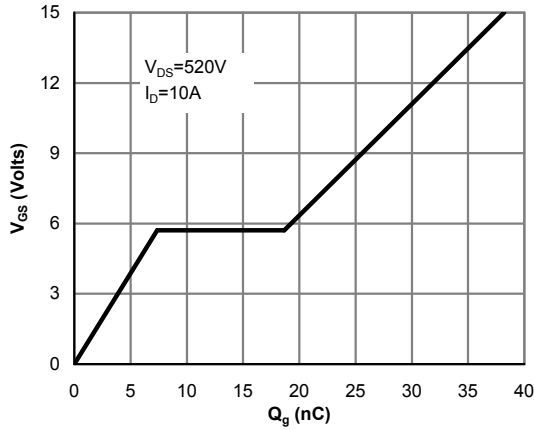**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**
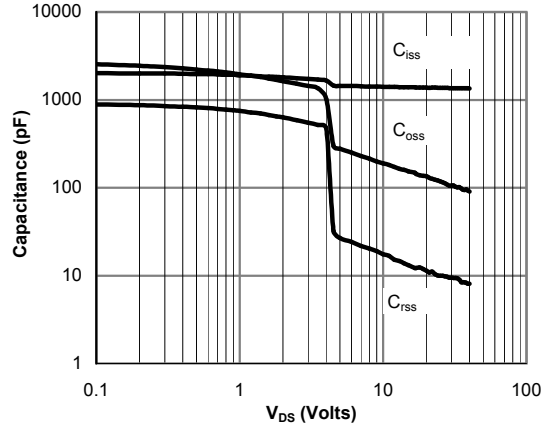
Figure 7: Gate-Charge Characteristics
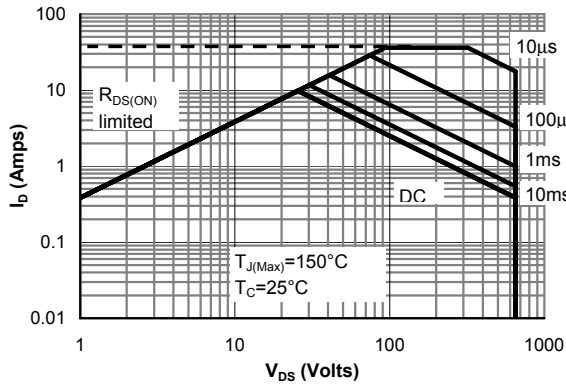
Figure 8: Capacitance Characteristics

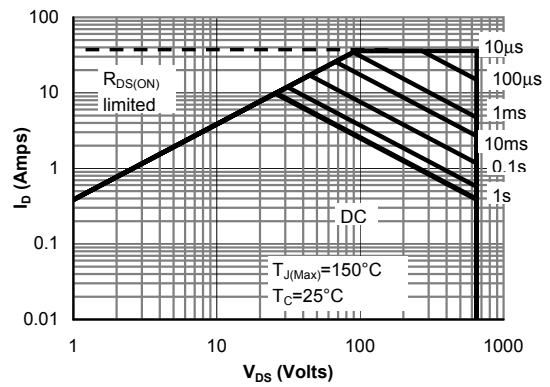**Figure 9: Maximum Forward Biased Safe Operating Area for AOT10N65 (Note F)**

Figure 10: Maximum Forward Biased Safe Operating Area for AOTF10N65 (Note F)
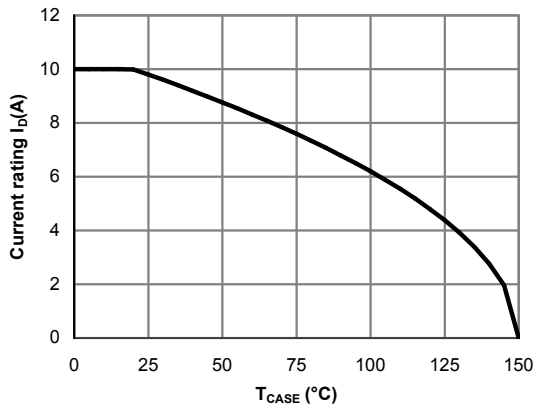
Figure 11: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

$D = T_{on}/T$

$T_{J,PK} = T_c + P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$

$R_{\theta JC} = 0.5°C/W$

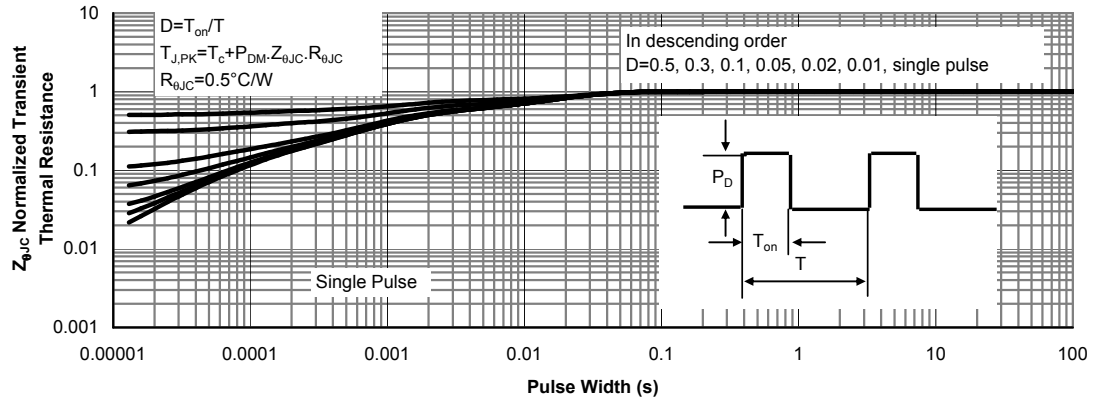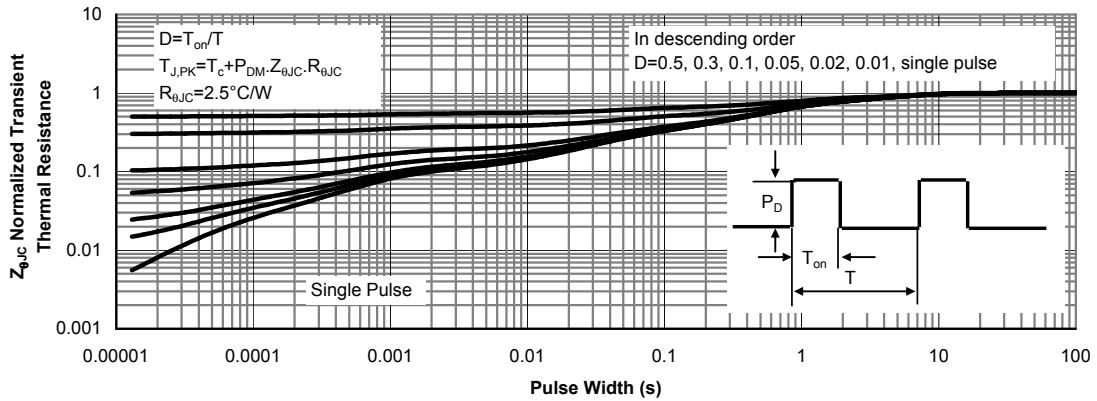In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Figure 12: Normalized Maximum Transient Thermal Impedance for AOT10N65 (Note F)

$D = T_{on}/T$

$T_{J,PK} = T_c + P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$

$R_{\theta JC} = 2.5°C/W$

In descending order
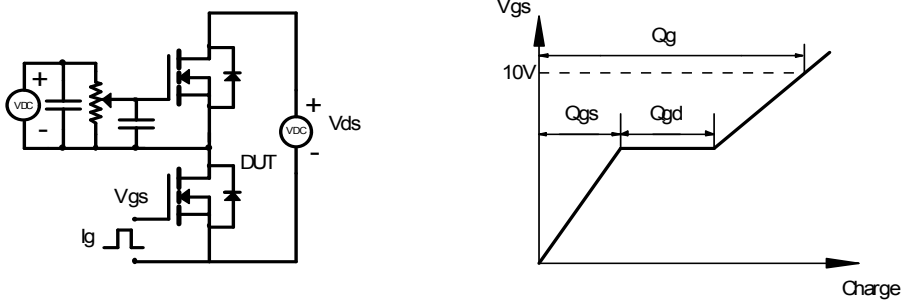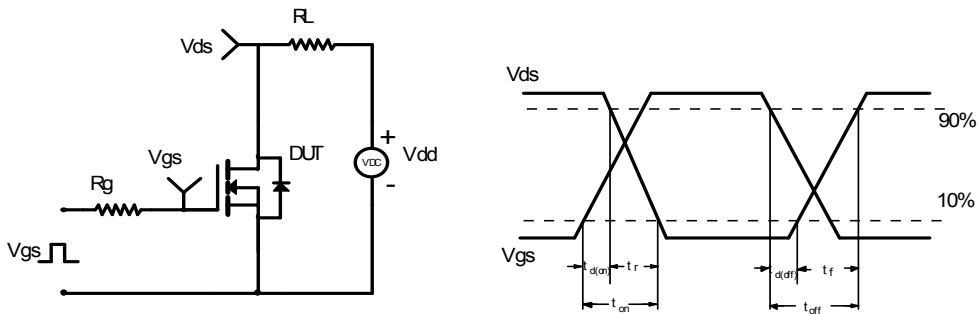D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

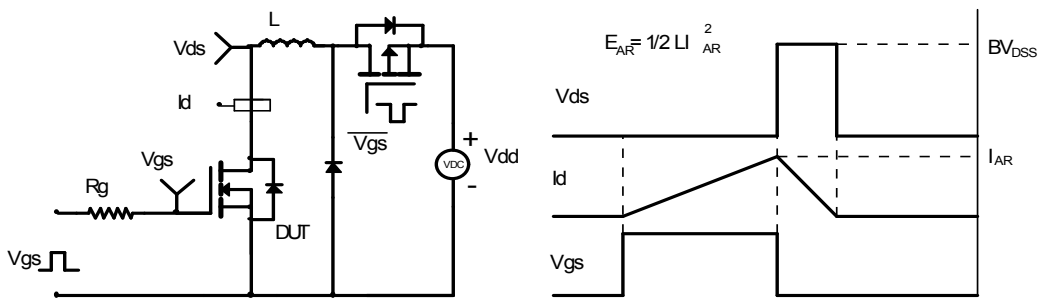**Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF10N65 (Note F)**

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2\, LI_{AR}^2$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int I\, dt$$