



FAN7389

3-Phase Half-Bridge Gate-Drive IC

Features

- Floating Channel for Bootstrap Operation to +600 V
- Typically 350 mA/650 mA Sourcing/Sinking Current Driving Capability for All Channels
- Extended Allowable Negative V_S Swing to -9.8 V for Signal Propagation at $V_{DD}=V_{BS}=15$ V
- Output In-Phase with Input Signal
- Over-Current Shutdown Turns off All Six Drivers
- Matched Propagation Delay for All Channels
- 3.3 V and 5.0 V Input Logic Compatible
- Adjustable Fault-Clear Timing
- Built-in Advanced Input Filter
- Built-in Shoot-Through Prevention Logic
- Built-in Soft Turn-Off Function
- Common-Mode dv/dt Noise Canceling Circuit
- Built-in UVLO Functions for All Channels

Applications

- 3-Phase Motor Inverter Driver
- Air Conditioners
- Washing Machines
- General-Purpose Three-Phase Inverters

Description

The FAN7389 is a monolithic three-phase half-bridge gate-drive IC designed for high-voltage, high-speed driving MOSFETs and IGBTs operating up to +600 V.

Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V.

The protection functions include under-voltage lockout and inverter over-current trip with an automatic fault-clear function.

Over-current protection that terminates all six outputs can be derived from an external current-sense resistor. An open-drain fault signal is provided to indicate that an over-current or under-voltage shutdown has occurred.

The UVLO circuits prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

Output drivers typically source and sink 350 mA and 650 mA, respectively; which is suitable for three-phase half-bridge applications in motor drive systems.

28-SOIC



Ordering Information

Part Number	Package	Operating Temperature	Packing Method
FAN7389MX1 ⁽¹⁾	28-Lead, Small Outline Integrated Circuit Wide Body (SOIC)	-40 to +125°C	Tape & Reel

Note:

1. These devices passed wave soldering test by JESD22A-111.

Typical Application Diagram

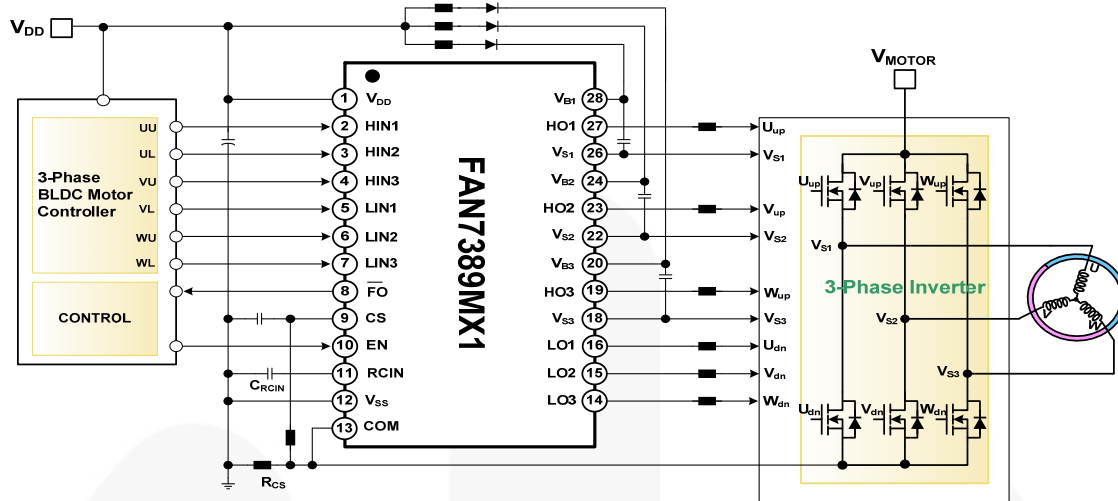


Figure 1. 3-Phase BLDC Motor Drive Application

Internal Block Diagram

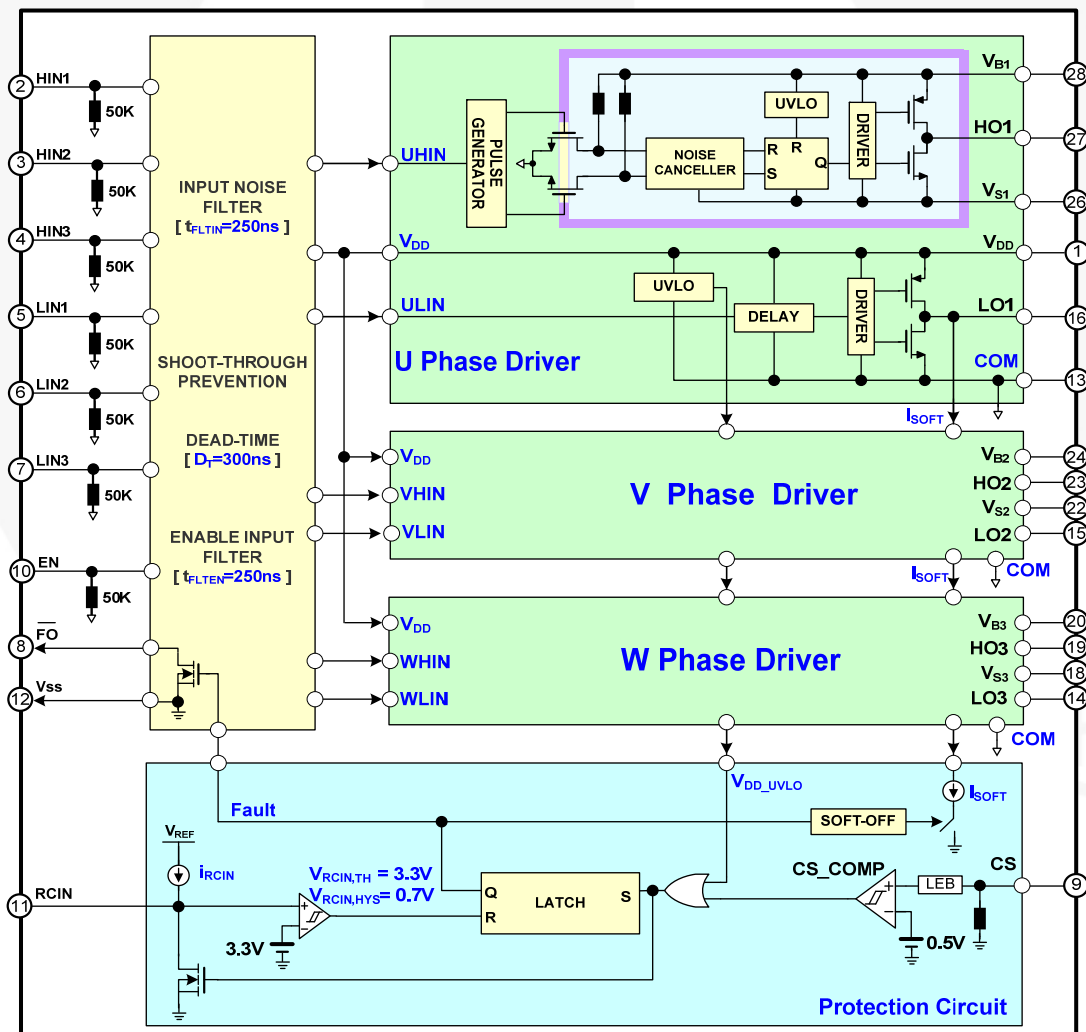


Figure 2. Functional Block Diagram

Pin Configuration

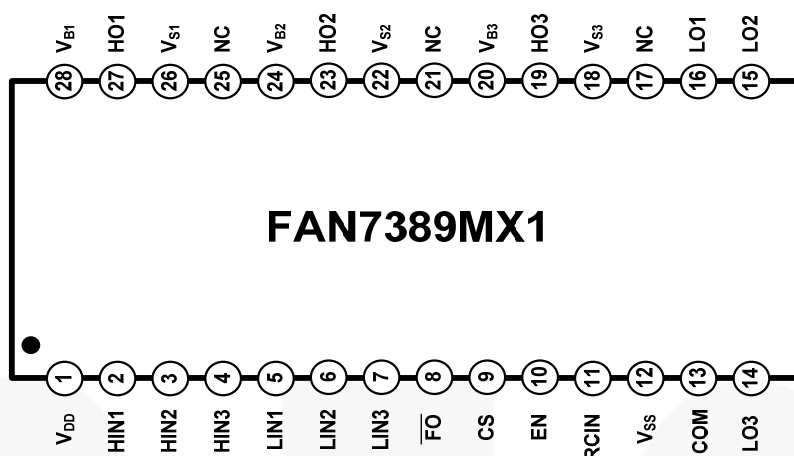


Figure 3. Pin Configuration

Pin Definitions

Pin	Name	Description
1	V _{DD}	Logic and low-side gate driver power supply voltage
2	HIN1	Logic Input 1 for high-side gate 1 driver
3	HIN2	Logic Input 2 for high-side gate 2 driver
4	HIN3	Logic Input 3 for high-side gate 3 driver
5	LIN1	Logic Input 1 for low-side gate 1 driver
6	LIN2	Logic Input 2 for low-side gate 2 driver
7	LIN3	Logic Input 3 for low-side gate 3 driver
8	FO	Fault output with open drain (indicates over-current and low-side under-voltage)
9	CS	Analog input for over-current shutdown
10	EN	Logic input for shutdown functionality
11	RCIN	An external RC network input used to define the fault-clear delay
12	V _{SS}	Logic ground
13	COM	Low-side driver return
14	LO3	Low-side gate driver 3 output
15	LO2	Low-side gate driver 2 output
16	LO1	Low-side gate driver 1 output
17, 21, 25	NC	No connect
18	V _{S3}	High-side driver 3 floating supply offset voltage
19	HO3	High-side driver 3 gate driver output
20	V _{B3}	High-side driver 3 floating supply
22	V _{S2}	High-side driver 2 floating supply offset voltage
23	HO2	High-side driver 2 gate driver output
24	V _{B2}	High-side driver 2 floating supply
26	V _{S1}	High-side driver 1 floating supply offset voltage
27	HO1	High-side driver 1 gate driver output
28	V _{B1}	High-side driver 1 floating supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_S	High-Side Floating Offset Voltage	$V_{B1,2,3}-25.0$	$V_{B1,2,3}+0.3$	V
V_B	High-Side Floating Supply Voltage	-0.3	625.0	V
V_{DD}	Low-Side and Logic-Fixed Supply Voltage	-0.3	25.0	V
V_{HO}	High-Side Floating Output Voltage $V_{HO1,2,3}$	$V_{S1,2,3}-0.3$	$V_{B1,2,3}+0.3$	V
V_{LO}	Low-Side Floating Output Voltage $V_{LO1,2,3}$	-0.3	$V_{DD}+0.3$	V
V_{IN}	Input Voltage (HINx, LINx, CS, and EN)	-0.3	5.5	V
V_{FO}	Fault Output Voltage (\overline{FO})	-0.3	$V_{DD}+0.3$	V
PW_{HIN}	High-Side Input Pulse Width	500		ns
dV_S/dt	Allowable Offset Voltage Slew Rate		± 50	V/ns
P_D	Power Dissipation ^(2,3,4)		1.4	W
θ_{JA}	Thermal Resistance		70	$^{\circ}\text{C}/\text{W}$
T_J	Junction Temperature		150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-55	150	$^{\circ}\text{C}$

Notes:

- Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.
- Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{B1,2,3}$	High-Side Floating Supply Voltage	$V_{S1,2,3}+10$	$V_{S1,2,3}+20$	V
$V_{S1,2,3}$	High-Side Floating Supply Offset Voltage	$6-V_{DD}$	600	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	10	20	V
$V_{HO1,2,3}$	High-Side Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	V
$V_{LO1,2,3}$	Low-Side Output Voltage	COM	V_{DD}	V
V_{FO}	Fault Output Voltage (\overline{FO})	COM	V_{DD}	V
V_{CS}	Current-Sense Pin Input Voltage	COM	5	V
V_{IN}	Logic Input Voltage (HIN1,2,3 and LIN1,2,3)	COM	5	V
V_{SS}	Logic Ground	-5	5	V
T_A	Ambient Temperature	-40	+125	$^{\circ}\text{C}$

Electrical Characteristics

V_{BIAS} (V_{DD} , $V_{BS1,2,3}$) = 15.0 V and T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to all six channels. The V_O and I_O parameters are referenced to $V_{S1,2,3}$ and COM and are applicable to the respective output leads: HO1,2,3 and LO1,2,3. The V_{DDUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to $V_{S1,2,3}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Low-Side Power Supply Section						
I_{QDD}	Quiescent V_{DD} Supply Current	$V_{LIN1,2,3}=0$ V or 5 V, EN=0 V		200		μ A
I_{PDD}	Operating V_{DD} Supply Current	$f_{LIN1,2,3}=20$ kHz, rms Value		400		μ A
V_{DDUV+}	V_{DD} Supply Under-Voltage Positive-Going Threshold	$V_{DD}=\text{Sweep}$	7.5	8.5	9.3	V
V_{DDUV-}	V_{DD} Supply Under-Voltage Negative-Going Threshold	$V_{DD}=\text{Sweep}$	7.0	8.0	8.7	V
V_{DDHYS}	V_{DD} Supply Under-Voltage Lockout Hysteresis	$V_{DD}=\text{Sweep}$		0.5		V
Bootstrapped Power Supply Section						
V_{BSUV+}	V_{BS} Supply Under-Voltage Positive-Going Threshold	$V_{BS1,2,3}=\text{Sweep}$	7.5	8.5	9.3	V
V_{BSUV-}	V_{BS} Supply Under-Voltage Negative-Going Threshold	$V_{BS1,2,3}=\text{Sweep}$	7.0	8.0	8.7	V
V_{BSHYS}	V_{BS} Supply Under-Voltage Lockout Hysteresis	$V_{BS1,2,3}=\text{Sweep}$		0.5		V
I_{LK}	Offset Supply Leakage Current	$V_{B1,2,3}=V_{S1,2,3}=600$ V			10	μ A
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{HIN1,2,3}=0$ V or 5 V, EN=0V	10	50	80	μ A
I_{PBS}	Operating V_{BS} Supply Current	$f_{HIN1,2,3}=20$ kHz, rms Value	200	420	480	μ A
Gate Driver Output Section						
V_{OH}	High-Level Output voltage, $V_{BIAS}-V_O$	$I_O=0$ mA (No Load)			100	mV
V_{OL}	Low-Level Output voltage, V_O	$I_O=0$ mA (No Load)			100	mV
I_{O+}	Output HIGH Short-Circuit Pulse Current ⁽⁵⁾	$V_O=0$ V, $V_{IN}=5$ V with $PW \leq 10$ μ s	250	350		mA
I_{O-}	Output LOW Short-Circuit Pulsed Current ⁽⁵⁾	$V_O=15$ V, $V_{IN}=0$ V with $PW \leq 10$ μ s	500	650		mA
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO			-9.8	-7.0	V
Logic Input Section						
V_{IH}	Logic "1" Input Voltage HIN1,2,3, LIN1,2,3		2.5			V
V_{IL}	Logic "0" Input Voltage HIN1,2,3, LIN1,2,3				0.8	V
I_{IN+}	Logic Input Bias Current (HO=LO=HIGH)	$V_{IN}=5$ V		100		μ A
I_{IN-}	Logic Input Bias Current (HO=LO=LOW)	$V_{IN}=0$ V			2	μ A
R_{IN}	Logic Input Pull-Down Resistance			50		K Ω
Enable Control Section (EN)						
V_{EN+}	Enable Positive-Going Threshold Voltage		2.5			V
V_{EN-}	Enable Negative-Going Threshold Voltage				0.8	V
I_{EN+}	Logic Enable "1" Input Bias Current	$V_{EN}=5$ V (Pull-Down=150K Ω)		33		μ A
I_{EN-}	Logic Enable "0" Input Bias Current	$V_{EN}=0$ V			2	μ A

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Electrical Characteristics

V_{BIAS} (V_{DD} , $V_{BS1,2,3}$) = 15.0 V and T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to all six channels. The V_O and I_O parameters are referenced to $V_{S1,2,3}$ and COM and are applicable to the respective output leads: HO1,2,3 and LO1,2,3. The V_{DDUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to $V_{S1,2,3}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Over-Current Protection Section						
V_{CSTH+}	Over-Current Detect Positive Threshold ⁽⁵⁾		400	500	600	mV
V_{CSTH-}	Over-Current Detect Negative Threshold ⁽⁵⁾			440		mV
V_{CSHYS}	Over-Current Detect Hysteresis ⁽⁵⁾			60		mV
I_{CSIN}	Short-Circuit Input Current	$V_{CSIN}=1$ V	5	10	15	μA
I_{SOFT}	Soft Turn-Off Sink Current		25	40	55	mA
Fault Output Section						
$V_{RCINTH+}$	RCIN Positive-Going Threshold Voltage			3.3		V
$V_{RCINTH-}$	RCIN Negative-Going Threshold Voltage			2.6		V
$V_{RCINHYS}$	RCIN Hysteresis Voltage			0.7		V
I_{RCIN}	RCIN Internal Current Source	$C_{RCIN}=2$ nF	3	5	7	μA
V_{FOL}	Fault Output Low Level Voltage	$V_{CS}=1$ V, $I_{FO}=1.5$ mA		0.2	0.5	V
R_{DSRCIN}	RCIN On Resistance	$I_{RCIN}=1.5$ mA	50	75	100	Ω
R_{DSFO}	Fault Output On Resistance	$I_{FO}=1.5$ mA	90	130	170	Ω

Note:

5. These parameters are guaranteed by design.

Dynamic Electrical Characteristics

$T_A=25^\circ\text{C}$, V_{BIAS} (V_{DD} , $V_{BS1,2,3}$) = 15.0 V, $V_{S1,2,3}$ = COM, $C_{RCIN}=2$ nF, and C_{Load} = 1000 pF unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-On Propagation Delay	$V_{LIN1,2,3}=V_{HIN1,2,3}=0$ V, $V_{S1,2,3}=0$ V	350	500	650	ns
t_{OFF}	Turn-Off Propagation Delay	$V_{LIN1,2,3}=V_{HIN1,2,3}=5$ V, $V_{S1,2,3}=0$ V	350	500	650	ns
t_R	Turn-On Rise Time	$V_{LIN1,2,3}=V_{HIN1,2,3}=0$ V	20	50	100	ns
t_F	Turn-Off Fall Time	$V_{LIN1,2,3}=V_{HIN1,2,3}=5$ V	10	30	80	ns
t_{EN}	Enable LOW to Output Shutdown Delay		400	500	600	ns
t_{CSBLT}	CS Pin Leading-Edge Blanking Time ⁽⁶⁾		200	300	400	ns
t_{CSFO}	Time from CS Triggering to \overline{FO} ⁽⁷⁾	From $V_{CSC}=1$ V to \overline{FO} Turn-Off		630		ns
t_{CSOFF}	Time from CS Triggering to All Gate Outputs Turn-Off ⁽⁷⁾	From $V_{CSC}=1$ V to Starting Gate Turn-Off		640		ns
t_{FLTIN}	Input Filtering Time ⁽⁸⁾ ($HINx$, $LINx$, EN)		200	250	300	ns
t_{FLTCLR}	Fault-Clear Time			1.3		ms
DT	Dead Time		250	300	350	ns
MDT	Dead-Time Matching (All Six Channels)				50	ns
MT	Delay Matching (All Six Channels)				50	ns
PM	Output Pulse-Width Matching ^(6,9)	$PW_{IN} > 1$ μs		50	100	ns

Notes:

6. These parameters are guaranteed by design.
 7. These parameters are referenced to specified $C_{RCIN}(=2$ nF), and proportional to value of C_{RCIN} as shown in Figure 43. It is strongly recommended that the capacitor on R_{CIN} pin should be less than 5 nF.
 8. The minimum width of the input pulse should exceed 500 ns to ensure the filtering time of the input filter is exceeded.
 9. PM is defined as $PW_{IN}-PW_{OUT}$.

Typical Characteristics

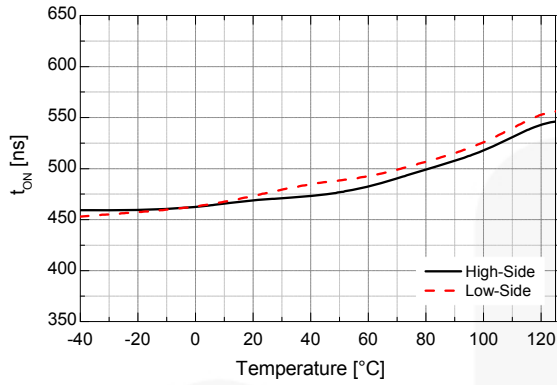


Figure 4. Turn-On Propagation Delay vs. Temperature

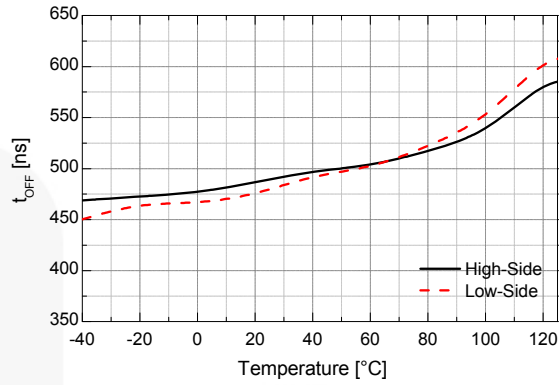


Figure 5. Turn-Off Propagation Delay vs. Temperature

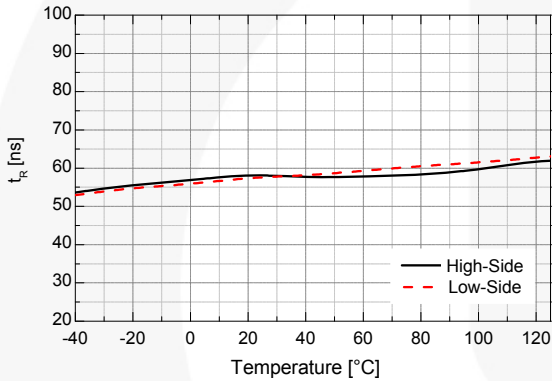


Figure 6. Turn-On Rise Time vs. Temperature

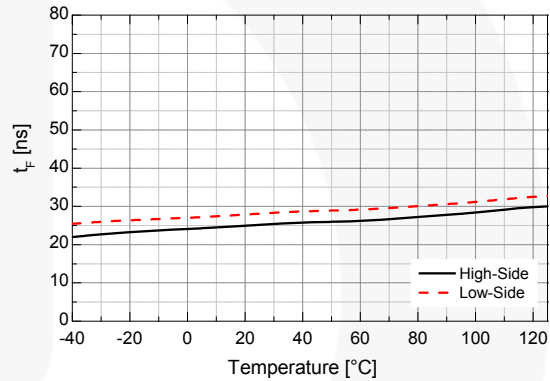


Figure 7. Turn-Off Fall Time vs. Temperature

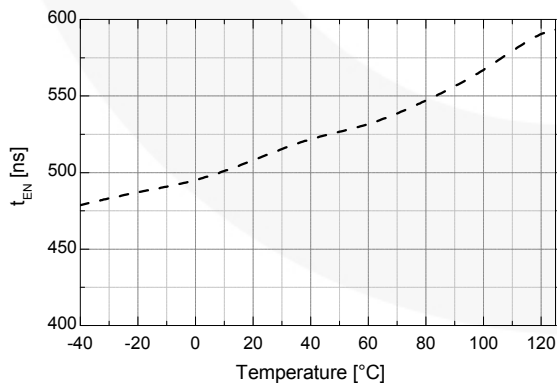


Figure 8. Enable LOW to Output Shutdown Delay vs. Temperature

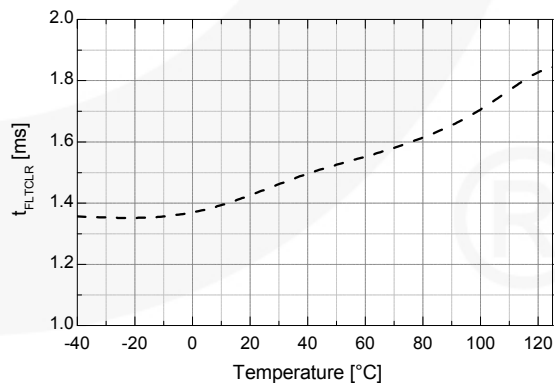


Figure 9. Fault-Clear Time vs. Temperature

Typical Characteristics (Continued)

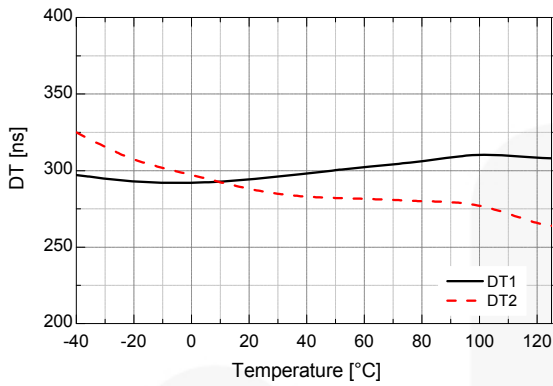


Figure 10. Dead Time vs. Temperature

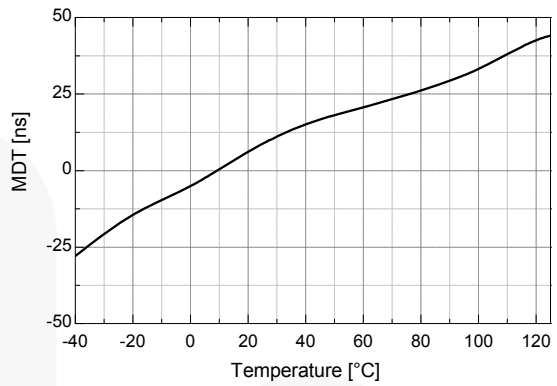


Figure 11. Dead-Time Matching vs. Temperature

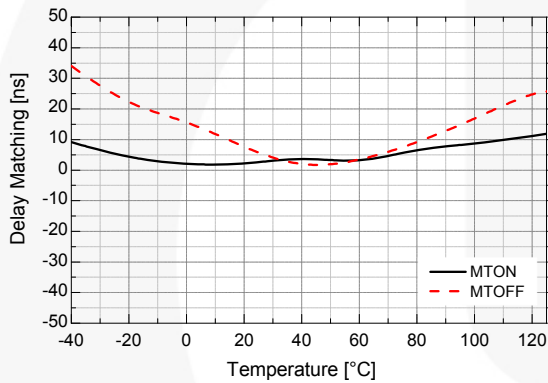


Figure 12. Delay Matching vs. Temperature

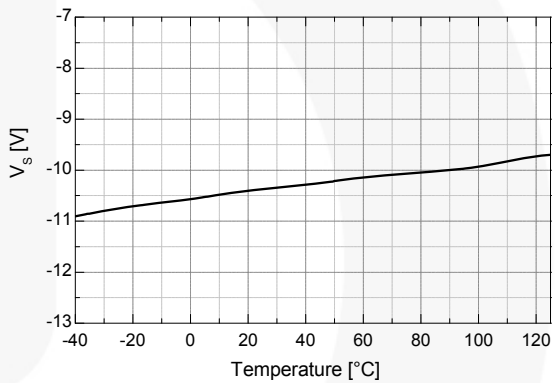


Figure 13. Allowable Negative V_S Voltage vs. Temperature

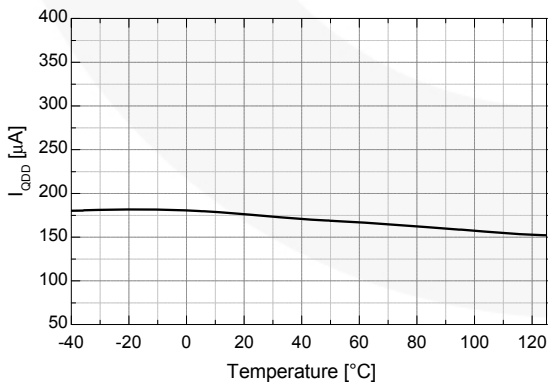


Figure 14. Quiescent V_{DD} Supply Current vs. Temperature

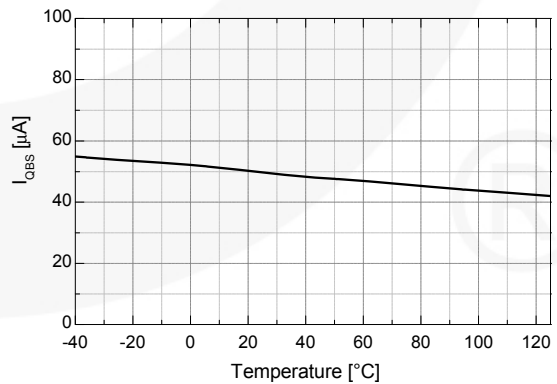


Figure 15. Quiescent V_{BS} Supply Current vs. Temperature

Typical Characteristics (Continued)

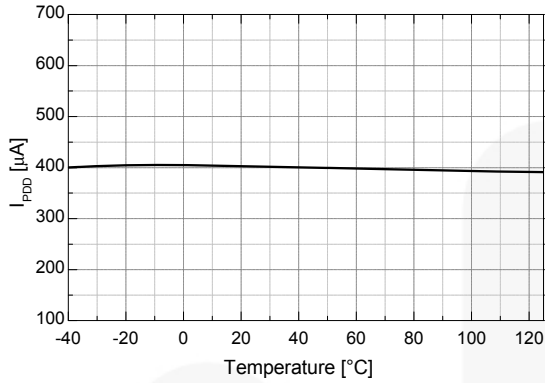


Figure 16. Operating V_{DD} Supply Current vs. Temperature

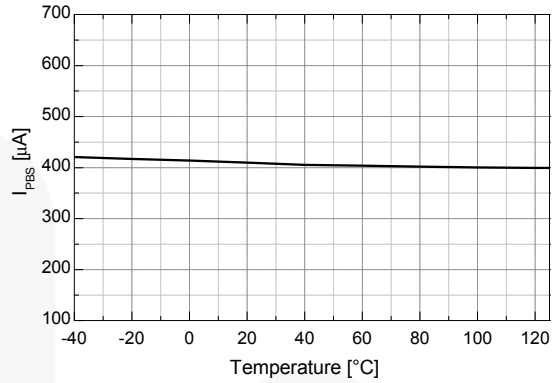


Figure 17. Operating V_{BS} Supply Current vs. Temperature

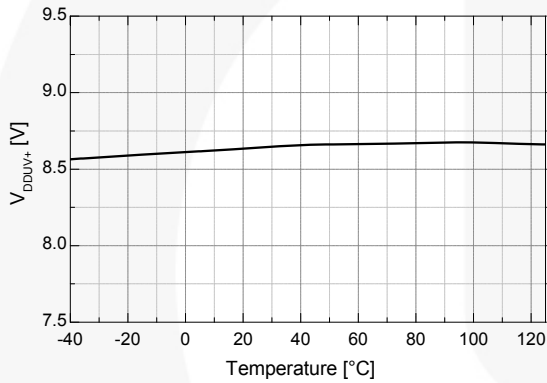


Figure 18. V_{DD} UVLO+ vs. Temperature

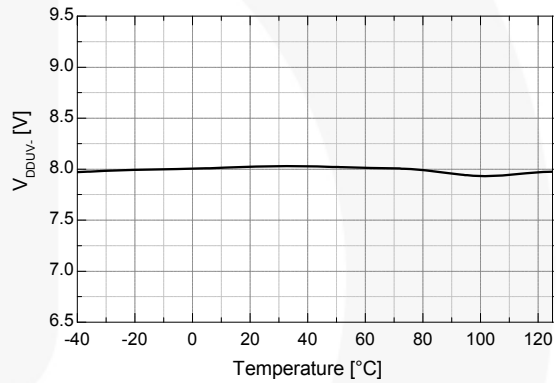


Figure 19. V_{DD} UVLO- vs. Temperature

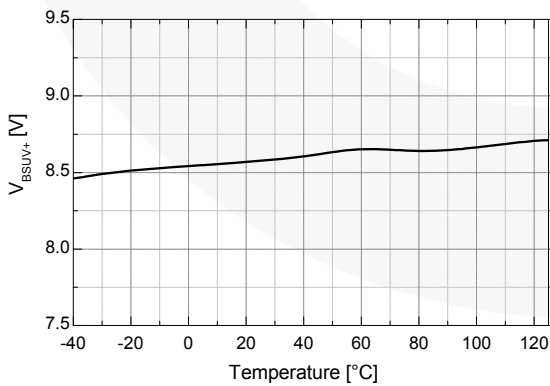


Figure 20. V_{BS} UVLO+ vs. Temperature

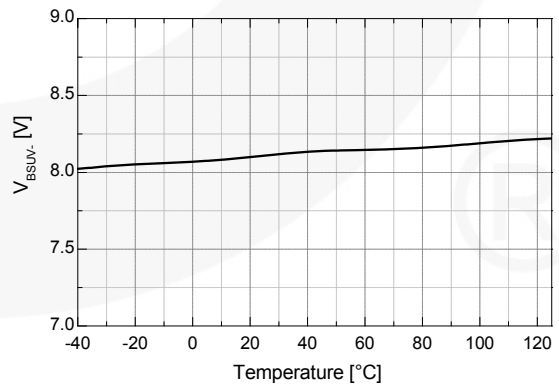


Figure 21. V_{BS} UVLO- vs. Temperature

Typical Characteristics (Continued)

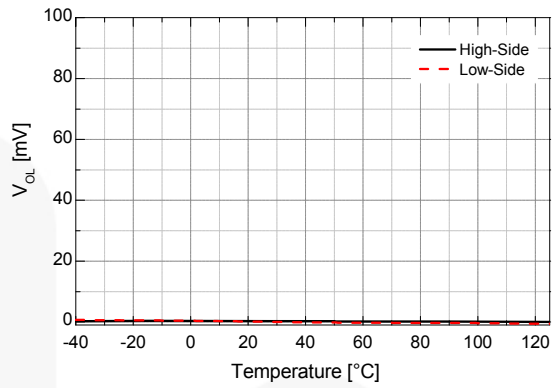
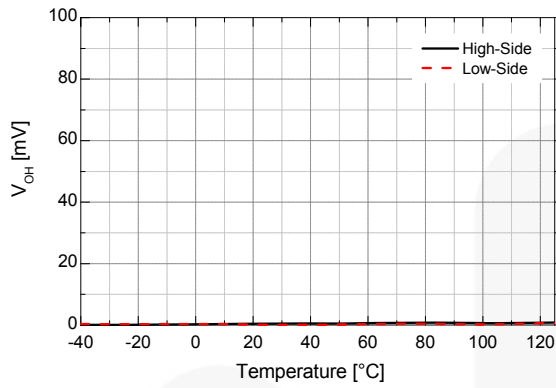


Figure 22. High-Level Output Voltage vs. Temperature Figure 23. Low-Level Output Voltage vs. Temperature

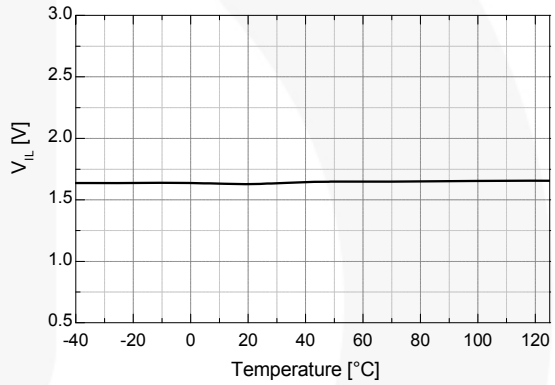
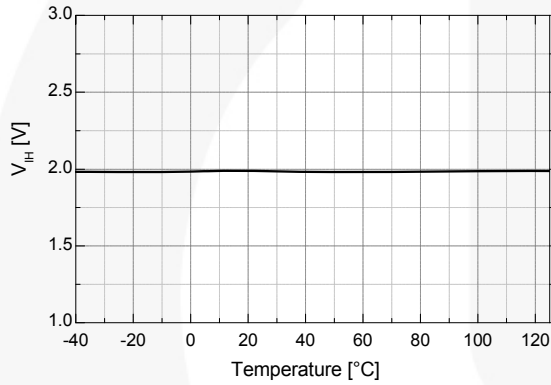


Figure 24. Logic HIGH Input Voltage vs. Temperature Figure 25. Logic LOW Input Voltage vs. Temperature

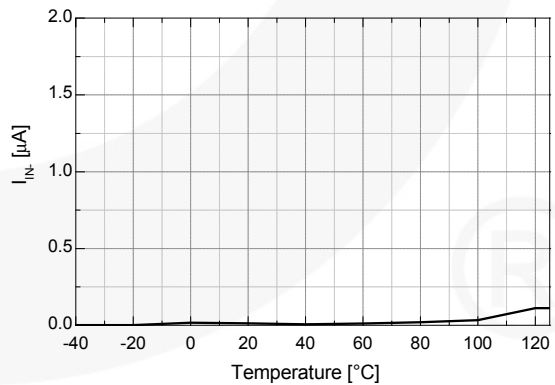
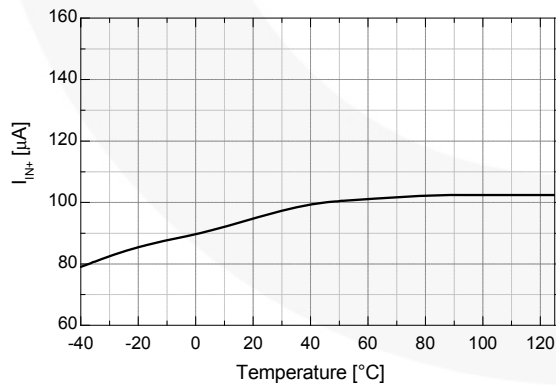


Figure 26. Logic Input HIGH Bias Current vs. Temperature

Figure 27. Logic Input LOW Bias Current vs. Temperature

Typical Characteristics (Continued)

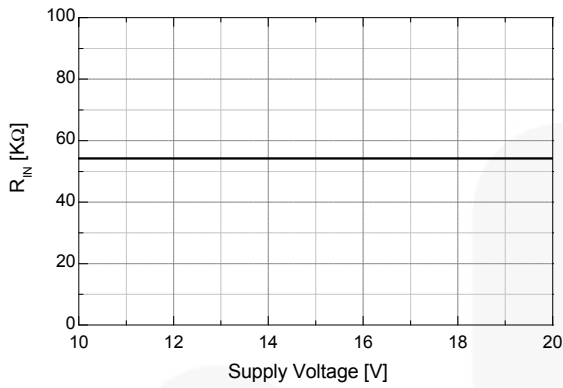


Figure 28. Input Pull-Down Resistance vs. Supply Voltage

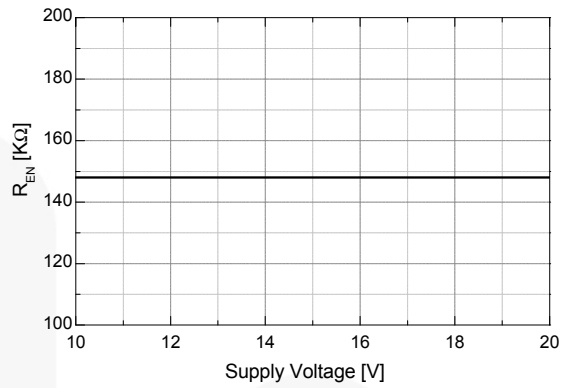


Figure 29. Enable Pin Pull-Down Resistance vs. Supply Voltage

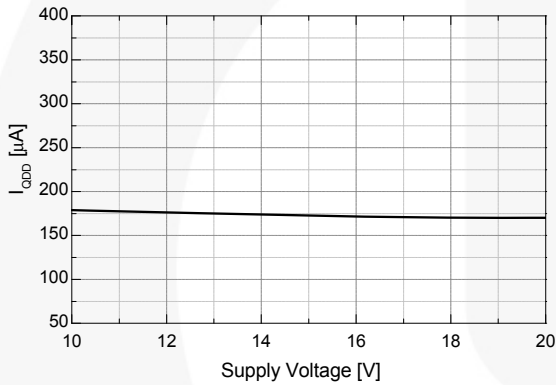


Figure 30. Quiescent V_{DD} Supply Current vs. Supply Voltage

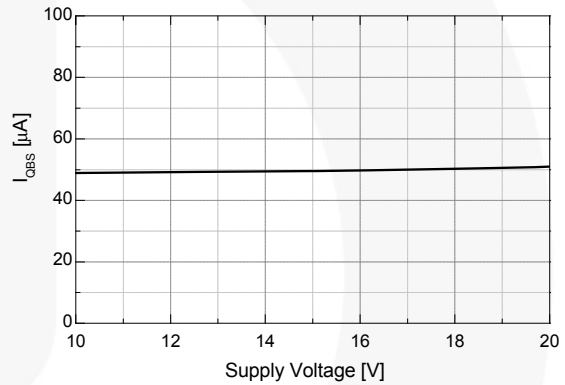


Figure 31. Quiescent V_{BS} Supply Current vs. Supply Voltage

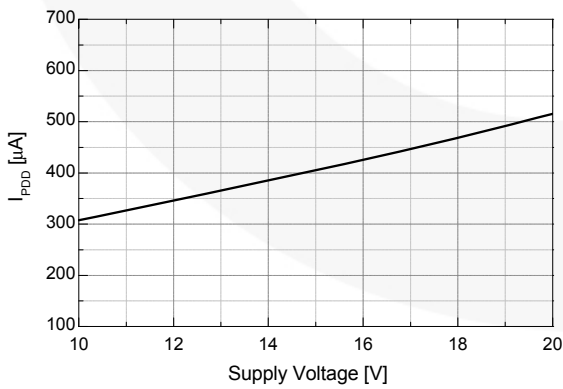


Figure 32. Operating V_{DD} Supply Current vs. Supply Voltage

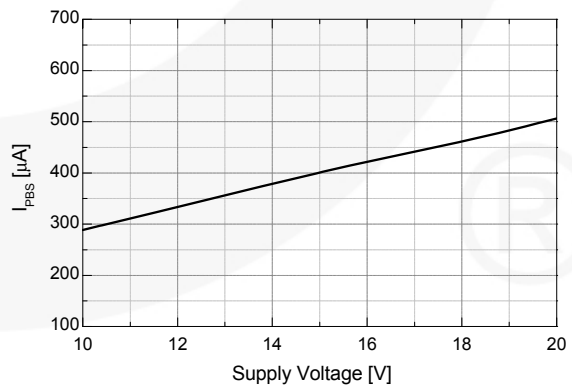


Figure 33. Operating V_{BS} Supply Current vs. Supply Voltage

Switching Time Definitions

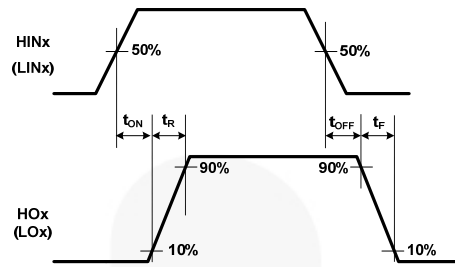


Figure 34. Switching Time Waveform Definitions

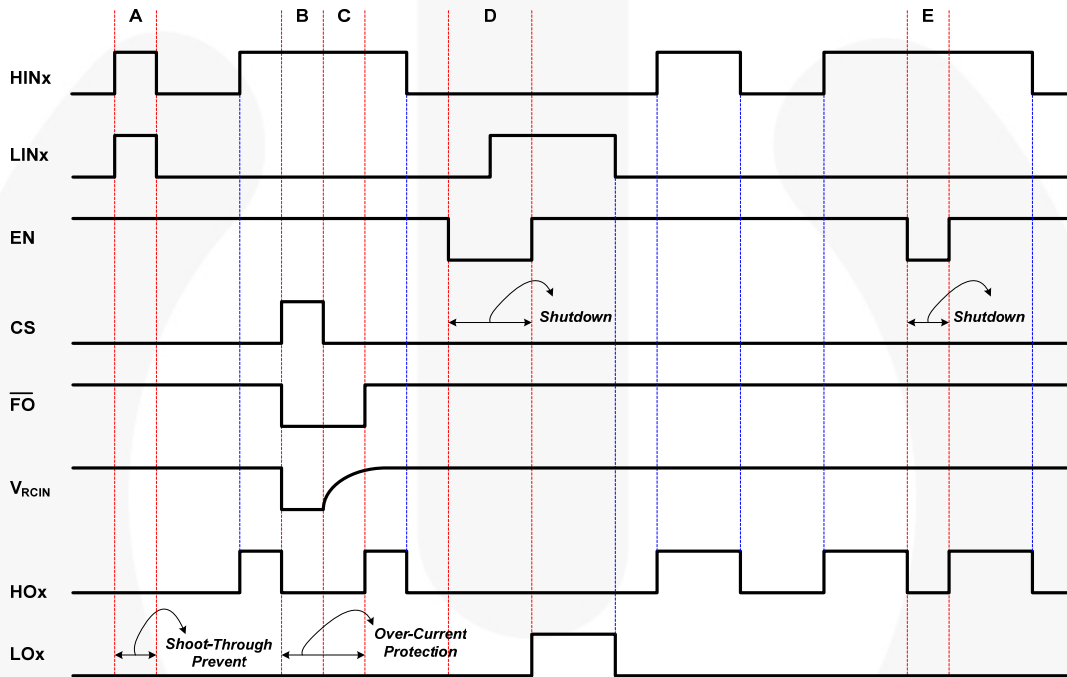


Figure 35. Input / Output Timing Diagram

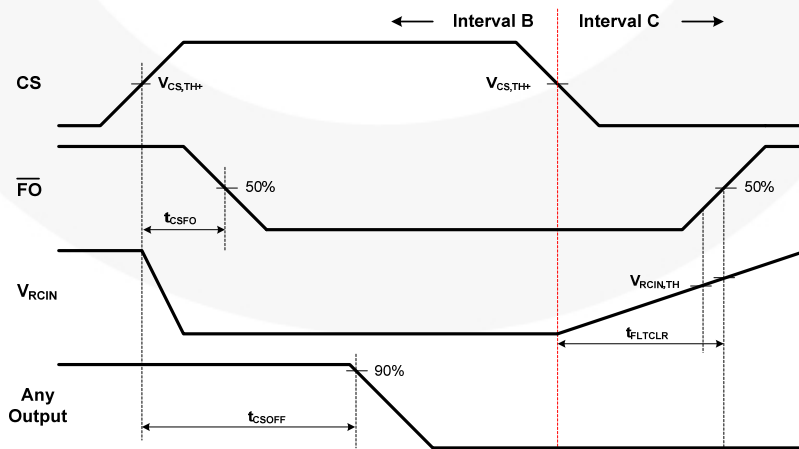


Figure 36. Detailed View of B and C Intervals During Over-Current Protection

Applications Information

1. Dead Time

Dead time is automatically inserted whenever the dead time of the external two input signals (between HINx and LINx signals) is shorter than internal fixed dead times (DT1 and DT2). Otherwise, external dead times larger than internal dead times are not modified by the gate driver and internal dead-time waveform definition is shown in Figure 37.

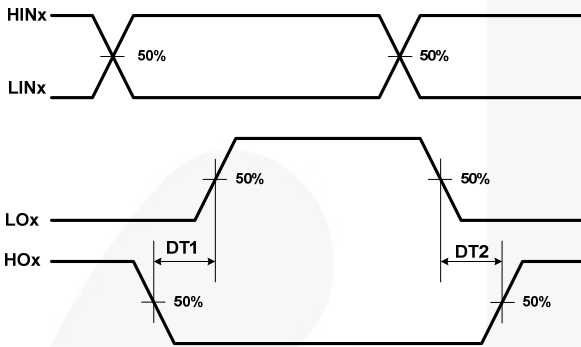


Figure 37. Internal Dead-Time Definitions

2. Protection Function

2.1 Fault Out (\overline{FO}) and Under-Voltage Lockout

The high- and low-side drivers include under-voltage lockout (UVLO) protection circuitry that monitors the supply voltage for V_{DD} and V_{BS} independently. It can be designed to prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage. Also, the UVLO hysteresis prevents chattering during power-supply transitions. Moreover, the fault signal (FO) goes to LOW state to operate reliably during power-on events, when the power supply (V_{DD}) is below the under-voltage lockout high threshold voltage for the circuit (during $t_1 \sim t_2$). The UVLO circuit is not otherwise activated; shown Figure 38.

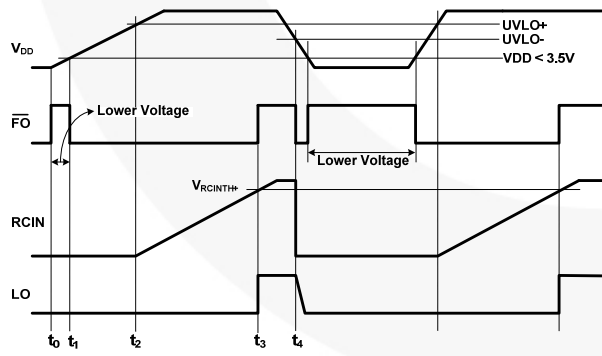
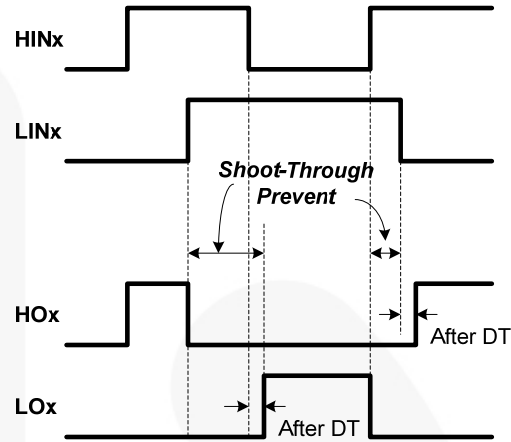


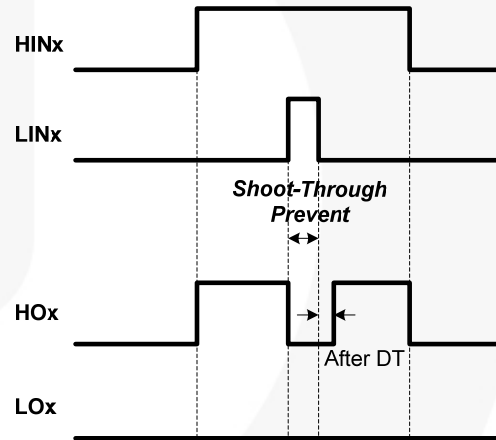
Figure 38. Waveforms for Under-Voltage Lockout

2.2 Shoot-Through Protection

The shoot-through protection circuitry prevents both high- and low-side switches from conducting at the same time, as shown Figure 39.



Example A



Example B

Figure 39. Shoot-Through Protection

2.3 Enable Input

When the EN pin is in HIGH state, the gate driver operates normally. When a condition occurs that should shut down the gate driver, the EN pin should be LOW. The enable circuitry has an input filter; the minimum input duration is specified by t_{FLTIN} (typically 250 ns).

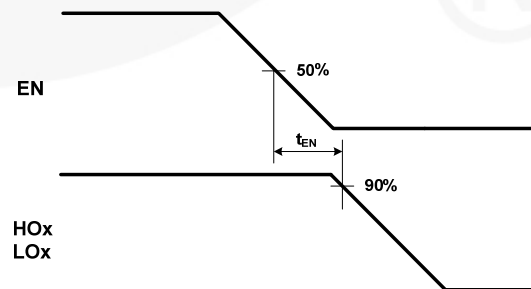


Figure 40. Output Enable Timing Waveform

2.4 Fault-Out (\overline{FO}) and Over-Current Protection

FAN7389 provides an integrated fault output (\overline{FO}) and an adjustable fault-clear timer (t_{FLTCLR}). There are two situations that cause the gate driver to report a fault via the \overline{FO} pin. The first is an under-voltage condition of low-side gate driver supply voltage (V_{DD}) and the second is when the current-sense pin (CS) recognizes a fault. Once the fault condition occurs, the \overline{FO} pin is internally pulled to COM, the fault-clear timer is activated, and all outputs (HO1,2,3 and LO1,2,3) of the gate driver are turned off. The fault output stays LOW until the fault condition has been removed and the fault-clear timer expires. Once the fault-clear timer expires, the voltage on the \overline{FO} pin returns to pull-up voltage.

The fault-clear time (t_{FLTCLR}) is determined by an internal current source ($I_{RCIN}=5\ \mu\text{A}$) and an external C_{RCIN} at the RCIN pin, as shown in this equation:

$$t_{FLTCLR} = \frac{C_{RCIN} \times V_{RCIN,TH}}{I_{RCIN}} \text{ [s]} \quad (1)$$

The R_{DSRCIN} of the MOSFET is a characteristic discharge curve with respect to the external capacitor C_{RCIN} . The time constant is defined by the external capacitor C_{RCIN} and the R_{DSRCIN} of the MOSFET.

The output of current-sense comparator (CS_COMP) passes a noise filter, which inhibits an over-current shutdown caused by parasitic voltage spikes of V_{CS} .

This corresponds to a voltage level at the comparator of $V_{CSTH+} - V_{CSHYS} = 500\ \text{mV} - 60\ \text{mV} = 440\ \text{mV}$, where $V_{CSHYS}=60\ \text{mV}$ is the hysteresis of the current comparator (CS_COMP) as shown in Figure 41.

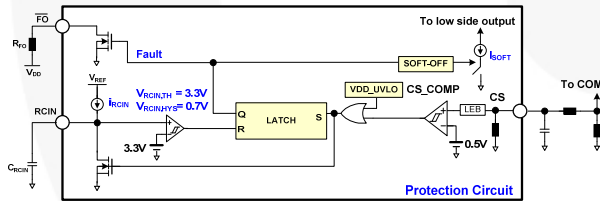


Figure 41. Over-Current Protection

Figure 42 shows the waveform definitions of RCIN, \overline{FO} and the low-side driver, which uses a soft turn-off method when an under-voltage condition of the low-side gate driver supply voltage (V_{DD}) or the current-sense pin (CS) recognizes a fault. Once a fault condition occurs, the \overline{FO} pin is internally pulled to COM and all outputs (HO1,2,3 and LO1,2,3) of the gate driver are turned off. Low-side outputs decline linearly by the internal sink current source ($I_{SOFT}=40\ \text{mA}$) for soft turn-off, as shown in Figure 42.

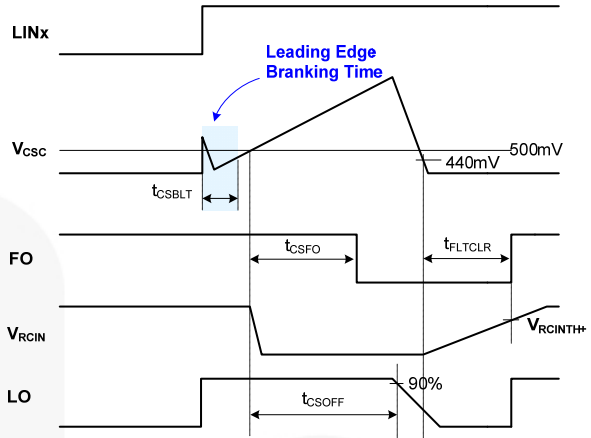


Figure 42. R_{CIN} and Fault-Clear Waveform Definition

2.5 Recommended R_{CIN}

Figure 43 shows timing of t_{CSOFF} and t_{CSFO} versus C_{RCIN} .

It is strongly recommended that the capacitor on R_{CIN} pin should be less than 5 nF in order to properly protect power devices in over-current situations.

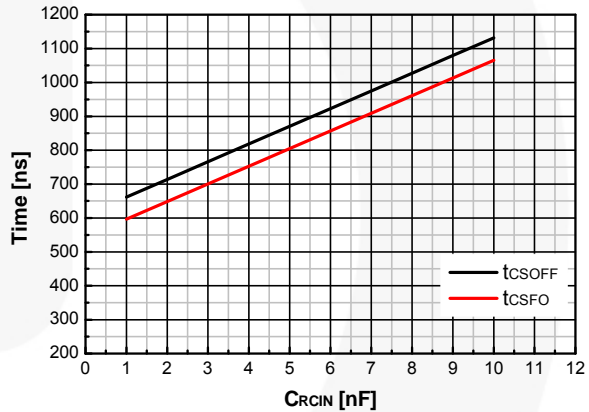


Figure 43. Timing of t_{CSOFF} and t_{CSFO} vs. C_{RCIN}

3. Noise Filter

3.1 Input Noise Filter

Figure 44 shows the input noise filter method, which has symmetry duration between the input signal (t_{INPUT}) and the output signal (t_{OUTPUT}) and helps to reject noise spikes and short pulses. This input filter is applied to the HINx, LINx, and EN inputs. The upper pair of waveforms (Example A) shows an input signal duration (t_{INPUT}) much longer than input filter time (t_{FLTIN}); it is approximately the same duration between the input signal time (t_{INPUT}) and the output signal time (t_{OUTPUT}). The lower pair of waveforms (Example B) shows an input signal time (t_{INPUT}) slightly longer than input filter time (t_{FLTIN}); it is approximately the same duration between input signal time (t_{INPUT}) and the output signal time (t_{OUTPUT}).

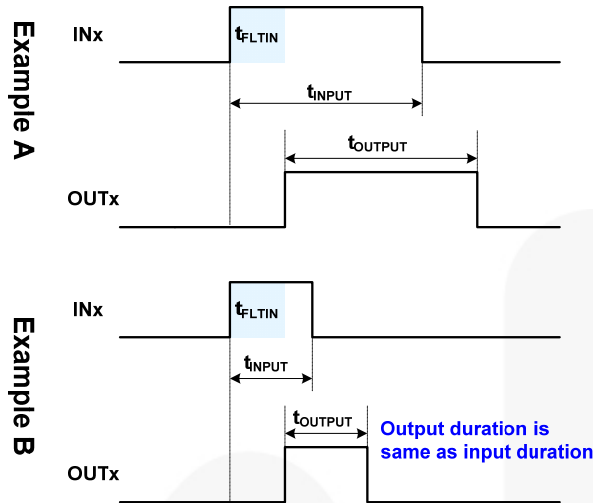


Figure 44. Input Noise Filter Definition

3.2. Short-Pulsed Input Noise Rejection Method

The input filter circuitry provides protection against short-pulsed input signals (H_{INx} , L_{INx} , and EN) on the input signal lines by applied noise signal.

If the input signal duration is less than input filter time (t_{FLTIN}), the output does not change states.

Example A and B of the Figure 45 show the input and output waveforms with short-pulsed noise spikes with a duration less than input filter time; the output does not change states.

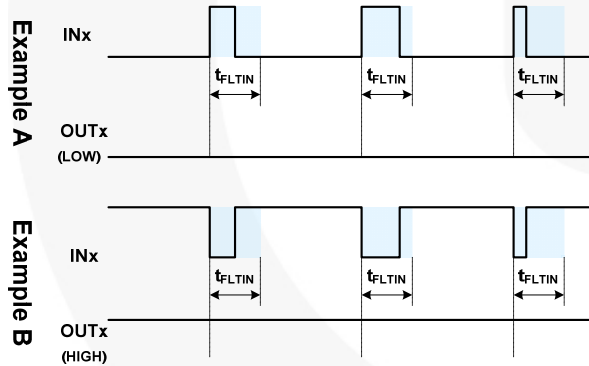


Figure 45. Noise Rejecting Input Filter Definition

Figure 46 shows the characteristics of the input filters while receiving narrow ON and OFF pulses. If input signal pulse duration, PW_{IN} , is less than input filter time, t_{FLTIN} ; the output pulse, PW_{OUT} , is zero. The input signal is rejected by input filter. Once the input signal pulse duration, PW_{IN} , exceeds input filter time, t_{FLTIN} , the output pulse durations, PW_{OUT} , matches the input pulse durations, PW_{IN} . FAN7389 input filter time, t_{FLTIN} , is about 250 ns for the high- and low-side outputs.

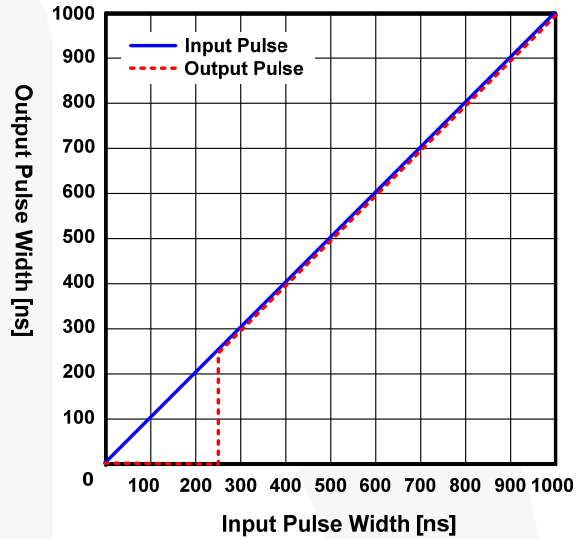
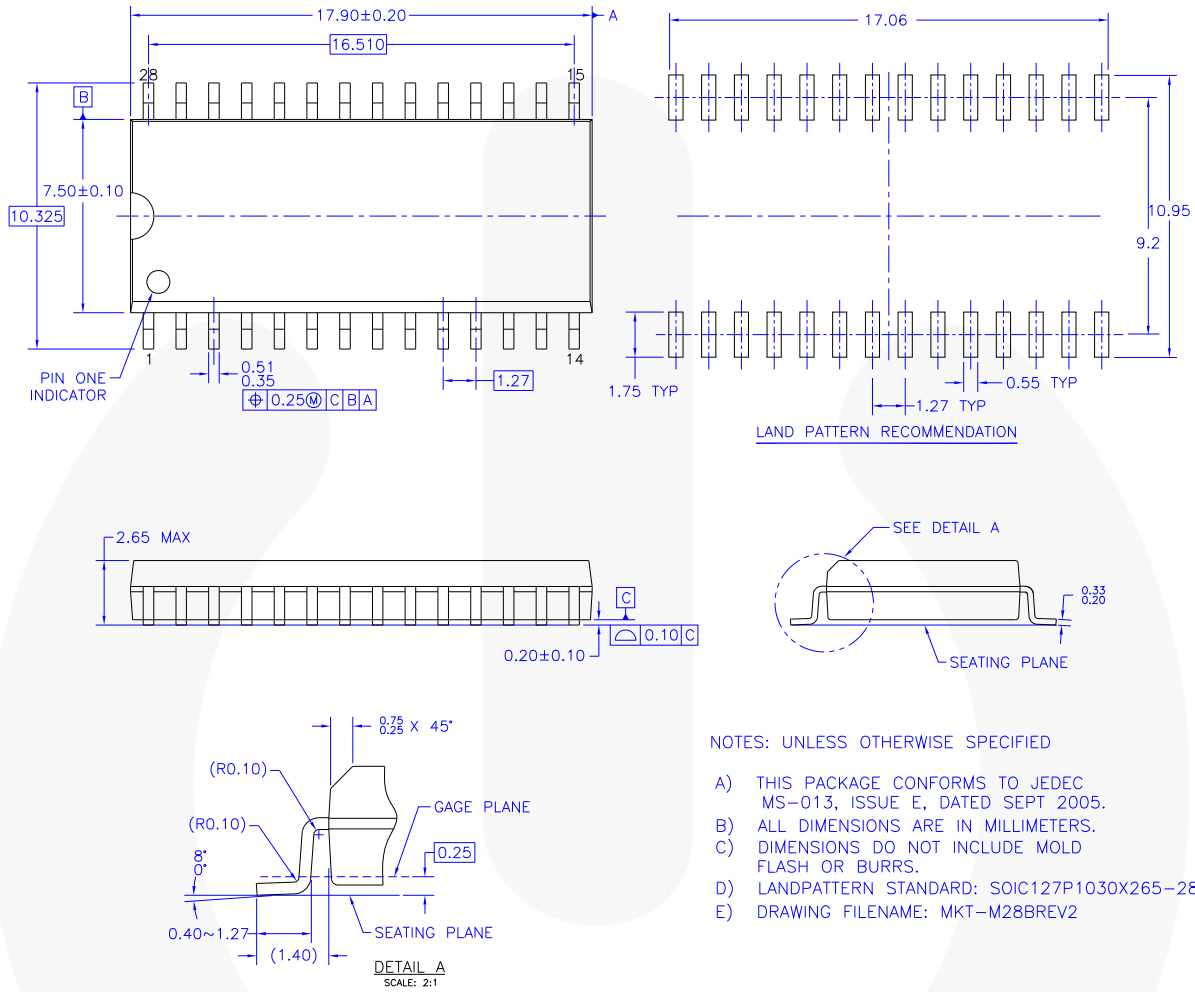


Figure 46. Input Filter Characteristic of Narrow ON

Package Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MS-013, ISSUE E, DATED SEPT 2005.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
 - D) LANDPATTERN STANDARD: SOIC127P1030X265-28L
 - E) DRAWING FILENAME: MKT-M28BREV2

Figure 47.28-Lead Small Outline Integrated Circuit (28-Wide Body SOIC)



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