HY5117404A, HY5116404A

4M x 4-bit CMOS DRAM with Extended Data Out

DESCRIPTION

This family is a 16M bit dynamic RAM organized 4,194,304 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended Data Out mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50,60 or 70ns) and refresh cycle(2K Ref. or 4K Ref.) and package type(SOJ or TSOP-II) and power consumption(Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high band-width, low power consumption and high reliability.

ORDERING INFORMATION

Part Number	Ref.	Power	Pkg.
HY5117404AJ	2K		SOJ
HY5117404ASLJ	2K	SL-part	SOJ
HY5117404AT	2K		TSOP-II
HY5117404ASLT	2K	SL-part	TSOP-II
HY5116404AJ	4K		SOJ
HY5116404ASLJ	4K	SL-part	SOJ
HY5116404AT	4K		TSOP-II
HY5116404ASLT	4K	SL-part	TSOP-II

* Reverse TSOP-II packages are also available

FEATURES

- Part Number Information
  - HY5117404A: 2K Ref.
  - HY5116404A: 4K Ref.
- Max. Active Power Dissipation

Speed	2K	4K
60	660 mW	495 mW
70	550 mW	440 mW
80	495 mW	385 mW

- Fast access time and cycle time

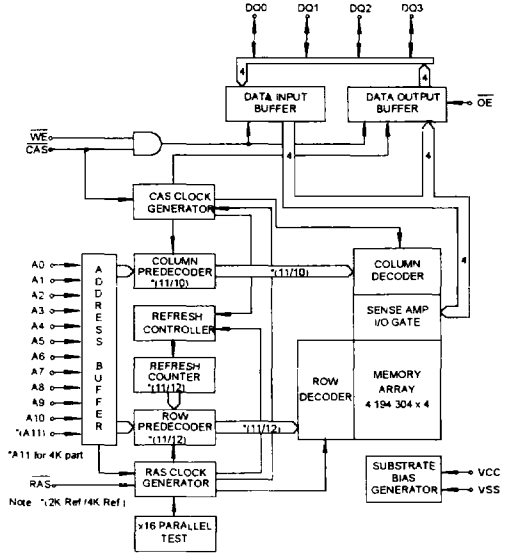
Speed	tRAC	tCAC	tHPC
60ns	60ns	15ns	25ns
70ns	70ns	18ns	30ns
80ns	80ns	20ns	35ns

- Extended Data Out Operation
- Single power supply of 5.0V±10%
- Read-Modify-Write Capability
- Early Write or Output Enable controlled write
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self Refresh Capability
- Refresh cycles

Part No.	Ref.	Normal	SL-part
HY5117404A	2K	32ms	256ms
HY5116404A	4K	64ms	

- JEDEC standard pinout
  24/26-pin Plastic SOJ (300 mil)
  24/26-pin Plastic TSOP-II (300mil)

BLOCK DIAGRAM



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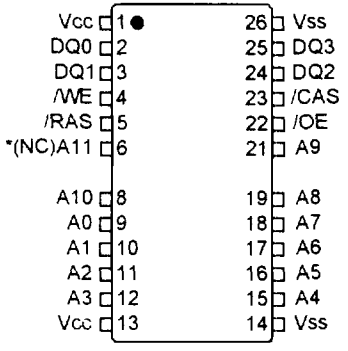
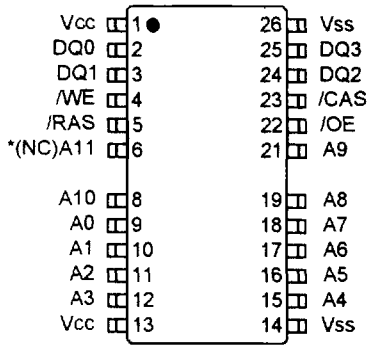
PIN CONFIGURATION (Marking Side)



24/26-pin Plastic SOJ (300mil)



24/26-pin Plastic TSOP-II (300mil)

*(N.C) : For 2K Refresh product

PIN DESCRIPTION

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A11	Address Inputs (4K Product)
A0-A10	Address Inputs (2K Product)
DQ0-DQ3	Data Input/Output
Vcc	Power (+5.0V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin relative to Vss	-1.0 to 7.0	V
V_{CC}	Voltage on Vcc relative to Vss	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	℃ · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0℃to 70℃)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	Vcc+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

Note: All voltages are referenced to Vss.

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DC CHARACTERISTICS

(T_A=0℃to 70℃, Vcc=5.0V ± 10% and Vss=0V, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current 2K Ref	Max. Current 4K Ref	UNIT
I_{CC1}	Operating Current	/RAS and /CAS cycling tRC=tRC (min.)	60 70 80	120 100 90	90 80 70	mA
I_{CC2}	TTL Standby Current	/RAS=/CAS ≥ V_{IH} other inputs ≥ Vss	 SL-part	2 1	2 1	mA
I_{CC3}	/RAS-only Refresh Current	/CAS=V_{IH}, /RAS cycling tRC=tRC (min.)	60 70 80	120 100 90	90 80 70	mA
I_{CC4}	EDO Mode Current	/RAS=V_{IL}, /CAS, Address cycling tHPC=tHPC (min.)	60 70 80	110 90 80	80 70 60	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS≥Vcc-0.2V	 SL-part	1 400	1 400	mA μA
I_{CC6}	/CAS-before-/RAS Refresh Current	/RAS and /CAS cycling tRC=tRC (min.)	60 70 80	120 100 90	90 80 70	mA
I_{CC7}	Battery Back-up Current (SL-part)	tRC=125μs(2K Ref), 62.5μs(4K Ref) /CAS = CBR cycling or 0.2V /OE & /WE=Vcc - 0.2V Address =Vcc-0.2V or 0.2V DQ0-DQ3 =Vcc-0.2V, 0.2V or open	tRAS ≤ 300ns	300	350	μA
			tRAS ≤ 1μs	500	600	μA
I_{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as I_{CC7}		300	300	μA

Symbol	Parameter	Test condition	Min.	Max.	UNIT
I_{LI}	Input Leakage current (Any Input Pin)	Vss ≤ V_{IN} ≤ Vcc + 1.0 All other pins not under test=Vss	-10	10	μA
I_{LO}	Output Leakage current (Any Input Pin)	Vss ≤ V_{OUT} ≤ Vcc /RAS & /CAS at V_{IH}	-10	10	μA
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5.0mA	2.4	-	V

NOTE

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(tRC and tHPC).
2. Specified values are obtained with outputs unloaded.
3. I_{CC} is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=V_{IH} within one EDO mode cycle time tHPC.
4. Only /RAS(max.) = 1μs is applied to refresh of battery backup but tRAS(max.) = 10μs is to applied to normal functional operation.
5. I_{CC5}(max.) = 400μA, Icc7 and Icc8 are applied to SL-part only.

AC CHARACTERISTICS

(T_A=0℃ to 70℃, Vcc=5.0V ± 10% and Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY5117404A / HY5116404A						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	2
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	75	-	85	-	95	-	ns	2
5	tRAC	Access Time from /RAS	-	60	-	70	-	80	ns	5,6,7
6	tCAC	Access Time from /CAS	-	15	-	18	-	20	ns	5,6
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	5,7
8	tCPA	Access Time from Column Precharge	-	35	-	40	-	45	ns	5
9	tCLZ	/CAS to Output Low Impedance	3	-	3	-	3	-	ns	5
10	tCEZ	Out Buffer Turn-Off Delay Time /CAS	3	15	3	18	3	20	ns	8
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	/RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	/CAS Hold Time	45	-	50	-	55	-	ns	
17	tCAS	/CAS Pulse Width	11	10K	14	10K	17	10K	ns	
18	tRCD	/RAS to /CAS Delay Time	20	45	20	52	20	60	ns	6
19	tRAD	/RAS to Column Address Delay Time	15	30	15	35	17	40	ns	7
20	tCRP	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	11
21	tCP	/CAS Precharge Time	10	-	12	-	14	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tRAL	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	9
29	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	9
30	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	
31	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
32	tRWL	Write Command to /RAS Lead Time	15	-	18	-	20	-	ns	
33	tCWL	Write Command to /CAS Lead Time	15	-	18	-	20	-	ns	
34	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	10
35	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	10

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AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HY5117404A / HY5116404A						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	tREF	Refresh Period (2048 cycles)	32	-	32	-	32	-	ms	
		Refresh Period (4096 cycles)	64	-	64	-	64	-	ms	
		Refresh Period (SL-part)	256	-	256	-	256	-	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	11
38	tCWD	/CAS to /WE Delay Time	40	-	45	-	50	-	ns	11
39	tRWD	/RAS to /WE Delay Time	80	-	95	-	105	-	ns	11
40	tAWD	Column Address to /WE Delay Time	50	-	60	-	65	-	ns	11
41	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
44	tCPT	/CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
45	tROH	/RAS Hold Time Reference to /OE	10	-	10	-	10	-	ns	
46	tOEA	/OE Access Time	-	15	-	18	-	20	ns	
47	tOED	/OE to Data Delay Time	15	-	18	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time from /OE	3	15	3	18	3	20	ns	8
49	tOEH	/OE Command Hold Time	15	-	18	-	20	-	ns	
50	tCPWD	/WE Delay Time from /CAS Precharge	55	-	65	-	75	-	ns	11
51	tRHCP	/RAS Hold Time from /CAS Precharge	35	-	40	-	45	-	ns	
52	tWRP	/WE to /RAS Precharge Time(CBR cycle)	10	-	10	-	10	-	ns	
53	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	
54	tRASS	/RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	µs	
55	tRPS	/RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
56	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	
57	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
58	tREZ	Output Buffer Turn Off Delay Time from /RAS	3	15	3	18	3	20	ns	
59	tWEZ	Output Buffer Turn Off Delay Time from /WE	3	15	3	18	3	20	ns	
60	tWED	/WE to Data Delay Time	15	-	18	-	20	-	ns	
61	tOEP	/OE Precharge Time	5	-	5	-	5	-	ns	
62	tWPE	/WE Pulse Width (EDO cycle)	5	-	5	-	5	-	ns	
63	tOCH	/OE to /CAS Hold Time	5	-	5	-	5	-	ns	
64	tCHO	/CAS Hold Time to /OE	5	-	5	-	5	-	ns	

TEST MODE

#	SYMBOL	PARAMETER	HY5117404A / HY5116404A						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	160	-	185	-	205	-	ns	
3	tHPC	EDO Mode Cycle Time	30	-	35	-	40	-	ns	2
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	80	-	90	-	100	-	ns	2
5	tRAC	Access Time from /RAS	-	65	-	75	-	85	ns	5,6,7
6	tCAC	Access Time from /CAS	-	20	-	23	-	25	ns	5,6
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	5,7
8	tCPA	Access Time from Column Precharge	-	40	-	45	-	50	ns	5
13	tRAS	/RAS Pulse Width	65	10K	75	10K	85	10K	ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	65	200K	75	200K	85	200K	ns	
15	tRSH	/RAS Hold Time	20	-	23	-	25	-	ns	
16	tCSH	/CAS Hold Time	50	-	55	-	60	-	ns	
17	tCAS	/CAS Pulse Width	16	10K	19	10K	22	10K	ns	
26	tRAL	Column Address to /RAS Lead Time	35	-	40	-	45	-	ns	
38	tCWD	/CAS to /WE Delay Time	45	-	50	-	55	-	ns	11
39	tRWD	/RAS to /WE Delay Time	85	-	100	-	110	-	ns	11
40	tAWD	Column Address to /WE Delay Time	55	-	65	-	70	-	ns	11
46	tOEA	/OE Access Time	-	20	-	23	-	25	ns	
47	tOED	/OE to Data Delay Time	20	-	23	-	25	-	ns	
49	tOEH	/OE Command Hold Time	20	-	23	-	25	-	ns	
50	tCPWD	/WE Delay Time from /CAS Precharge	60	-	70	-	80	-	ns	11

In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all `1`s or `0`s), the DQ pin indicates a `1`. If they are not equal, the DQ pin indicates a `0`. The 4M x 4 DRAM can be tested in the same way as a 1M x 4 DRAM is tested.

/WE (when in /CAS-before-/RAS cycle) puts the 4Mx4 DRAM into Test Mode and a /CAS-before-/RAS or a /RAS-only refresh cycle put it back into Normal Mode. /WE (when in /CAS-before-/RAS cycle) shall be used for the refresh operation in the test mode. The Test Mode function reduces test time(1/4 in case of N test pattern).

NOTE

1. An initial pause of 200 μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2. tASC ≥ tCP(min.), assume tT=2ns
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA = 0 to 70℃) is assured.
5. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 2 TTL loads and 100pF.
6. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC
7. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA
8. tCEZ(max.), tOEZ(max.), tREZ(max.) and tWEZ(max.) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
9. Either tRCH or tRRH must be satisfied for a read cycle..
10. These parameters are referred to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
11. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tCWD ≥ tCWD(min.), tRWD ≥ tRWD(min.) and tCPWD ≥ tCPWD(min.), then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
12. If /RAS goes to high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going. If /CAS goes to high before /RAS high going, the open circuit condition of the output is achieved by /RAS high going.

CAPACITANCE

(T_A=25℃, Vcc=5.0V ± 10%, Vss=0V and f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0 - A11)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input /Output Capacitance (DQ0 - DQ3)	-	7	pF