VECTRON INTERNATIONAL
A DOVER COMPANY

TM-096

Integrated Stratum 3E Timing Solution

Product Brief

The TM-096 Integrated Timing Module is based on a digital PLL that performs filtering of the selected input signal and then synchronizes the signal to an onboard Stratum 3E OCXO. The synchronized signal is then passed through an analog PLL with an integrated VCXO in order to deliver 3 high quality output signals. Configuration and monitoring of the module's operation is achieved via an SPI interface.

The operating modes of the TM-096 include: 1) free-run, 2) holdover, and 3) locked. In the free-run mode the timing module locks to the on-board OCXO. In the holdover mode, the TM-096 generates outputs based upon its most recent input signal lock history. For the locked mode, the DPLL locks onto one of 8 input reference clocks. Selection of the reference can be automatic or manual.

The TM-096 supports both Master and Slave operation. A typical application for the TM-096 would include two modules whereby one unit is configured as a master clock and the other serves as a backup or redundant clock.

A number of external hardware pins are provided for configuration and alarm purposes. The TM-096 is also equipped with a JTAG interface for factory programming and testing.

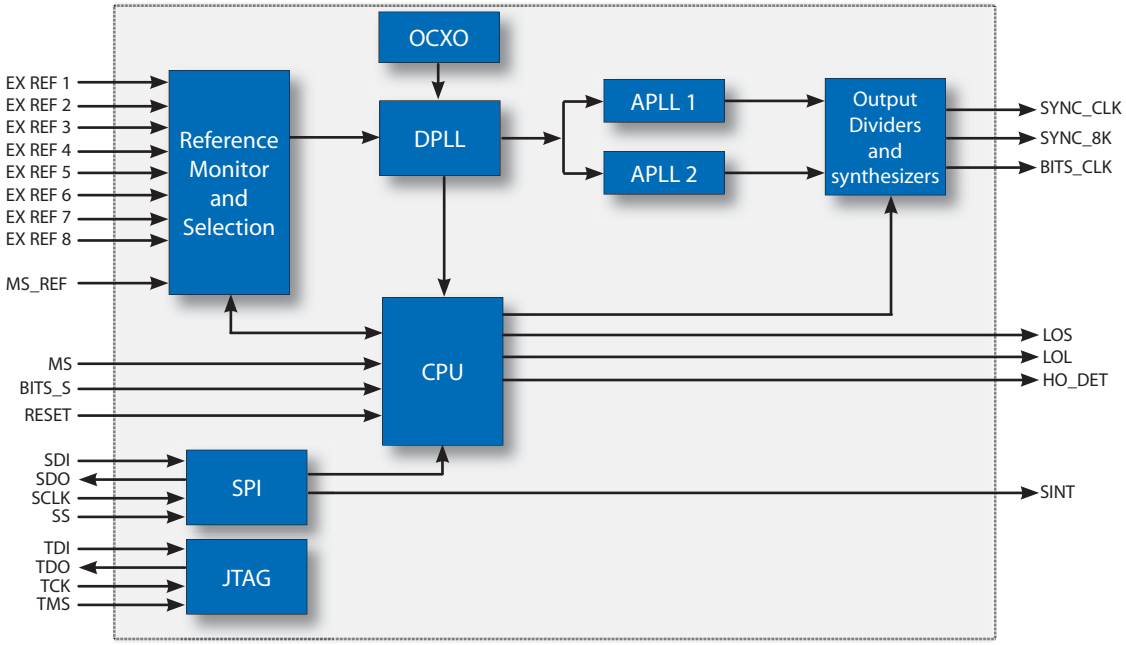
Applications

- Multiservice Switches/Routers
- Add/Drop Multiplexers (ADMs)
- IP and ATM Core Switches
- SONET/SDH
- DWDM
- Synchronous Ethernet

Features

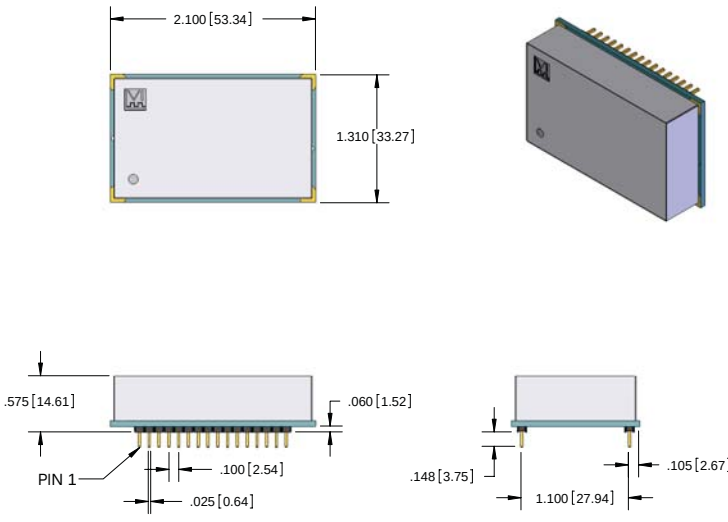
- Single module for stratum 3E clock synchronization
- Complies with Telcordia/ITU-T recommendations
- Free-Run, holdover, and locked operating modes
- Accepts 8 reference inputs
- Generates 3 output clocks
- Hit-less reference switching
- Master or slave configuration
- Supports serial peripheral interface (SPI)
- IEEE 1149.1 JTAG standard test access port
- Single 3.3V operation
- 2.05 x 1.25 x 0.76 package size
- RoHS/Lead free compliant

Block Diagram



REV. 1

Outline Drawing



Specifications

Parameter	Specifications
Voltage	+3.3 VDC
Power	<1 A during warm up, < 500 mA steady state
Input Signals	
Number of input references	8
Reference 1-8 frequency range	8kHz - 77.76MHz
Signal level	LVCMOS
Time reference characteristics	Telcordia: GR-1244-CORE 3.2.1. R3-1
Output Signals	
Number of output signals	3
Output 1 (Sync_Clk)	1.544 to 77.76MHz
Output 2 (Sync_8k)	8kHz
Output 3 (BITS_Clk)	1.544 or 2.048MHz
Signal level	LVCMOS
Input and Output Reference Signal Characteristics	
Input signal	Telcordia: GR-1244-CORE 3.2.1
Jitter tolerance	Telcordia: GR-1244-CORE 4.2, GR-253-CORE 5.4.4.3.6
Phase transient tolerance	Telcordia: GR-1244-CORE 4.4
Wander generation	Telcordia: GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2
Wander tolerance	Telcordia: GR-1244-CORE 4.3
Wander transfer	Telcordia: GR-1244-CORE 5.3, GR-253-CORE 5.4.4.2.4
MTIE	Telcordia: GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2
TDEV	Telcordia: GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2
Phase transients	Telcordia: GR-1244-CORE 5.6, GR-253-CORE 5.4.4.3.3
Jitter generation	Telcordia: GR-1244-CORE 5.5, GR-253-CORE 5.6.2.3
Jitter transfer	Telcordia: GR-1244-CORE 5.5, GR-253-CORE 5.6.2.1
DPLL Performance	
Free run accuracy	$\leq \pm 4.6$ppm
Holdover stability	$\leq \pm 1.2 \times 10^{-8}$ (Stratum 3E)
Pull in range	$\geq \pm 17$ppm
Lock time	$\leq$ 100s (Stratum 3E)
Lock accuracy	$\leq 1 \times 10^{-11}$ (Average 24hr)

Pin Out

Pin#	Symbol	I/O	Function
1	LOS	O	Loss of Signal Alarm
2	LOL	O	Loss of Lock Alarm
3	MS_REF	I	Master/Slave Reference Input
4	REF1	I	Reference Input Signal 1
5	REF2	I	Reference Input Signal 2
6	REF3	I	Reference Input Signal 3
7	REF4	I	Reference Input Signal 4
8	TDI	I	JTAG Test Data Input
9	TMS	I	JTAG Test Mode Select
10	TRST	I	JTAG Test Reset
11	BITS_CLK	O	Output 3 - Synchronous BITS Clock (Either 1.544 or 2.048 MHz)
12	SYNC_8K	O	Output 2 - Synchronous Mast/Slave 8 kHz Clock
13	SYNC_CLK	O	Output 1 - Synchronous Primary Clock
14	NC		No Connect
15	REF5	I	Reference Input Signal 5
16	REF6	I	Reference Input Signal 6
17	REF8	I	Reference Input Signal 8
18	REF7	I	Reference Input Signal 7
19	NC		No Connect
20	BITS_S	I	BITS_CLK Select Input (1 = 1.544MHz, 0 = 2.048MHz)
21	HO_DET	O	Holdover Detect (1 = holdover available)
22	TDO	O	JTAG Test Data Output
23	TCLK	I	JTAG Test Clock
24	GND		Case Ground
25	SCLK	I	SPI Serial Clock Input
26	SDI	I	SPI Serial Data Input
27	VCC	I	+3.3 V Supply Voltage
28	SS	I	SPI Slave Select (Active Low enables SPI port)
29	RESET	I	TM-096 Reset (Active Low, 10 ms hold time minimum)
30	SDO	O	SPI Serial Data Output
31	SINT	O	SPI Interrupt (Active Low)
32	MS	I	Master Select (1 = Master, 0 = Slave)

Ordering Information

TM-096-DAC-B-SNNNN*

TM-096 = Timing Module in 2.05" x 1.25" x 0.76" package, D = 3.3V ±5%, A = LVCMOS output, C = 0° to 70°C,
B = Stratum 3E, SNNNN* = unique alpha-numeric code assigned at time of order designating customers output frequencies.
Please specify Out1 (1.544 – 77.76 MHz) and Out3 (1.544 or 2.048 MHz).

Version Change Notes

Version	Date	Note
1.0	11/29/2007	Pre-release

Product status and specifications are subject to change.