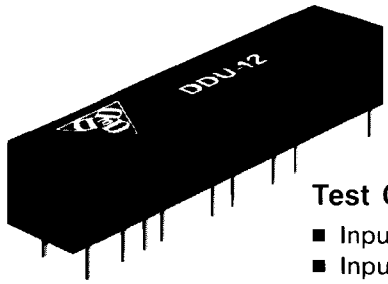
Digital Delay Units

SERIES DDU-12 — 10 Taps ECL Interfaced

data delay devices, inc.



Features:

- **Input & Output ECL Buffered**
- **10 Equally Spaced Taps**
- **PC Board Economy Achieved**

Specifications:

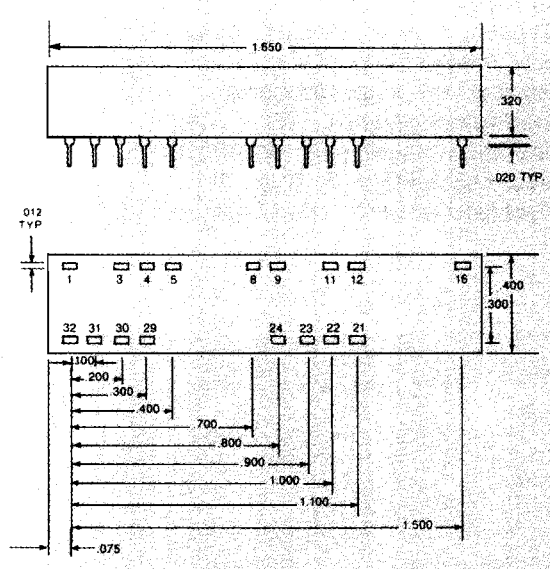
- **Total Delay Tolerance:** ± 5% or better, or 2 ns whichever is greater.
- **No. Taps:** 10 equally spaced.
- **Rise-time:** 2 ns typical.
- **Supply voltage:** 5.2V
- **Operating Temperature:** 30 C to 85 C.
- **Power Dissipation:** 400 mw typ. (no load).
- **Temperature coefficient:** 100 PPM/ C.
- **DC Parameters:** See ECL-10K Logic Table on Page 6.

Test Conditions:

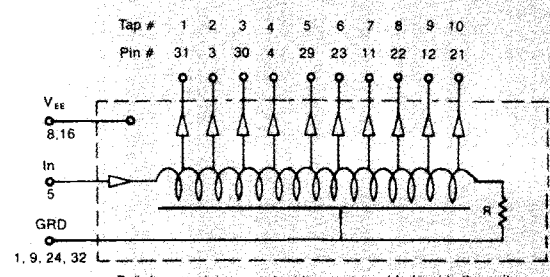
- Input pulse-width: 150% of total delay.
- Input pulse rise-time: 6 ns.
- Input pulse voltage: .7V
- Rise-time measured from 20% to 80% of leading edge.
- Delay time measured at 50% of leading edge.
- All measurements taken @ V_{EE} = 5.2V and T_A = 25 C.
- Unless otherwise specified, all time-delays are referenced to the input pin.

Part No.	Total Delay (ns)	Tap Delay (ns)
* DDU-12-10	9	1 ± .3
* DDU-12-20	18	2 ± .4
* DDU-12-25	22.5	2.5 ± .4
DDU-12-40	40	4 ± .5
DDU-12-50	50	5 ± 1.0
DDU-12-75	75	7.5 ± 1.5
DDU-12-100	100	10 ± 2.0
DDU-12-150	150	15 ± 2.0
DDU-12-200	200	20 ± 2.0
DDU-12-250	250	25 ± 2.0
DDU-12-300	300	30 ± 2.0
DDU-12-400	400	40 ± 2.0
DDU-12-500	500	50 ± 2.5
DDU-12-750	750	75 ± 4.1
DDU-12-1000	1000	100 ± 5.0
DDU-12-1500	1500	150 ± 7.0

*Time delay measurements referenced to 1st tap.
3 ns ± 1 ns inherent delay.



† or case stand-offs



Pull-down resistor on output taps not provided inside the unit.

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