RICOH

R5101G SERIES

Microprocessor power management with Watchdog Timer

NO. EA-071-100128

OUTLINE

The R5101G Series are CMOS-based µ con power management ICs with high accuracy output voltage and detector threshold and with ultra low supply current. Each of these ICs consists of a voltage regulator, a voltage detector and a watchdog timer. Thus, the R5101G Series have the function of a power management for microprocessor, a monitor of the voltage of a power source and a microprocessor supervisor.

The built-in voltage regulator with an internal driver transistor can supply typically 50mA current to a system when the voltage difference between input and output is 2V. Therefore these ICs are very suitable for various power supply systems for microprocessors. The output voltage is monitored by the voltage detector which is built-in these ICs.

The built-in voltage detector has an output delay function and the delay time can be set by an external capacitor (C_D).

The output voltage and the detector threshold voltage can be set individually for each IC by laser trimming.

Furthermore, when a microprocessor works incorrectly, the watchdog timer which checks over microprocessor generates reset signals intermittently to prevent a whole system from being malfunction.

The timeout periods for watchdog and reset can also be set individually by an external capacitor (C_{TW}).

FEATURES

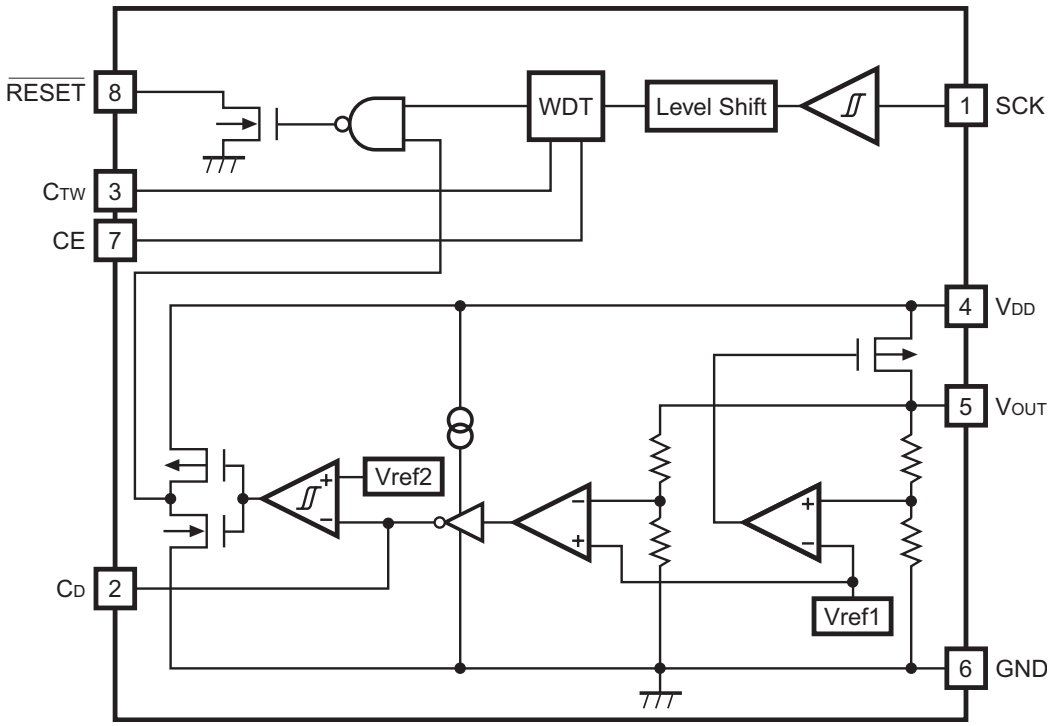
- Built-in a watchdog timer
- Timeout period for watchdog and generating a reset signal can be set by an external capacitor
- Watchdog timer can be stopped individually by CE Pin
- Supply current..... Typ. 5µA
- The output voltage of Voltage Regulator and the detector threshold voltage can be set individually with a step of 0.1V for each IC by laser-trim.
- High Accuracy Output Voltage of Voltage Regulator and Detector Threshold ·····±2.5%
- Power-on Reset Delay Time can be set by an external capacitor
- Output Current..... Typ. 50mA (at V_{IN}–V_{OUT}=2V)
- Package..... SSOP-8G

APPLICATIONS

- Power source for microprocessors

BLOCK DIAGRAMS

R5101GxxxA



SELECTION GUIDE

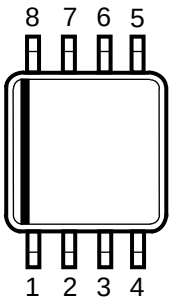
The output voltage and the detector threshold for the ICs can be selected at the users' request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5101GxxxA-TR	SSOP-8G	3,000 pcs	Yes	Yes

xxx: The combination of output voltage and detector threshold for each channel can be designated by serial numbers.
(For details, please refer to MARK INFORMATIONS.)

PIN CONFIGURATION

● **SSOP-8G**



PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	SCK	Clock Input Pin from Microprocessor
2	C_D	External Capacitor Pin for Setting Delay Time of Voltage Detector
3	C_{TW}	External Capacitor Pin for Setting Reset and Watchdog Timeout Periods
4	V_{DD}	Power supply Pin
5	V_{OUT}	Output Pin for Voltage Regulator
6	GND	Ground Pin
7	CE	Control Switch Pin for Watchdog timer ("H" active, "L" inactive)
8	$\overline{\text{RESET}}$	Output Pin for Reset signal of Watchdog timer and Voltage Detector. (Output Type is Nch Open Drain, Output "L" at detecting Detector Threshold and Watchdog Timer Reset.)

ABSOLUTE MAXIMUM RATINGS

Topt=25°C, V_{SS}=0V

Symbol	Item		Rating	Unit
V_{DD}	Supply Voltage		−0.3 to 12	V
V_{CD}	Output Voltage	Voltage of C_D Pin	V_{SS}−0.3 to V_{DD}+0.3	V
V_{CTW}		Voltage of C_{TW} Pin	V_{SS}−0.3 to V_{DD}+0.3	V
V_{OUT}		Voltage of V_{OUT} Pin	V_{SS}−0.3 to V_{DD}+0.3	V
$V_{\overline{RESET}}$		Voltage of $\overline{RESET}$ Pin	V_{SS}−0.3 to 12	V
V_{CE}	Input Voltage	Voltage of CE Pin	V_{SS}−0.3 to V_{DD}+0.3	V
V_{SCK}		Voltage of SCK Pin	V_{SS}−0.3 to V_{DD}+0.3	V
I_{OUT}	Output Current	Current of V_{OUT} Pin	150	mA
$I_{\overline{RESET}}$		Current of $\overline{RESET}$ Pin	10	mA
P_D	Power Dissipation (SSOP-8G)*		380	mW
Topt	Operating Temperature Range		−40 to 85	°C
Tstg	Storage Temperature Range		−55 to 125	°C

∗) For Power Dissipation, please refer to PACKAGE INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings is not assured.

ELECTRICAL CHARACTERISTICS

- **R5101GxxxA**

Topt=25°C

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage			1.5		10	V
I_{SS}-On	Supply Current (WDT active)	V_{DD}=CE=V_{OUT}+2.0V			5	15	µA
I_{SS}-Off	Supply Current (WDT inactive)	V_{DD}=V_{OUT}+2.0V, CE=GND			6	18	µA
V_{OUT}	Output Voltage	V_{DD}=V_{OUT}+2.0V, I_{OUT}=10mA		×0.975		×1.025	V
I_{OUT}	Output Current[*1]	V_{DD}=V_{OUT}+2.0V		50			mA
V_{DIF}	Dropout Voltage	Refer to the following table					
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{DD}=V_{OUT}+2.0V, 1mA≤I_{OUT}≤30mA (In case that 3.0V≤V_{OUT}≤5.0V, 1mA≤I_{OUT}≤50mA)			50	100	mV
$\Delta V_{OUT}/\Delta V_{DD}$	Line Regulation	I_{OUT}=10mA V_{OUT}+0.5V≤V_{DD}≤10V			0.1	0.2	%/V
I_{LIM}	Current Limit (Short mode)	V_{OUT}=GND		10	50	100	mA
$\Delta V_{OUT}/\Delta Topt$	Output Voltage Temperature Coefficient	I_{OUT}=10mA -40°C≤Topt≤85°C			±100		ppm/°C
$-V_{DET}$	Detector Threshold			×0.975		×1.025	V
V_{HYS}	Hysteresis Range			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.07	V
V_{DETMGN}	Regulator Voltage Margin against Released Voltage	V_{OUT}-((-V_{DET})+V_{HYS}), I_{OUT}=10mA		0.02			V
$\Delta-V_{DET}/\Delta Topt$	Detector Threshold Temperature Coefficient	-40°C≤Topt≤85°C			±100		ppm/°C
t_{PR}	Reset Delay Time	V_{DD}=V_{OUT}+2.0V, C_D=0.001µF		7	14	35	ms
t_{WD}	Watchdog Timeout period	V_{DD}=V_{OUT}+2.0V, C_W=0.01µF		50	120	250	ms
t_{WR}	Reset Hold Time of WDT	V_{DD}=V_{OUT}+2.0V, C_W=0.01µF		5	12	25	ms
V_{IHSCK}	SCK Input Voltage "H"	V_{DD}=V_{OUT}+2.0V		0.8 ×V_{OUT}		V_{DD}	V
V_{ILSCK}	SCK Input Voltage "L"	V_{DD}=V_{OUT}+2.0V	1.8V≤V_{OUT}≤2.9V	0		0.1 ×V_{OUT}	V
			3.0V≤V_{OUT}≤5.0V	0		0.2 ×V_{OUT}	
V_{IHCE}	CE Input Voltage "H"			1.2		V_{DD}	V
V_{ILCE}	CE Input Voltage "L"			0.0		0.2	V
I_{IHSCK}	SCK Input Current "H"	V_{DD}=SCK=V_{OUT}+2.0V		-1		1	µA
I_{ILSCK}	SCK Input Current "L"	V_{DD}=V_{OUT}+2.0V, SCK=GND		-1		1	µA
R_{PU}	CE Pull-up Resistance			2	4	10	MΩ
I_{CD}	C_D Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V		1	2		mA
I_{CTW}	C_{TW} Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V		1	2		mA
$I_{\overline{RESET}}$	$\overline{RESET}$ Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V		1	2		mA
Ileak	$\overline{RESET}$ Pin Leakage Current	V_{DD}=10.0V, CE=GND, V_{DS}=10.0V		-1		1	µA

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
T_{SCKW}	SCK Input Pulse Width	$V_{DD}=V_{OUT}+2.0V$	500			ns
Vstart	Minimum Operating Voltage of Voltage Detector			0.9	1.5	V

∗1) In case that V_{OUT}<2V, please use I_{OUT} with 0.1mA or more.

- **Dropout Voltage by Output Voltage**

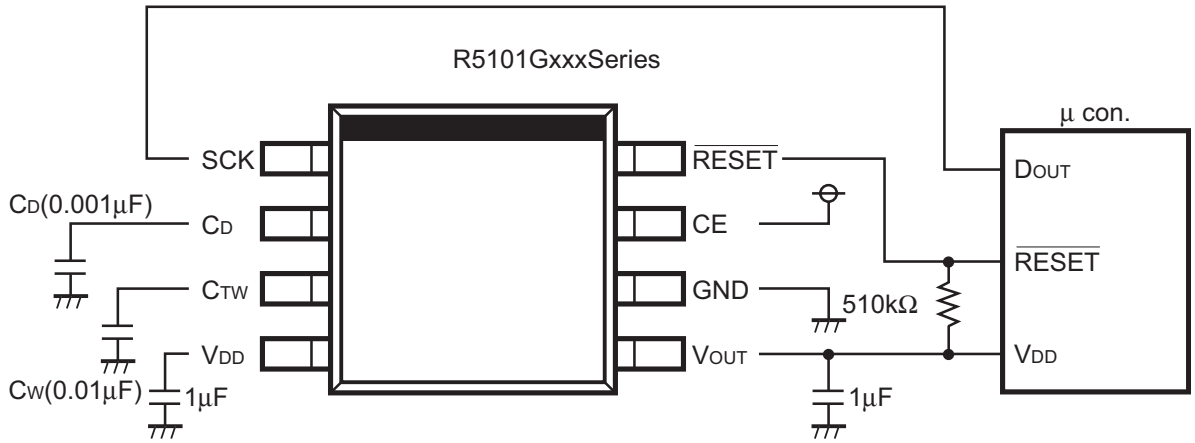
Topt=25°C

Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (V)			
	Condition	Min.	Typ.	Max.
1.8 ≤ V_{OUT} ≤ 2.9	I_{OUT}=10mA	0.100	0.350	0.650
3.0 ≤ V_{OUT} ≤ 3.9	I_{OUT}=30mA	0.100	0.500	0.850
4.0 ≤ V_{OUT} ≤ 5.0		0.100	0.350	0.650

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

TYPICAL APPLICATIONS



TECHNICAL NOTES

The minimum value of the operation margin for releasing the voltage detector is specified as 0.02V.

This IC is sensing the output voltage of the regulator of this IC itself, and depending on the input voltage transient or load transient, the operation margin may be disappeared.

The power line noise may cause a mis-operation of the watchdog timer, therefore V_{DD} and GND lines must be sufficient enough for avoiding the mis-operation.

If the power line has some noise, the output of the regulator of this IC may generate the noise, in such a case, the built-in detector may detect the output noise of the voltage regulator and $\overline{\text{RESET}}$ signal may output.

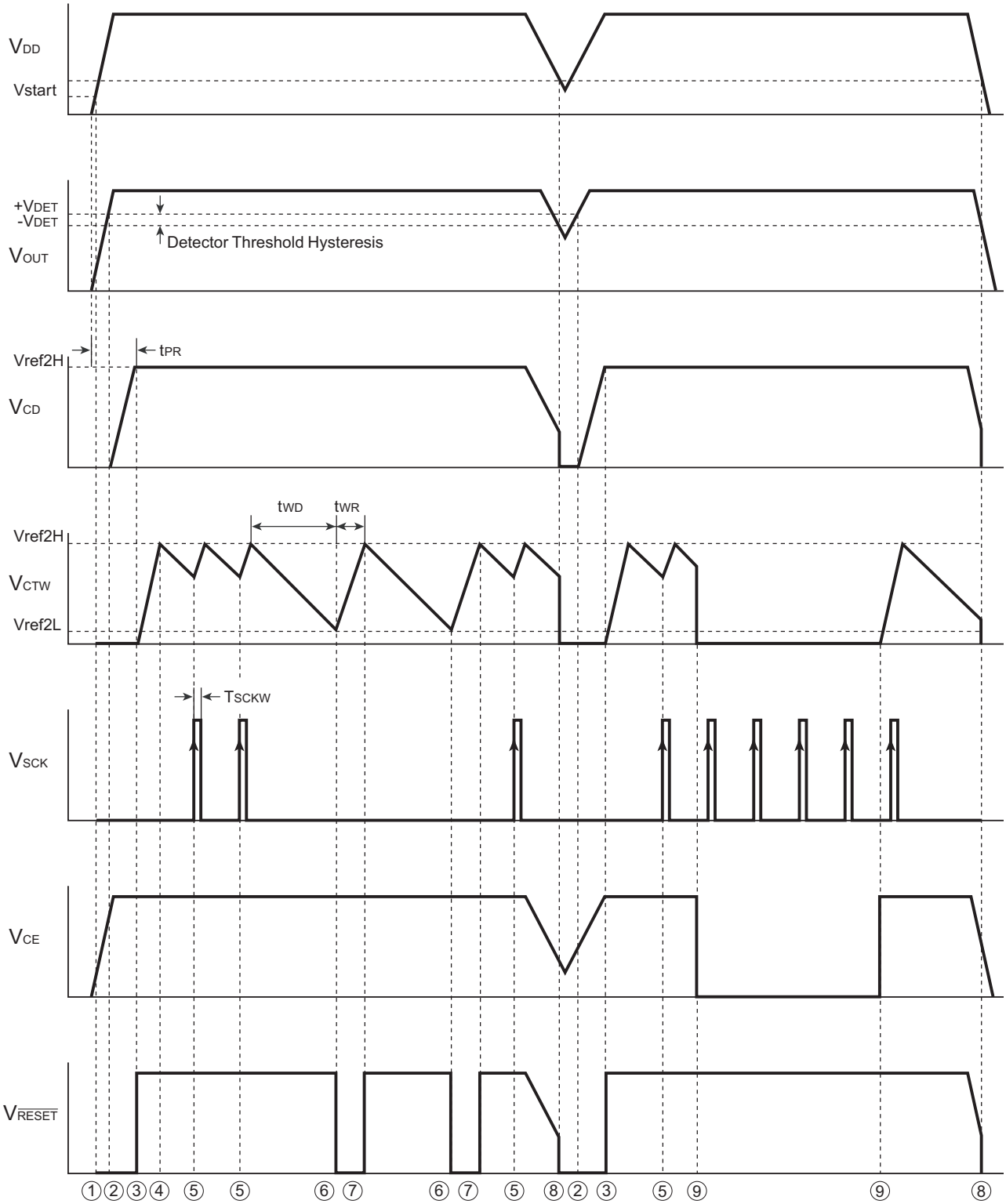
To prevent the IC from this kind of mis-operation, we recommend using a capacitor in the capacitance range from 1μF to 2.2μF between V_{OUT} pin and GND pin.

To avoid the mis-operation, during watchdog timer monitoring time, there is some ignoring time against clock pulse. Therefore, during the ignoring time, input clock pulse (rising edge trigger) is ignored. The ignoring time is approximately as follows:

1) The time interval for V_{CTW} pin voltage from Vref2H to (Vref2H-Vref2H/20)

2) The time interval for V_{CTW} pin voltage from Vref2L+Vref2L/20 to Vref2L

TIMING CHART



OPERATION

① When V_{DD} is turned on and Input Voltage reaches Vstart (nearly equal 0.8V), the output of $\overline{\text{RESET}}$ pin becomes "L" level.

② An External Capacitor starts to be charged through the C_D pin when an Output Voltage of the Voltage Regulator, V_{OUT}, crosses the Released Voltage, $+V_{DET}$, from Lower to Higher. The $V_{\overline{\text{RESET}}}$ is kept "L" level until Voltage of the C_D pin, V_{CD}, reaches to the Vref2H, and after that the $V_{\overline{\text{RESET}}}$ becomes to "H" level.

* t_{PR}: Time interval between the timing of starting edge of forcing voltage to V_{DD} pin and the timing of reverse the voltage level of $V_{\overline{\text{RESET}}}$.
  t_{PR} can be set by connecting an external capacitor to C_D pin, t_{PR} can be calculated as shown below;
  t_{PR}(ms) ≈ 14000× C_D(µF); C_D means a value of an external capacitor connected to C_D pin.

③ When the voltage level of V_{CD} reaches to the Vref2H, the external capacitor starts to be charged through the C_{TW} pin and the watchdog timer begins to operate.

④ The operation mode for the external capacitor changes from charging mode to discharging mode through C_{TW} pin when the voltage level of C_{TW} pin, V_{CTW}, reaches to the Vref2H.

⑤ While the C_{TW} pin is on the discharging mode, if a clock pulse is entered (synchronous with a rising edge of the pulse), the operation mode of C_{TW} pin changes from discharging mode to charging mode. And the external capacitor connected to C_{TW} pin is charged until its voltage level reaches to Vref2H.

⑥ While the C_{TW} pin is on the discharging mode, if V_{CTW} level drops to Vref2L without clock pulse to CLK pin, the voltage level of $\overline{\text{RESET}}$ pin becomes from "H" to "L".

* Watchdog Timeout period, t_{WD},: Discharging Time of C_{TW} pin level from Vref2H to Vref2L
  t_{WD} can be set by connecting an external capacitor to C_W pin, t_{WD} can be calculated as shown below;
  t_{WD} (ms) ≈ 12000× C_W (µF); C_W means a value of an external capacitor connected to C_W pin.

⑦ C_{TW} pin is changed to charging mode from discharging mode when the Reset signal is generated.

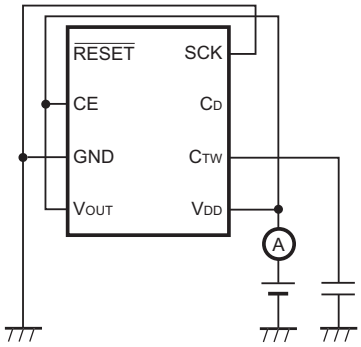
* Reset timeout period of the watchdog timer, t_{WR},: Time interval between Charging time of the C_{TW} pin from Vref2L to Vref2H. t_{WR} can be calculated by the next equation as shown below;
  t_{WR} (ms) ≈ t_{WD}/10

⑧ The Output Voltage level of $\overline{\text{RESET}}$ pin becomes from "H" to "L", or a Reset signal is generated when an output voltage of the Voltage Regulator drops to a level at equal or less than $-V_{DET}$.

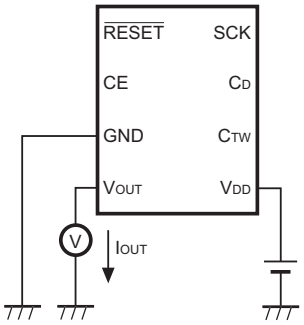
⑨ The watchdog timer will be halted when a Voltage level of CE pin becomes to "L". In this case, only the watchdog timer is stopped and monitoring the output voltage is continued. After that, if the voltage level of CE pin becomes to "H", C_{TW} pin starts to be on charging mode.

TEST CIRCUIT

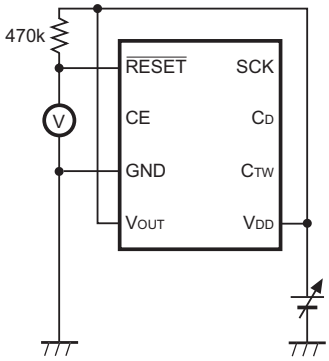
Supply Current Test Circuit



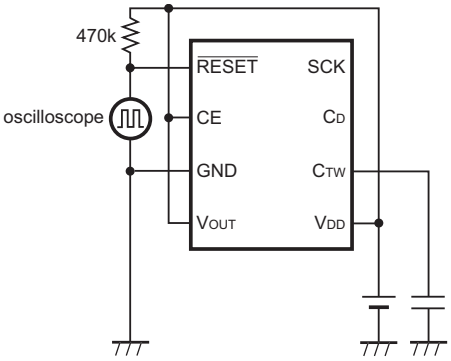
Output Voltage Test Circuit



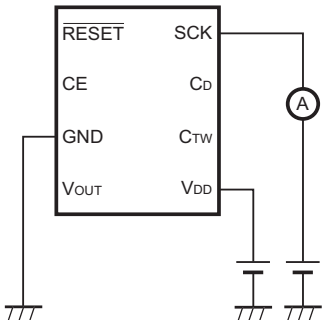
Detector Threshold(V_{DET}) Test Circuit



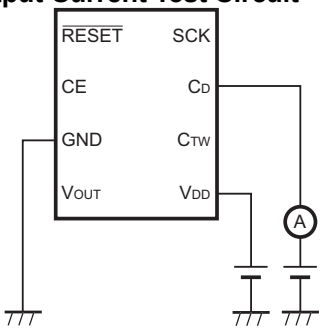
Reset and Watchdog Timeout Periods Test Circuit



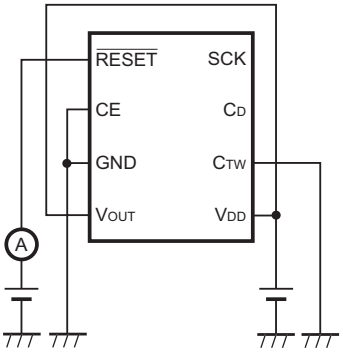
SCK Input Current Test Circuit



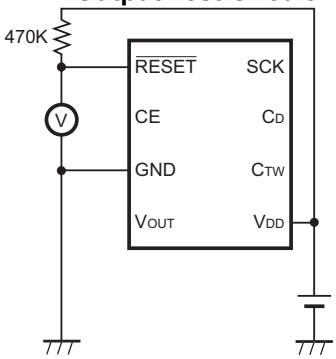
Output Current Test Circuit



RESET Output leakage Current Test Circuit



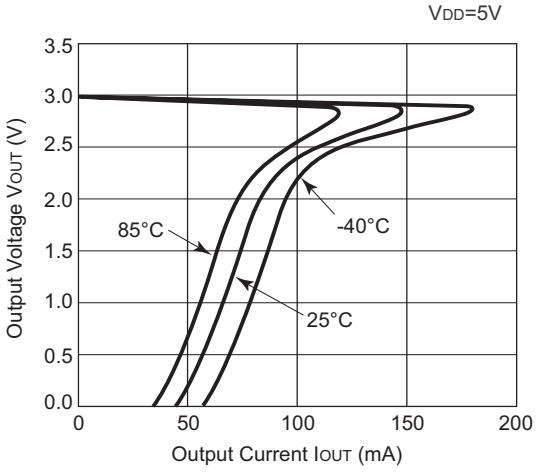
Minimum Input Voltage for RESET Output Test Circuit



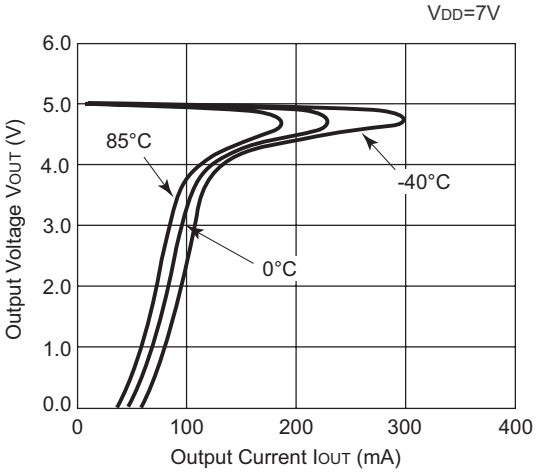
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current

R5101G (VR=3V)

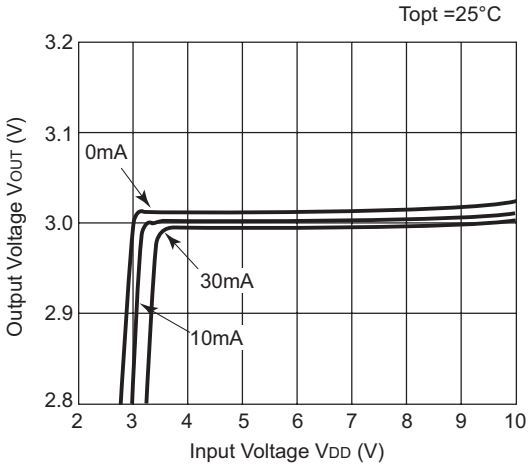


R5101G (VR=5V)

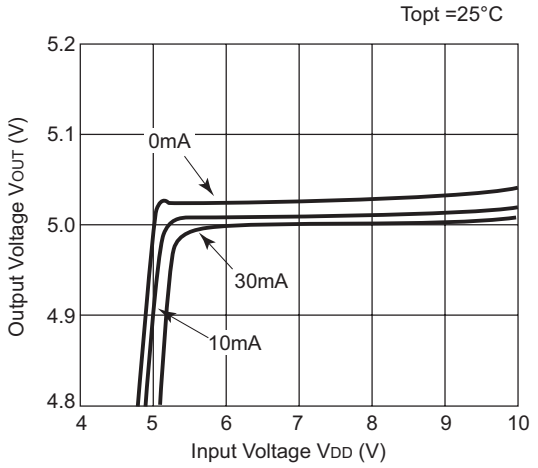


2) Output Voltage vs. Input Voltage

R5101G (VR=3V)

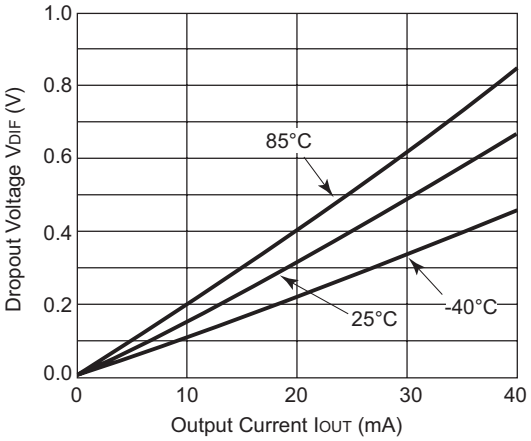


R5101G (VR=5V)

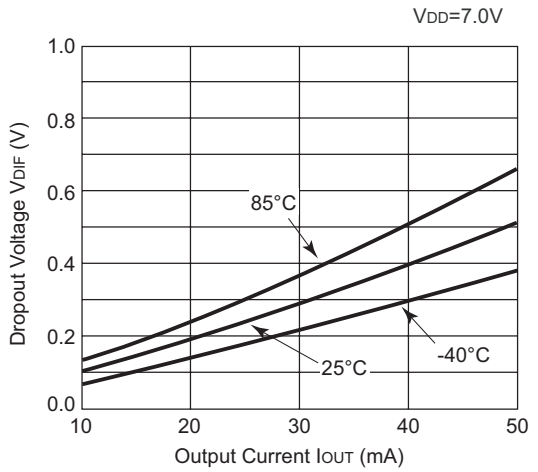


3) Dropout Voltage vs. Output Current

R5101G (VR=3V)

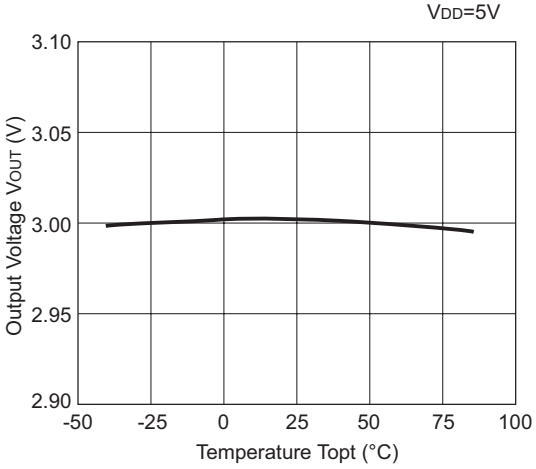


R5101G (VR=5V)

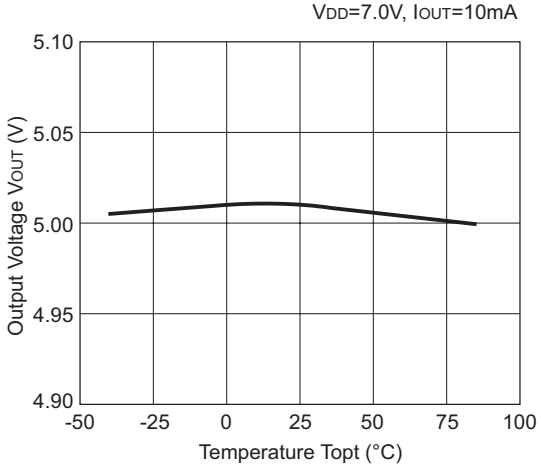


4) Output Voltage vs. Temperature

R5101G (VR=3V)

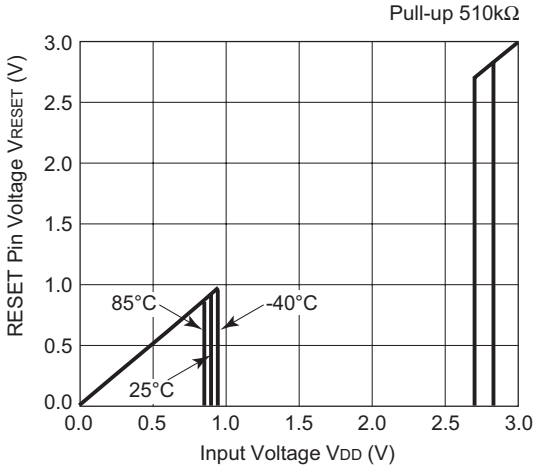


R5101G (VR=5V)



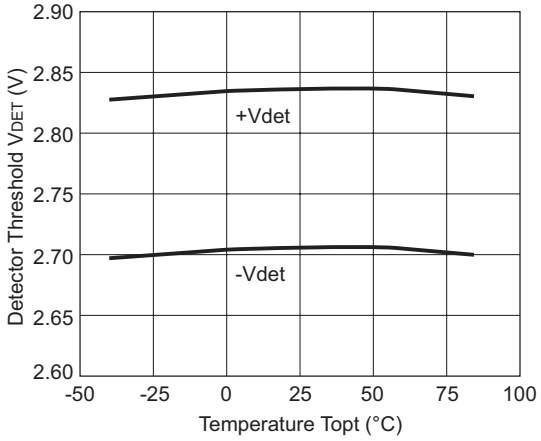
5) RESET Pin Voltage vs. Input Voltage

R5101G (VD=2.7V)



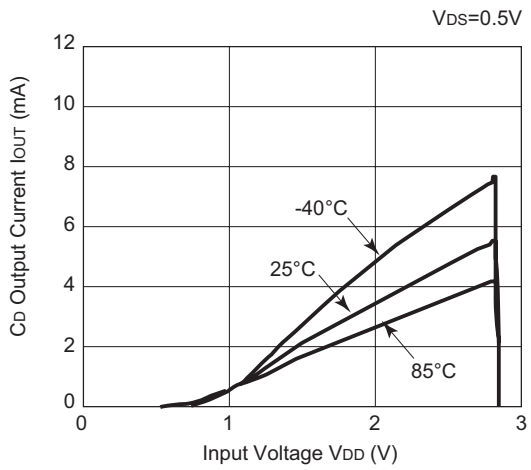
6) Detector Threshold vs. Temperature

R5101G (VD=2.7V)



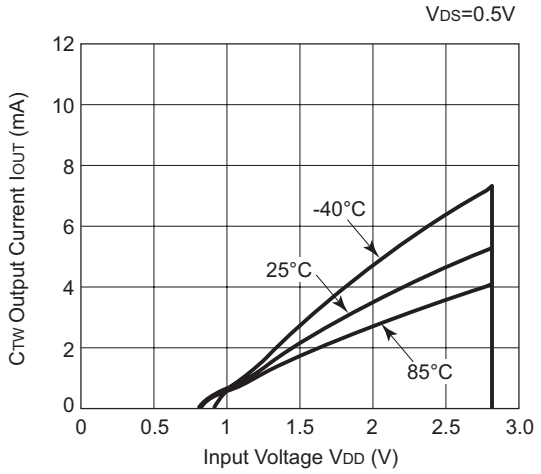
7) C_D Pin Output Current vs. Input Voltage

R5101G (VD=2.7V)

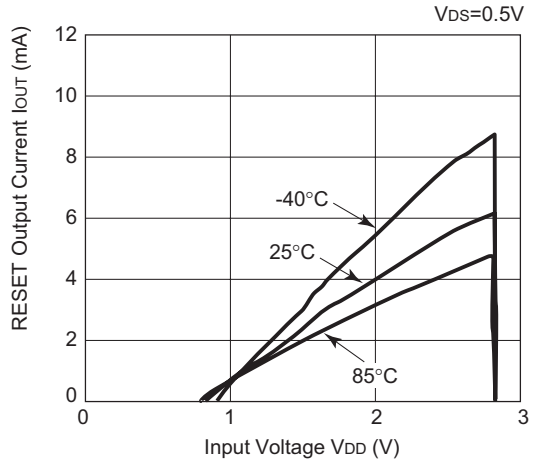


8) C_{TW} Pin Output Current vs. Input Voltage

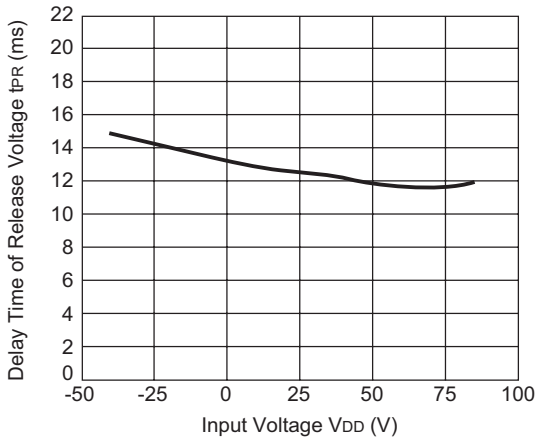
R5101G (VD=2.7V)



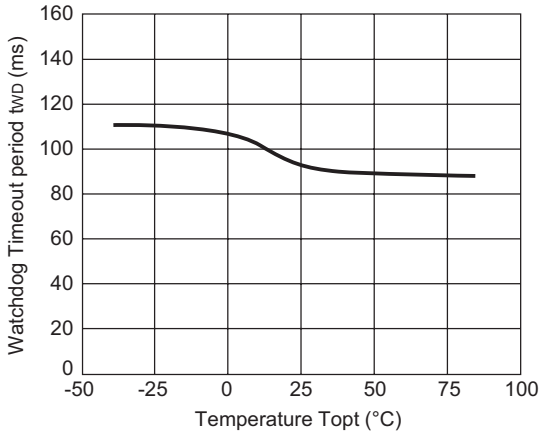
9) RESET Pin Output Current vs. Input Voltage
R5101G (VD=2.7V)



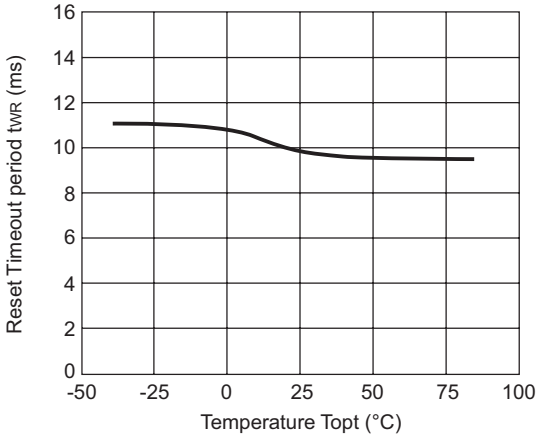
10) Delay Time of Released Voltage vs. Temperature
R5101G



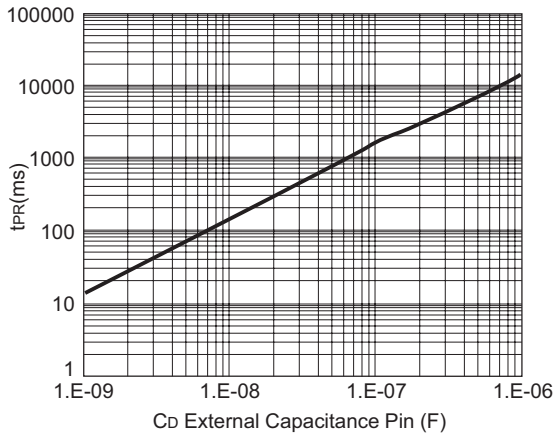
11) Watchdog Timeout period vs. Temperature
R5101G



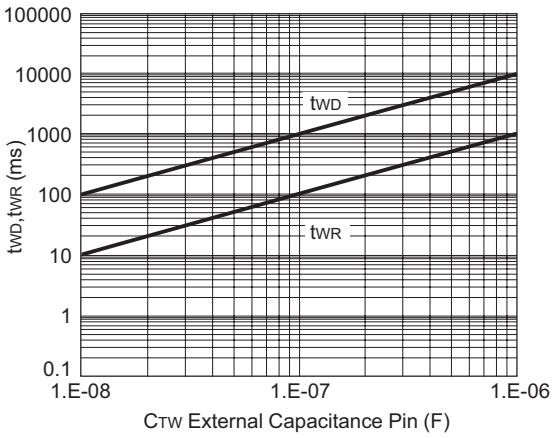
12) Reset Timeout period vs. Temperature
R5101G



13) t_{PR} vs. External Capacitance of C_D Pin

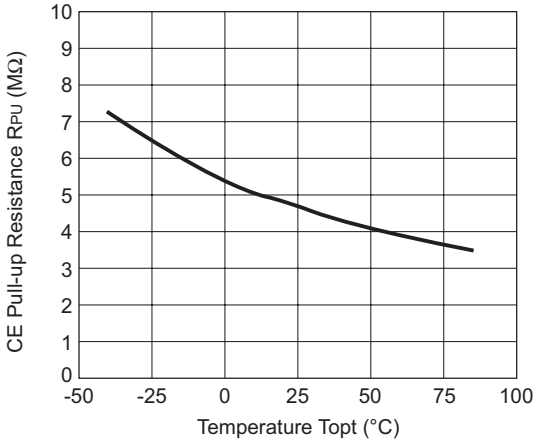


14) t_{WD}, t_{WR} vs. External Capacitance of C_{TW} Pin



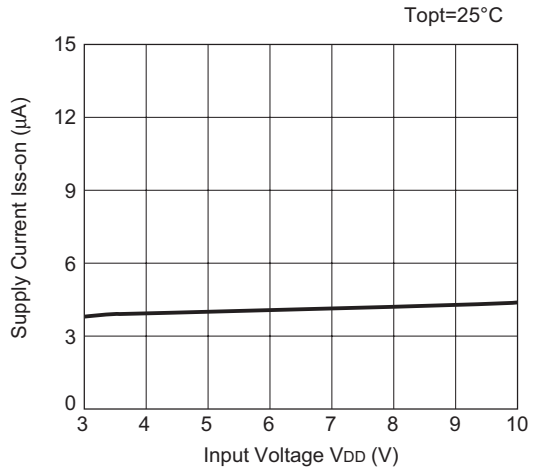
15) CE Pull-up Resistance vs. Temperature

R5101G



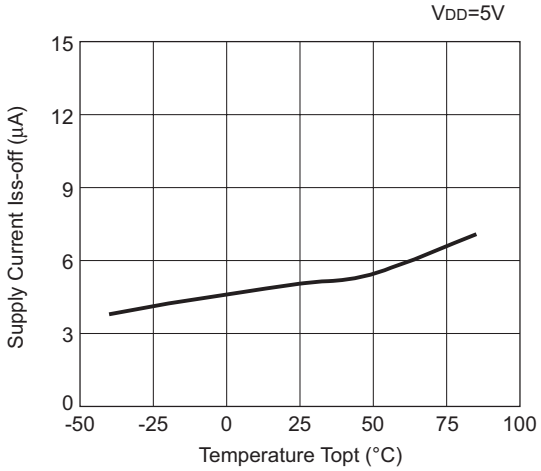
16) Supply Current vs. Input Voltage (WDT ON)

R5101G



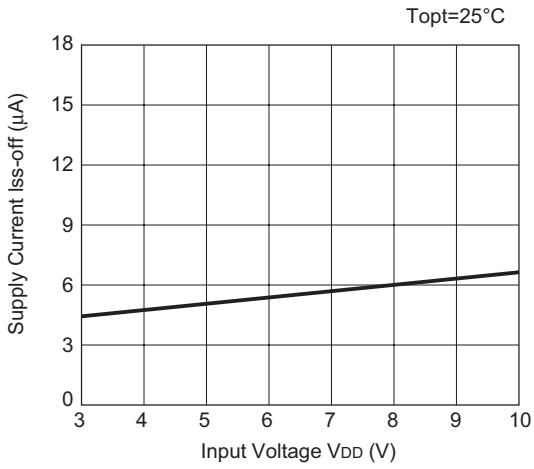
17) Supply Current vs. Temperature (WDT ON)

R5101G



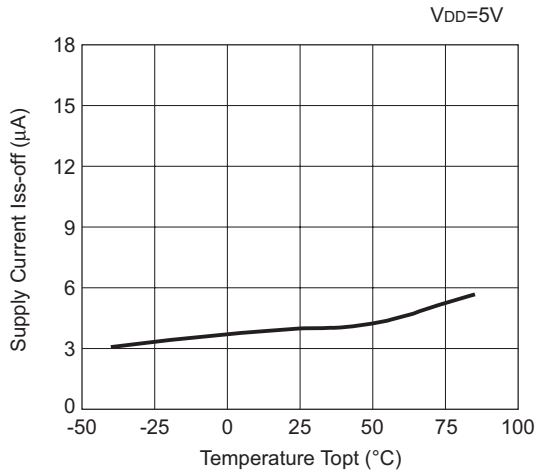
18) Supply Current vs. Input Voltage (WDT OFF)

R5101G



19) Supply Current vs. Temperature (WDT OFF)

R5101G



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RICOH COMPANY, LTD.
Electronic Devices Company
● **Shin-Yokohama office (International Sales)**
3-2-3, Shin-Yokohama, Kohoku-ku, Yokohama City, Kanagawa 222-8530, Japan
Phone: +81-45-477-1697 Fax: +81-45-477-1698

RICOH EUROPE (NETHERLANDS) B.V.
● **Semiconductor Support Centre**
Prof. W.H.Keesomlaan 1, 1183 DL Amstelveen, The Netherlands
P.O.Box 114, 1180 AC Amstelveen
Phone: +31-20-5474-309 Fax: +31-20-5474-791

RICOH ELECTRONIC DEVICES KOREA Co., Ltd.
11 floor, Haesung 1 building, 942, Daechidong, Gangnamgu, Seoul, Korea
Phone: +82-2-2135-5700 Fax: +82-2-2135-5705

RICOH ELECTRONIC DEVICES SHANGHAI Co., Ltd.
Room403, No.2 Building, 690#Bi Bo Road, Pu Dong New district, Shanghai 201203, People's Republic of China
Phone: +86-21-5027-3200 Fax: +86-21-5027-3299

RICOH COMPANY, LTD.
Electronic Devices Company
● **Taipei office**
Room109, 10F-1, No.51, Hengyang Rd., Taipei City, Taiwan (R.O.C.)
Phone: +886-2-2313-1621/1622 Fax: +886-2-2313-1623