1.1 Scope.

This specification covers the detail requirement for a 16-bit ADC which uses a sigma-delta conversion technique. No missing codes ensures true, usable, 16-bit dynamic range, removing the need for programmable gain and level-setting circuitry.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows.

Device	Part Number
−1	AD7701TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package	Description
Q-20	20-Pin Cerdip

1.3 Absolute Maximum Ratings.

DV_{DD} to AGND ..... −0.3 V dc to +6.0 V dc
DV_{DD} to AV_{DD} ..... −0.3 V dc to +0.3 V dc
DV_{SS} to AGND ..... +0.3 V dc to −6.0 V dc
AV_{DD} to AGND ..... −0.3 V dc to +6.0 V dc
AV_{SS} to AGND ..... +0.3 V dc to −6.0 V dc
AGND to DGND ..... −0.3 V dc to +0.3 V dc
Digital Input Voltage to DGND ..... −0.3 V dc to DV_{DD} + 0.3 V dc
Analog Input Voltage to AGND ..... AV_{SS} − 0.3 V dc to AV_{DD} + 0.3 V dc
Input Current to Any Pin Except Supplies ..... ±10 mA
Power Dissipation, P_D ..... 450 mW
Thermal Resistance, Junction-to-Case ..... See MIL-M-38510, Appendix C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

1.4 Recommended Operating Conditions.

Positive Supply Voltage Range
  AV_{DD} ..... +4.5 V dc to +5.5 V dc
  DV_{DD} ..... +4.5 V dc to AV_{DD}
Negative Supply Voltage Range (AV_{SS}, DV_{SS}) ..... −4.5 V dc to −5.5 V dc
Calibration Memory Retention Supply Voltage ..... +2.0 V dc minimum
Operating Temperature Range, T_A ..... −55°C to +125°C

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Table 1.

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups A	Conditions[1] ($-55°C \le T_A \le +125°C$ unless otherwise noted)	Unit
Resolution	RES	All	16		1, 2, 3	Guaranteed Minimum Resolution	Bits
Integral Nonlinearity	INL	All		±0.0015	1, 2, 3		%FSR
Differential Nonlinearity	DNL	All		±0.5	1, 2, 3	Guaranteed No Missing Codes	LSB
Positive Full-Scale Error[2]	PFSE	All		±0.5	1		LSB
Unipolar Offset Error[2]	UOE	Al		±1.0	1		LSB
Bipolar Zero Error[2]	BZE	All		±1.0	1		LSB
Bipolar Negative Full-Scale Error[2]	BNFSE	All		±2.0	1		LSB
Positive Full-Scale Overrange[3]	$+V_{FSO}$	All		$V_{REF} + 0.1$	1		V
Negative Full-Scale Overrange[3]	$-V_{FSO}$	All		$-(V_{REF} + 0.1)$	1		V
Unipolar Input Offset Calibration Range[4, 5]	V_{UCAL}	All		$-(V_{REF} + 0.1)$	1		V
Bipolar Input Offset Calibration Range[4, 5]	V_{BCAL}	All	$-0.4\ V_{REF}$	$+0.4\ V_{REF}$	1		V
Calibration Input Span[6]	V_{CIS}	All	$0.8\ V_{REF}$	$2\ V_{REF} + 0.2$	1		V
Analog Input Voltage Range, Unipolar	$V_{AIN(U)}$	All	0	2.5	1, 2, 3		V
Bipolar	$V_{AIN(B)}$	All	−2.5	+2.5	1, 2, 3		V
Logic Input Low Voltage	V_{IL}	All		0.8	1, 2, 3		V
Logic Input High Voltage	V_{IH}	All	2.0		1, 2, 3	All Input Except CLKIN	V
			3.5			CLKIN	
Logic Input Current	I_{IN}	All		10	1, 2, 3		μA
Output Logic Low Voltage	V_{OL}	All		0.4	1, 2, 3	I_{SINK} = 1.6 mA	V
Output Logic High Voltage	V_{OH}	All	$DV_{DD} - 1.0$		1, 2, 3	I_{SOURCE} = 100 μA	V
Floating State Leakage Current		All		±10	1, 2, 3		μA
Analog Positive Supply Current	AI_{DD}	All		3.2	1, 2, 3	Note 7	mA
Digital Positive Supply Current	DI_{DD}	All		1.5	1, 2, 3	Note 7	mA
Analog Negative Supply Current	AI_{SS}	All		3.2	1, 2, 3	Note 7	mA
Digital Negative Supply Current	DI_{SS}	All		0.1	1, 2, 3	Note 7	mA
Master Clock Frequency[8, 9]	f_{CLKIN}	All	40		9, 10, 11	Internal Gate Oscillator	kHz
				5000		Externally Supplied	
Digital Output Rise Time[8, 10]	t_r	All		50	9, 10, 11		ns
Digital Output Fall Time[8, 10]	t_f	All		50	9, 10, 11		ns
Setup Time, SC1, SC2 to CAL High	t_1	All	0		9, 10, 11		ns
SC1, SC2 Hold Time After CAL Goes High	t_2	All	50		9, 10, 11		ns
Setup Time, SLEEP High to CLKIN High[8, 11]	t_3	All	1000		9, 10, 11		ns

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups A	Conditions[1] ($-55°C \le T_A \le +125°C$ unless otherwise noted)	Unit
Synchronous Self-Clocking Mode (SSC) Timing Characteristics							
Data Access Time ($\overline{CS}$ Low to Data Valid)[8, 12]	t_4	All	$3/f_{CLKIN}$		9, 10, 11		ns
SCLK Falling Edge to Data Valid Delay[8]	t_5	All		100	9, 10, 11		ns
MSB Data Setup Time[8]	t_6	All	250		9, 10, 11		ns
SCLK High Pulse Width[8]	t_7	All		300	9, 10, 11		ns
SCLK Low Pulse Width[8]	t_8	All		790	9, 10, 11		ns
SCLK Rising Edge to High Impedance Delay[8, 13]	t_9	All		$1/f_{CLKIN} + 200$	9, 10, 11		ns
$\overline{CS}$ High to High Impedance Delay[8, 13, 14]	t_{10}	All		$4/f_{CLKIN} + 200$	9, 10, 11		ns
Synchronous External Clock Mode (SEC) Timing Characteristics							
Serial Clock Input Frequency[8]	f_{SCLK}	All		5.0	9, 10, 11		MHz
SCLK Input High Pulse Width[8]	t_{11}	All	50		9, 10, 11		ns
SCLK Low Pulse Width[8]	t_{12}	All	180		9, 10, 11		ns
Data Access Time ($\overline{CS}$ Low to Data Valid)[8, 12, 15]	t_{13}	All		160	9, 10, 11		ns
SCLK Falling Edge to Data Valid Delay[8, 16]	t_{14}	All	150		9, 10, 11		ns
$\overline{CS}$ High to High Impedance Delay[8, 13]	t_{15}	All	250		9, 10, 11		ns
SCLK Falling Edge to High Impedance Delay[8]	t_{16}	All	200		9, 10, 11		ns
Asynchronous Communications Mode (AC) Timing Characteristics							
$\overline{CS}$ Setup Time[8]	t_{17}	All		40	9, 10, 11		ns
Data Delay Time[8]	t_{18}	All		180	9, 10, 11		ns
SCLK Falling Edge to High Impedance Delay[8]	t_{19}	All		200	9, 10, 11		ns

NOTES

[1]AV_{DD} = DV_{DD} = 5.0 V dc; AV_{SS} = DV_{SS} = −5.0 V dc; V_{REF} = +2.5 V dc; f_{CLKIN} = 4.096 MHz; bipolar mode; MODE = 5.0 V dc; A_{IN} source resistance = 1 kΩ with 1.0 nF to AGND at A_{IN}, unless otherwise specified (the A_{IN} pin presents a very high impedance dynamic load which varies with clock frequency.)

[2]Apply after calibration at the temperature of interest. Full-scale error applies for both unipolar and bipolar input ranges.

[3]Applies to unipolar and bipolar ranges. After calibration, if $A_{IN} > V_{REF}$, the device will output all 1s. If $A_{IN} < 0$ (unipolar) or $-V_{REF}$ (bipolar), the device will output all 0s.

[4]In unipolar mode the offset can have a negative value ($-V_{REF}$) such that the unipolar mode can mimic bipolar mode operation.

[5]The specifications for input overrange and for input span apply additional constraints on the offset calibration range.

[6]For unipolar mode, input span is the difference between full-scale and zero scale. For bipolar mode, input span is the difference between positive and negative full-scale points. When using less than the maximum input span, the span range may be place anywhere within the range of $\pm(V_{REF} + 0.1)$.

[7]All digital outputs loaded. All digital inputs at 5.0 V dc CMOS levels.

[8]Sample tested at +25°C to ensure compliance

[9]CLKIN Duty Cycle range is 20% to 80%. CLKIN must be supplied whenever the device is not in SLEEP mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[10]Specified using 10% and 90% points on waveform of interest.

[11]In order to synchronize several devices together using the $\overline{SLEEP}$ pin, this specification must be met.

[11]t_4 and t_{13} are measured with the load circuit of Figure xx and defined as the time required for an output to cross 0.8 V or 2.4 V.

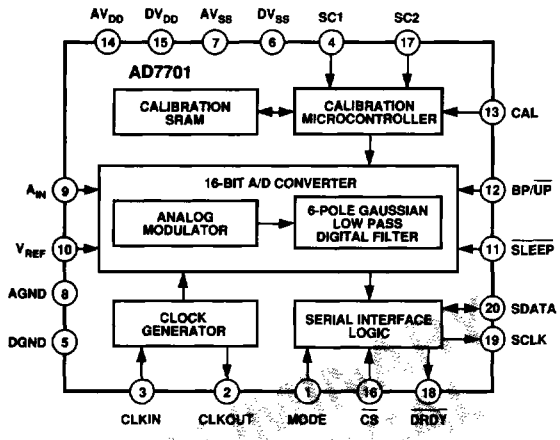
[13]t_8, t_{10}, t_{15} and t_{16} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure xx. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in Table 1 is the true bus relinquish time of the part and as such as independent of external bus loading capacitance.

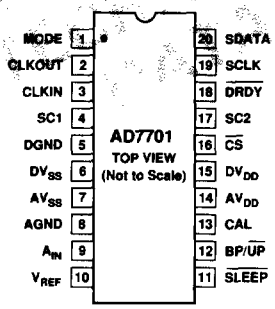
[14]If $\overline{CS}$ is returned high before all 16 bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

[15]If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for four clock cycles. The propagation delay time be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, the SCLK input should not be taken high sooner than 4 CLKIN cycles plus 160 ns after $\overline{CS}$ goes low.

[16]SDATA is clocked out on the falling edge of the SCLK input.

3.2.1 Functional Block Diagram and Terminal Assignments.





3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).