ANALOG DEVICES

Dual Low-Noise Low-Offset Instrumentation Operational Amplifier

OP-227

1.0 SCOPE

This specification covers the detail requirements for a dual low-noise low-offset instrumentation operational amplifier.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

1.2 Part Number. The complete part numbers per Table I of this specification follow:

Device	Part Number	Package
A	OP-227AY/883	Y

1.2.3 Case Outline.

Letter	Case Outline (Lead finish per MIL-M-38510)
Y	14-lead ceramic dual-in-line package (CERDIP)

1.3 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

Supply Voltage ..... ±22V
Internal Power Dissipation 500mW
Input Voltage (Note 1) ..... ±22V
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltages.
2. The OP-227 inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

1.5 Thermal Characteristics:

Thermal Resistance, CERDIP (Y) package:
Junction-to-Case (Θ_{JC}) = 29°C/W MAX
Junction-to-Ambient (Θ_{JA}) = 91°C/W MAX

TABLE 1

V_S = ±15V; R_S = 50Ω; T_A = 25°C unless otherwise specified.

Individual Amplifier Characteristics	Symbol	Special Conditions	OP-227/883 LIMITS A Min	Max	Units
Input Offset Voltage	V_{OS}		–	80	μV
		-55°C ≤ T_A ≤ +125°C	–	180	μV
Input Offset Current	I_{OS}		–	35	nA
		-55°C ≤ T_A ≤ +125°C	–	50	nA
Input Bias Current	I_B		–	±40	nA
		-55°C ≤ T_A ≤ +125°C	–	±60	nA
Input Noise Voltage (Note 1)	e_n	f_O = 1Hz to 100Hz	–	50	nV_{RMS}
Input Noise Current (Note 1)	i_n	f_O = 1Hz to 100Hz	–	40	pA_{RMS}
Input Voltage Range (Note 2)	IVR		±11	–	V
		-55°C ≤ T_A ≤ +125°C	±10	–	V
Common-Mode Rejection	CMR	V_{CM} = IVR = ±11V	114	–	dB
		V_{CM} = IVR = ±10V	108	–	dB
		-55°C ≤ T_A ≤ +125°C			
Power Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	–	10	μV/V
		V_S = ±4.5V to ±18V	–	16	μV/V
		-55°C ≤ T_A ≤ +125°C			
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L ≥ 2kΩ	1000	–	V/mV
		V_O = ±10V, R_L ≥ 600Ω	800	–	V/mV
		V_O = ±10V, R_L ≥ 2kΩ	600	–	V/mV
		-55°C ≤ T_A ≤ +125°C			

TABLE 1 (Continued)

V_S = ±15V; R_S = 50Ω; T_A = 25°C unless otherwise specified.

Individual Amplifier Characteristics	Symbol	Special Conditions	OP-227/883 LIMITS A Min	Max	Units
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	–	V
		$R_L \geq 600\Omega$	±10	–	V
		$R_L \geq 2k\Omega$ $-55°C \leq T_A \leq +125°C$	±11.5	–	V
Power Dissipation (Each Amplifier) (Note 3)	P_d	V_O = 0V	–	140	mW
Power Supply Current (Each Amplifier)	I_{SY}	V_O = 0V	–	4.67	mA
Offset Adjustment Range	$V_{OS}adj$	R_p = 10kΩ	±0.5	–	mV
Output Short-Circuit Current	I_{SC}^+		–	70	mA
	I_{SC}^-		-70	–	mA

NOTES:
1. This test is 100% tested.
2. IVR is defined as the V_{CM} range used for the CMR test.
3. P_d is derived from I_{SY} by the relationship $P_d = V_S * I_{SY}$.

TABLE 1 (Continued)

V_S = ±15V; R_S = 50Ω; T_A = 25°C unless otherwise specified.

Matching Characteristics	Symbol	Special Conditions	OP-227/883 LIMITS A Min	Max	Units
Input Offset Voltage Match	ΔV_{OS}		–	80	μV
		-55°C ≤ T_A ≤ +125°C	–	180	μV
Average Non-Inverting Bias Current	I_{B^+}	$I_{B^+} = \frac{(I_{B^+A}) + (I_{B^+B})}{2}$	–	±40	nA
		$I_{B^+} = \frac{(I_{B^+A}) + (I_{B^+B})}{2}$ -55°C ≤ T_A ≤ +125°C	–	±60	nA
Noninverting Offset Current	I_{OS^+}	$I_{OS^+} = (I_{B^+A}) - (I_{B^+B})$	–	±60	nA
		$I_{OS^+} = (I_{B^+A}) - (I_{B^+B})$ -55°C ≤ T_A ≤ +125°C	–	±90	nA
Inverting Offset Current	I_{OS^-}	$I_{OS^-} = (I_{B^-A}) - (I_{B^-B})$	–	±60	nA
		$I_{OS^-} = (I_{B^-A}) - (I_{B^-B})$ -55°C ≤ T_A ≤ +125°C	–	±90	nA
Common-Mode Rejection Match	ΔCMR	V_{CM} = ±11V	110	–	dB
		V_{CM} = ±10V -55°C ≤ T_A ≤ +125°C	105	–	dB
Power Supply Rejection Ratio Match	ΔPSRR	V_S = ±4V to ±18V	–	10	μV/V
		V_S = ±4.5V to ±18V -55°C ≤ T_A ≤ +125°C	–	16	μV/V

TABLE 2

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Electrical Test Requirements
For Class B Devices

MIL-STD-883 Test Requirements	Subgroups (see Table 3)
Interim Electrical Parameters (pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6

* PDA applies to Subgroup 1 only.
V_{OS} is excluded from PDA calculation.
No other Subgroups are included in PDA.

TABLE 3

Group A Inspection

V_S = ±15V; R_S = 50Ω; T_A = T_J unless otherwise specified.

Subgroup	Symbol	Special Conditions	OP-227/883 LIMITS A Min	Max	Units
Subgroup 1	V_{OS}		–	80	μV
T_A = +25°C	I_{OS}		–	35	nA
	I_B		–	±40	nA
	I_{SY}	V_O = 0V	–	4.67	mA
	CMR	V_{CM} = +11V	114	–	dB
	PSRR	V_S = ±4V, ±18V	–	10	μV/V
	V_{OS}adj		±0.5	–	mV
	I_{SC}^+		–	70	mA
	I_{SC}^-		-70	–	mA
	ΔV_{OS}		–	80	μV
	I_B^+	$I_B^+ = \frac{(I_B^+A) + (I_B^+B)}{2}$	–	±40	nA
	I_{OS}^+	$I_{OS}^+ = (I_B^+A) - (I_B^+B)$	–	±60	nA
	I_{OS}^-	$I_{OS}^- = (I_B^-A) - (I_B^-B)$	–	±60	nA
	ΔCMR	V_{CM} = ±11V	110	–	dB
	ΔPSRR	V_S = ±4V, ±18V	–	10	μV/V
Subgroup 2	V_{OS}		–	180	μV
T_A = +125°C	I_{OS}		–	50	nA
	I_B		–	±60	nA

TABLE 3

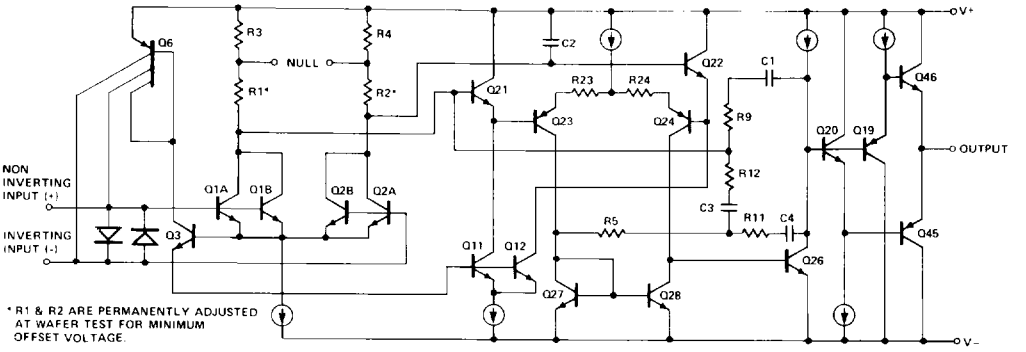
Group A Inspection

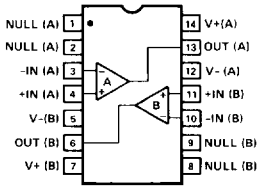
V_S = ±15V; R_S = 50Ω; T_A = T_J unless otherwise specified.

Subgroup	Symbol	Special Conditions	OP-227/883 LIMITS A Min	Max	Units
Subgroup 2	CMR	V_{CM} = ±10V	108	–	dB
T_A = +125°C	PSRR	V_S = ±4.5V, ±18V	–	16	µV/V
(Continued)	ΔV_{OS}		–	180	µV
	I_{B^+}	$I_{B^+} = \frac{(I_{B^+A}) + (I_{B^+B})}{2}$	–	±60	nA
	I_{OS^+}	$I_{OS^+} = (I_{B^+A}) - (I_{B^+B})$	–	±90	nA
	I_{OS^-}	$I_{OS^-} = (I_{B^-A}) - (I_{B^-B})$	–	±90	nA
	ΔCMR	V_{CM} = ±10V	105	–	dB
	ΔPSRR	V_S = ±4.5V, ±18V	–	16	µV/V
Subgroup 3 T_A = -55°C		All Tests, Limits and Conditions are the same as for Subgroup 2.			
Subgroup 4	V_O	R_L = 2kΩ	±12	–	V
		R_L = 600Ω	±10	–	V
T_A = +25°C	A_{VO}	V_O = ±10V, R_L = 2kΩ	1000	–	V/mV
		V_O = ±10V, R_L = 600Ω	800	–	V/mV
Subgroup 5	V_O	R_L = 2kΩ	±11.5	–	V
T_A = +125°C	A_{VO}	V_O = ±10V, R_L = 2kΩ	600	–	V/mV
Subgroup 6 T_A = -55°C		All Tests, Limits and Conditions are the same as for Subgroup 5.			

3.2.1 Simplified Schematic and Pin Connections.

(1/2 OP-227)





14-PIN CERAMIC DIP
(Y-Suffix)

NOTES:
1. **Device may be operated even if insertion is reversed: this is due to inherent symmetry of pin locations of amplifiers A and B.**
2. **V- (A) and V- (B) are internally connected via substrate resistance.**

3.2.4 Microcircuit Group Assignment.

This microcircuit is covered by microcircuit group 49.

4.2 Life Test/Burn-In Circuit.