Panasonic

The most suitable for multimedia applications

32-bit Microprocessor MN103E010H

■ Overview

MN103E010H is a high performance general-purpose 32-bit microprocessor, which integrates Matsushita-original architecture AM33 CPU core.
It is suitable for various multimedia applications with its OS support mechanism such as privilege level support and MMU.

■ Feature

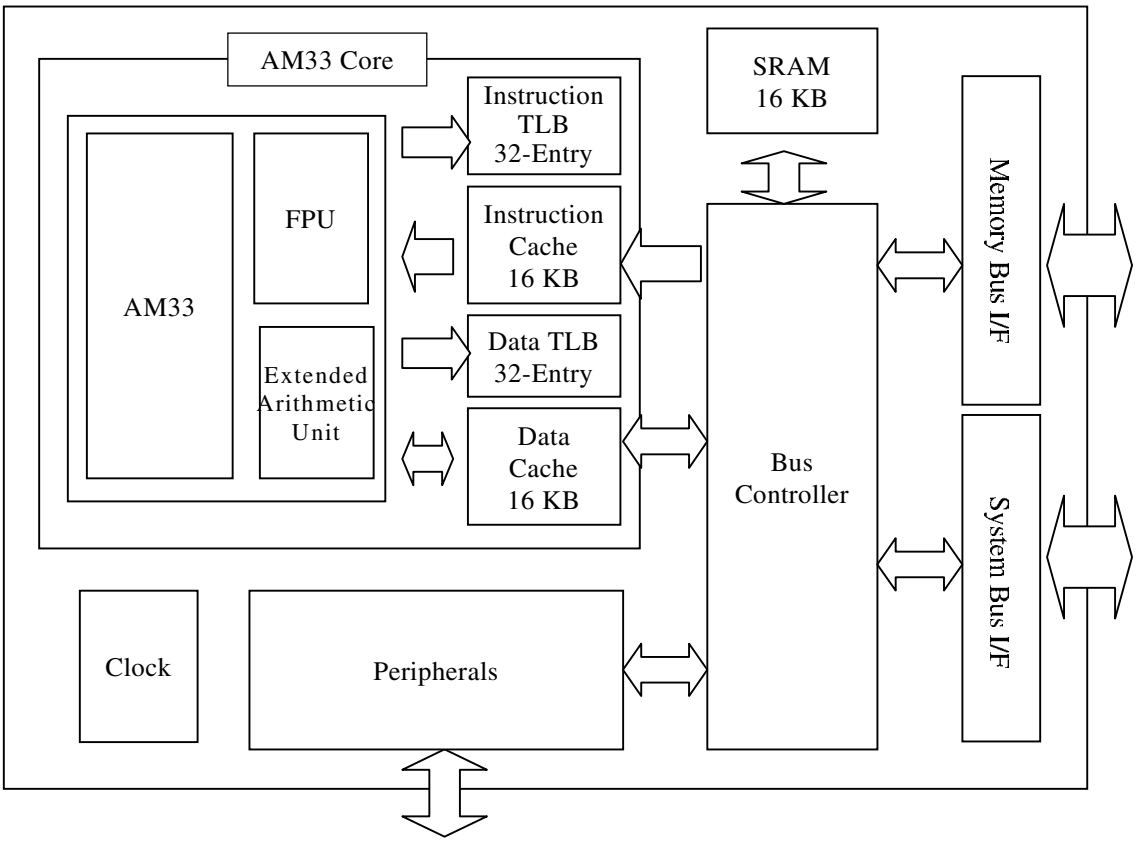
- On-chip Cache Memory
- MMU (Memory Management Unit)
- Single precision Floating Point Unit
- Parallel processing instructions (SIMD-type instructions, LIW-type instructions)
- Cross-bar switch for reducing bus bottleneck
- C language oriented CPU architecture with minimum code size
- Microsoft® Windows® CE supported

※ Microsoft and Windows are either registered trademarks or trademarks of Microsoft Corp. in the United States and/or other countries.

■ Applications

Digital TV, Set-Top-Box, ITS, PDA, Internet Devices

■ System block diagram



Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

1 Kotari-yakemachi, Nagaokakyo, Kyoto 617-8520, Japan Tel. +81-75-951-8151 http://www.panasonic.co.jp/semicon/

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■ Development environment

- Compiler
  - ·Matsushita C compiler/assembler/linker
  - ·CYGNUS GNU C/C++ compiler/assembler/linker
- On-board debug
  - · Source code debugger
  - ·Rich debug functions
    - Cache access monitor, Real-time memory watch
    - Instruction/Operand Break, Code back-trace
- Evaluation board
- Middleware

■ Specification Overview

CP U	133 MIPS (133 MHz)
General purpose register	General purpose register : 16 Floating point register : 32
Cache memory	Instruction cache: 16 KB (4-way set associative) Data cache : 16 KB (4-way set-associative)
MMU	Full associative TLB Instruction TLB, Data tlb:32-entry each Software table walk
On-chip RAM	16 KB (Instruction / Data, cacheable)
FPU	Single precision floating point (IEE754 compliant)
Timer/counter	8-bit x 4,16=bit x 8,WDT x 1
Serial Interface	UART x 3
Interrupt source	Internal source : 32, External source:9(including NMI)
A/D converter	10-bit (8 channels)
DMA controller	4 channels
System bus I/F	16 / 32- bit width selectable SRAM / ROM / BurstROM interface
Memory bus I/F	16-bit, glue-less SDRAM interface
I/O port	34 (selectable)
Operating Voltage	Core 1.8 ±5% , IO 3.3 V ±5%
Package	PBGA 292 pins / C-CSP 424 pins