XC95432 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 432 macrocells with 9,600 usable gates
- Up to 232 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in a 304-pin HQFP package

Description

The XC95432 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of twenty-four 36V18 Function Blocks, providing 9,600 usable gates with propagation delays of 10 ns.