HARRIS SEMICONDUCTOR

RFG40N10LE, RFP40N10LE, RF1S40N10LE, RF1S40N10LESM

40A, 100V, ESD Rated, Avalanche Rated, Logic Level N-Channel, Enhancement-Mode Power MOSFETs

December 1995

Features

- 40A, 100V
- $r_{DS(ON)} = 0.040\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG40N10LE, RFP40N10LE, RF1S40N10LE, and RF1S40N10LESM are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

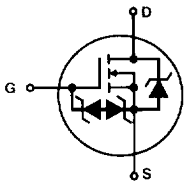
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG40N10LE	TO-247	FG40N10L
RFP40N10LE	TO-220AB	FP40N10L
RF1S40N10LE	TO-262AA	F40N10LE
RF1S40N10LESM	TO-263AB	F40N10LE

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S40N10LESM9A.

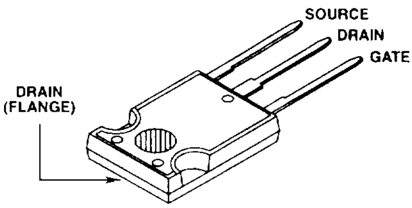
Formerly developmental type TA49163.

Symbol

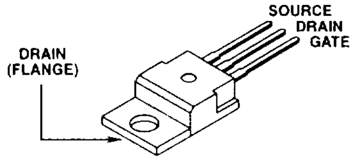


Packages

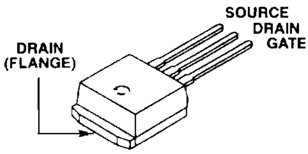
JEDEC STYLE TO-247



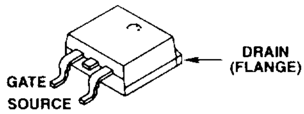
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25°C$

		RFG40N10LE, RFP40N10LE, RF1S40N10LE, RF1S40N10LESM	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	100	V
Gate-Source Voltage (Note)	V_{GS}	±10	V
Continuous Drain Current	I_D	40	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	150	W
Derate above +25°C		1.00	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	kV

NOTE: May be exceeded if gate current is limited to 1mA.

File Number **4061.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =100V, V_{GS} = 0V	T_C = +25°C	-	-	1	μA
			T_C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	10	μA
On Resistance	$r_{DS(ON)}$	I_D = 40A, V_{GS} = 5V		-	-	0.040	Ω
Turn-On Time	t_{ON}	V_{DD} = 50V, I_D = 40A, R_L = 1.25Ω, V_{GS} = 5V, R_{GS} = 2.5Ω		-	-	200	ns
Turn-On Delay Time	$t_{D(ON)}$			-	22	-	ns
Rise Time	t_R			-	140	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	70	-	ns
Fall Time	t_F			-	65	-	ns
Turn-Off Time	t_{OFF}			-	-	165	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 80V, I_D = 40A, R_L = 2.0Ω	-	145	180	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	85	105	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	3	4	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3000	-	pF
Output Capacitance	C_{OSS}			-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-247		-	-	30	°C/W
		TO-220, TO-262, and TO-263		-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 40A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 40A, dI_{SD}/dt = 100A/μs	-	-	205	ns

Typical Performance Curves

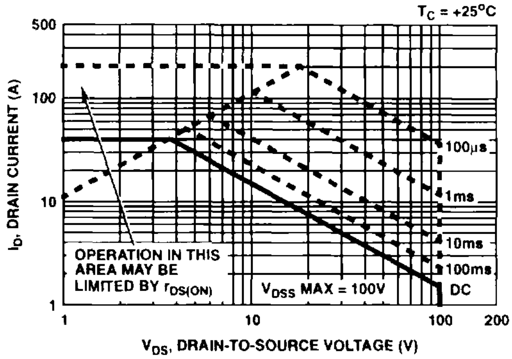


FIGURE 1. SAFE OPERATING AREA CURVE

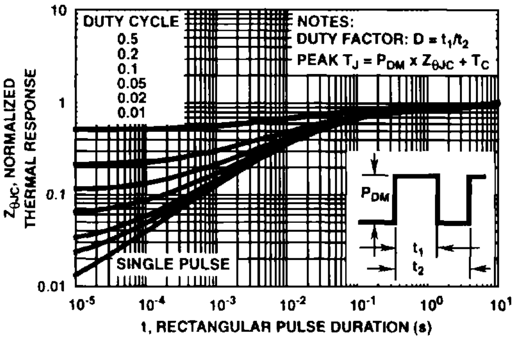


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

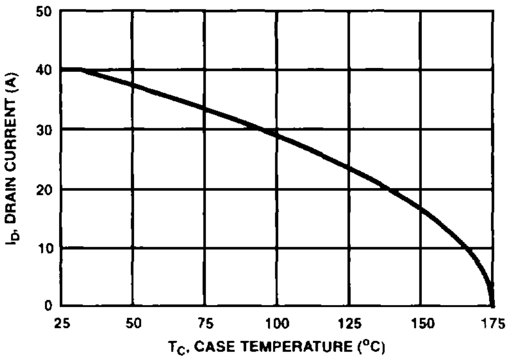


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

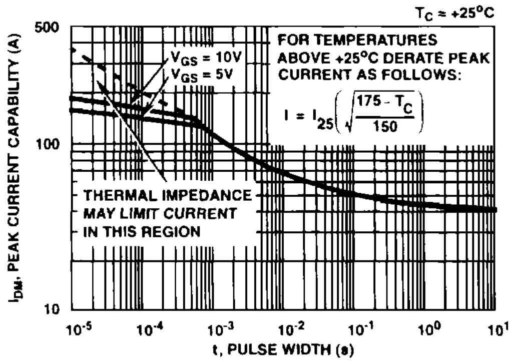


FIGURE 4. PEAK CURRENT CAPABILITY

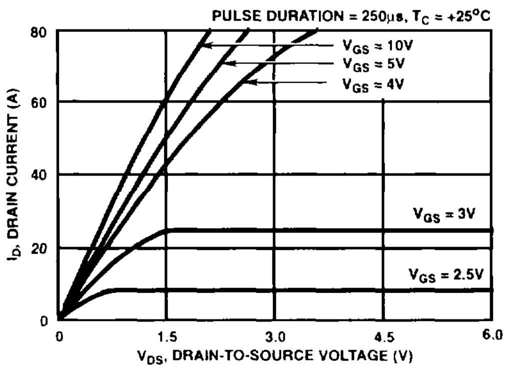


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

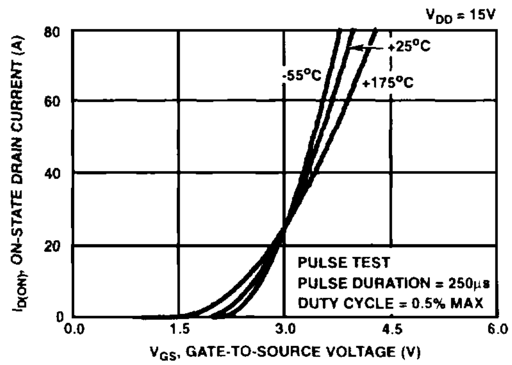


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

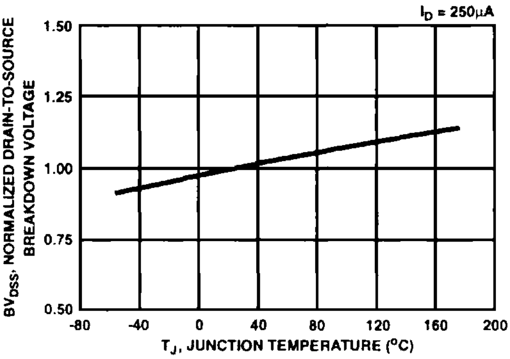


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

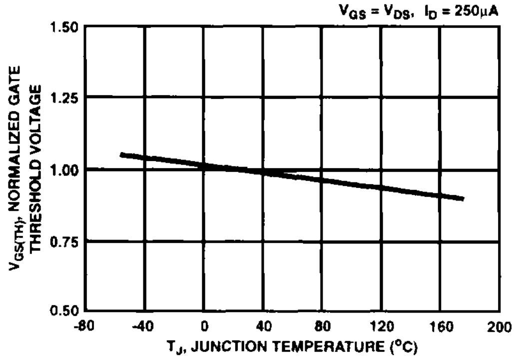


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

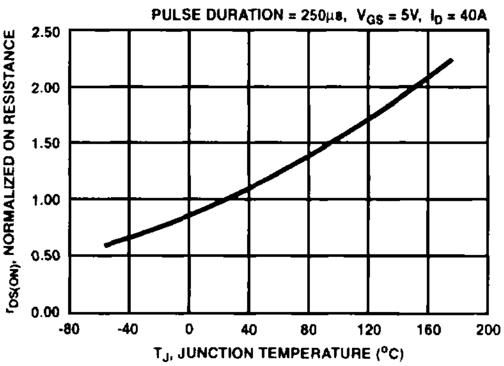


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

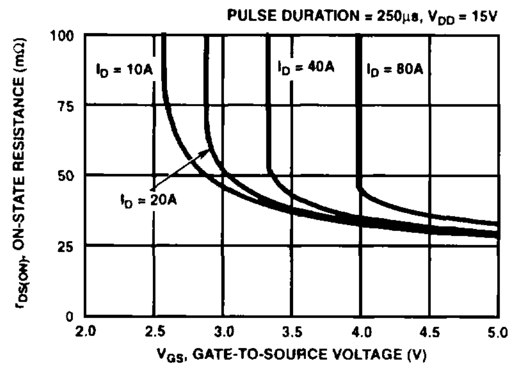


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

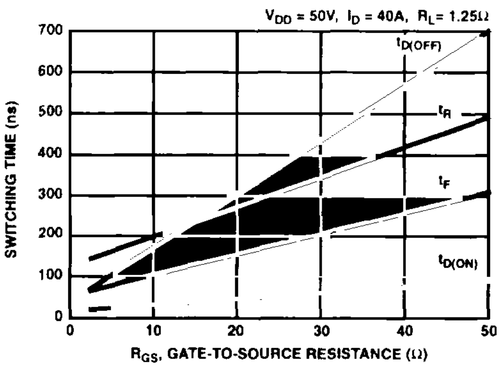


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

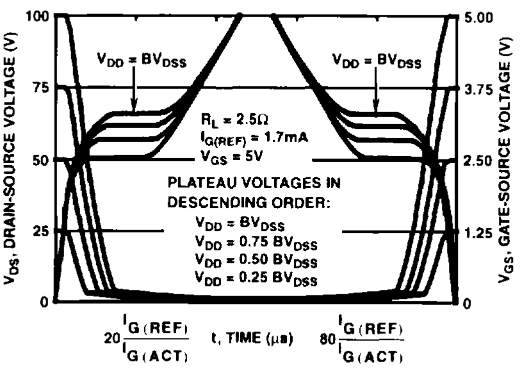


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

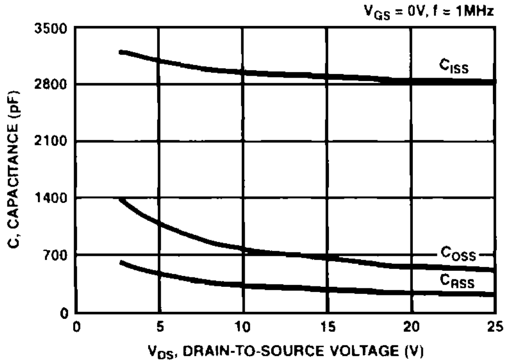


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

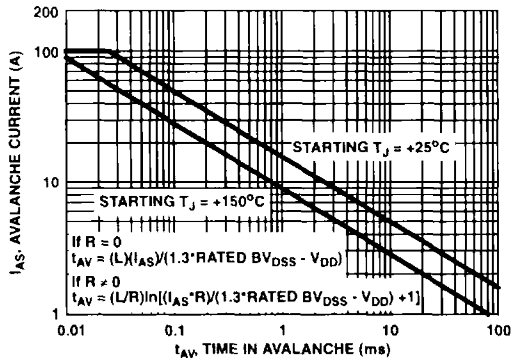


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

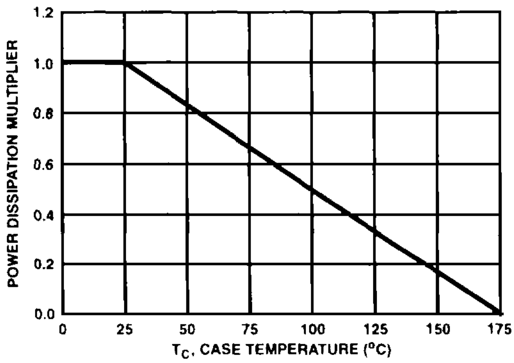


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

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LOGIC LEVEL POWER MOSFETs

Test Circuits and Waveforms

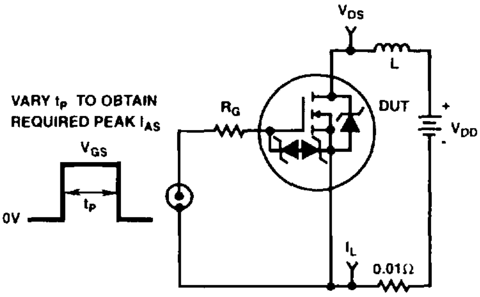


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

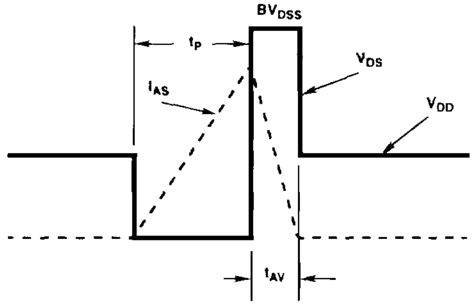


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

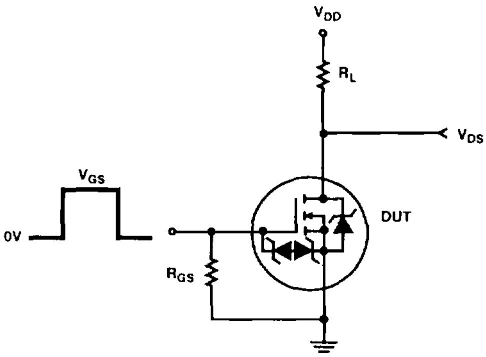


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

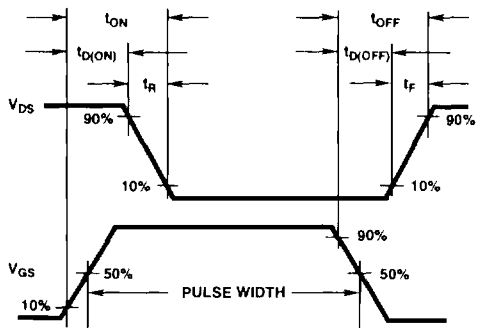
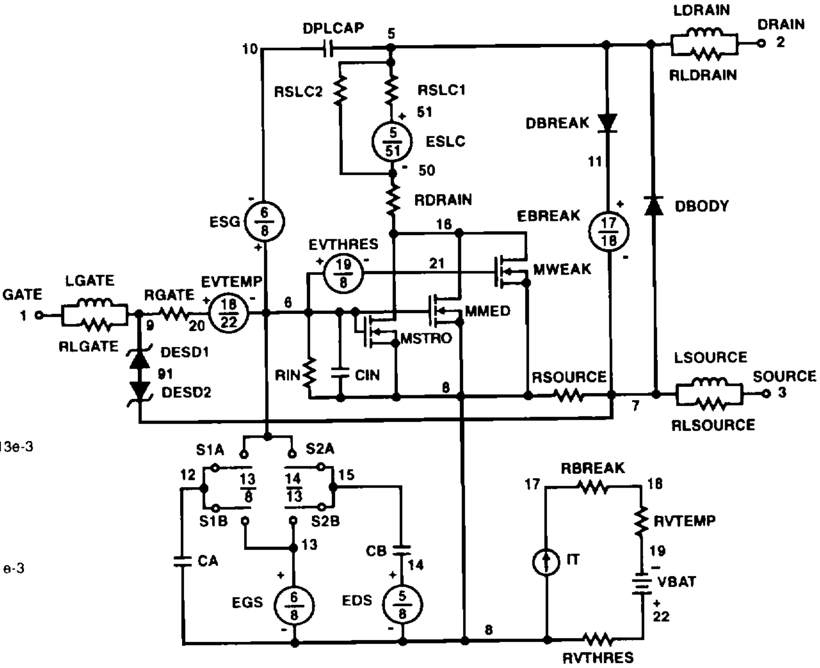


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG40N10LE, RFP40N10LE, RF1S40N10LE, RF1S40N10LESM

SUBCKT 40N10LE 2 1 3 ;   rev 8/15/95

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CA 12 8 11.0e-9
CB 15 14 10.4e-9
CIN 6 8 2.62e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 114.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 7.05e-9
LSOURCE 3 7 3.79e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 19.13e-3
RGATE 9 20 1.19
RLDRAIN 2 5 10
RLGATE 1 9 70.5
RLSOURCE 3 7 37.9
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 1e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*115),4))}

.MODEL DBODYMOD D (IS = 2.0e-12 RS = 9.60e-3 TRS1 = 1.3e-3 TRS2 = -1.16e-7 CJO = 1.50e-9 TT = 1.05e-7 M = 0.5)
.MODEL DBREAKMOD D (RS = 1.92e-1 TRS1 = 1.60e-3 TRS2 = 3.47e-6)
.MODEL DESD1MOD D (BV = 12.43 TBV1 = 0 TBV2 = 0 RS = 57 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 12.45 TBV1= -1.5e-5 TBV2 = 1e-7 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 1.25e-9 IS = 1e-30 N = 10 M = 0.55)
.MODEL MMEDMOD NMOS (VTO = 1.50 KP = 0.40 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.19)
.MODEL MSTROMOD NMOS (VTO = 1.83 KP = 37.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.335 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 11.9 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.04e-3 TC2 = -6.00e-7)
.MODEL RDRAINMOD RES (TC1 = 7.33e-3 TC2 = 2.00e-5)
.MODEL RSLCMOD RES (TC1 = 2.25-3 TC2 = 0)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -0.8e-3 TC2 = -2.5e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.98e-3 TC2 = 1.38e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.25 VOFF = -1.25)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.25 VOFF = -4.25)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.35 VOFF = 1.65)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.65 VOFF = -0.35)

.ENDS
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NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.