



## Dual N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
20	0.225 at V <sub>GS</sub> = 4.5 V	1.5	1.1 nC
	0.270 at V <sub>GS</sub> = 2.5 V	1.5	
	0.345 at V <sub>GS</sub> = 1.8 V	1.5	
	0.960 at V <sub>GS</sub> = 1.5 V	0.5	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- New Thermally Enhanced PowerPAK<sup>®</sup> SC-75 Package
  - Small Footprint Area
  - Low On-Resistance
  - Thin 0.75 mm Profile
- Typical ESD Protection 2800 V
- Rated ESD Protection 1400 V
- Compliant to RoHS Directive 2002/95/EC

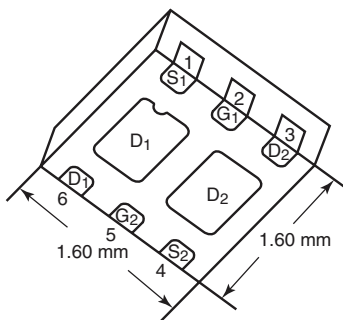


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

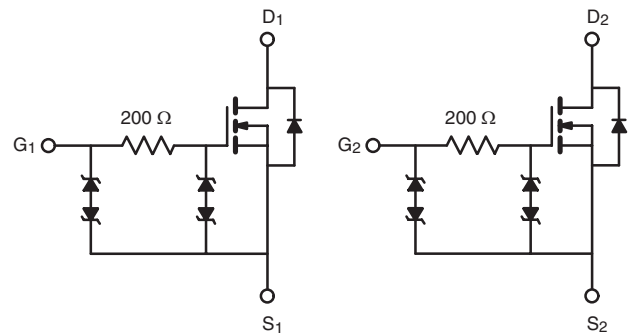
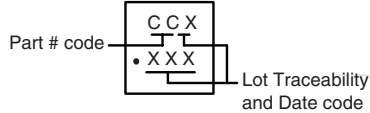
### APPLICATIONS

- Load Switch for Portable Devices
- Low Voltage Load Switch

PowerPAK SC75-6L-Dual



Marking Code



Ordering Information: SiB900EDK-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	± 6	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	1.5 <sup>a</sup>
		T <sub>C</sub> = 70 °C	1.5 <sup>a</sup>
		T <sub>A</sub> = 25 °C	1.5 <sup>a, b, c</sup>
		T <sub>A</sub> = 70 °C	1.3 <sup>b, c</sup>
Pulsed Drain Current	I <sub>DM</sub>	4	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	0.9 <sup>b, c</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	3.1
		T <sub>C</sub> = 70 °C	2
		T <sub>A</sub> = 25 °C	1.1 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	0.7 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	



### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$t \leq 5$ s	$R_{thJA}$	90	115	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	32	40	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 125 °C/W.

### SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ $\mu$ A		21		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-2.3			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	0.4		1.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 3$ V			$\pm 1$	$\mu$ A
		$V_{DS} = 0$ V, $V_{GS} = \pm 6$ V			$\pm 1$	mA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	$\mu$ A
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 4.5$ V	4			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 1.6$ A		0.183	0.225	$\Omega$
		$V_{GS} = 2.5$ V, $I_D = 1.5$ A		0.220	0.270	
		$V_{GS} = 1.8$ V, $I_D = 1.3$ A		0.275	0.345	
		$V_{GS} = 1.5$ V, $I_D = 0.3$ A		0.320	0.960	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10$ V, $I_D = 1.6$ A		3.5		S
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 1.7$ A		1.1	1.7	nC
Gate-Source Charge	$Q_{gs}$		0.2			
Gate-Drain Charge	$Q_{gd}$		0.1			
Gate Resistance	$R_g$	$f = 1$ MHz		200		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 7.7$ $\Omega$ $I_D \cong 1.3$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ $\Omega$		20	30	ns
Rise Time	$t_r$		12	20		
Turn-Off Delay Time	$t_{d(off)}$		70	105		
Fall Time	$t_f$		20	30		
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C			1.5	A
Pulse Diode Forward Current	$I_{SM}$				4	
Body Diode Voltage	$V_{SD}$	$I_S = 1.3$ A, $V_{GS} = 0$ V		0.9	1.2	V

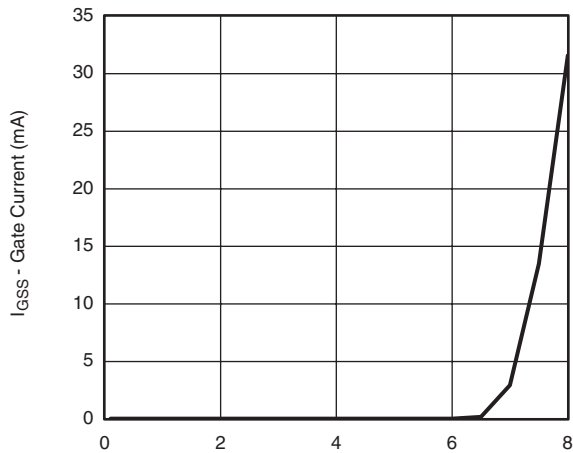
Notes:

- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- Guaranteed by design, not subject to production testing.

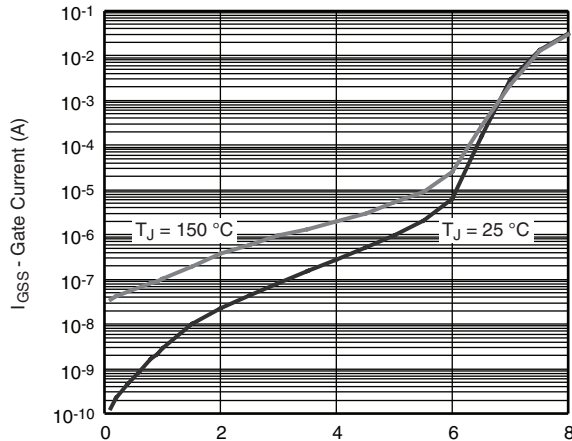
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



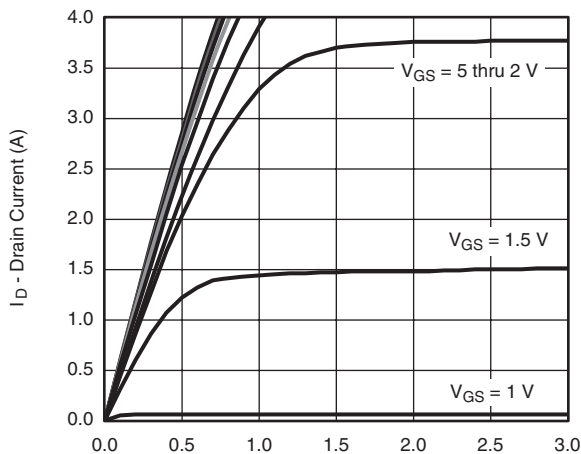
**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



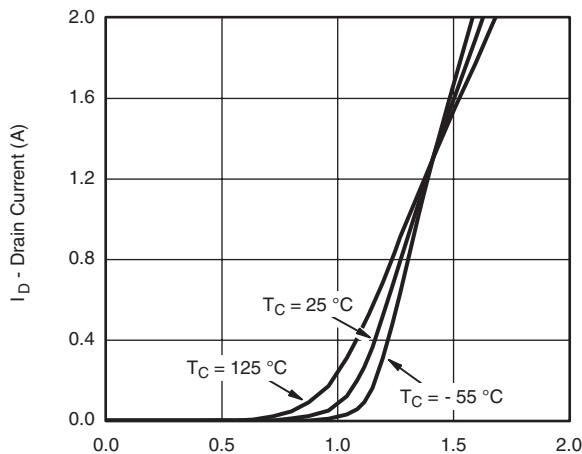
$V_{GS}$  - Gate-to-Source Voltage (V)  
**Gate Current vs. Gate-to-Source Voltage**



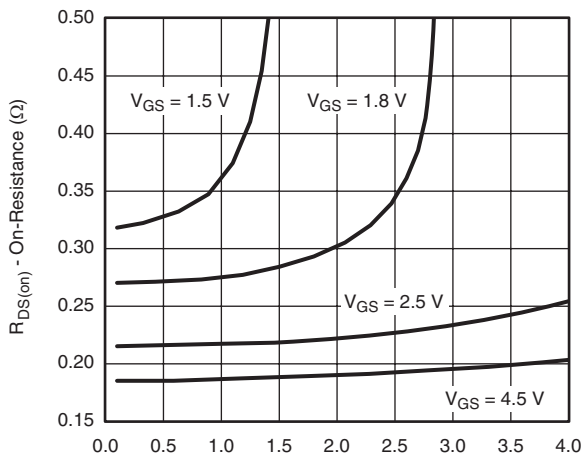
$V_{GS}$  - Gate-to-Source Voltage (V)  
**Gate Current vs. Gate-to-Source Voltage**



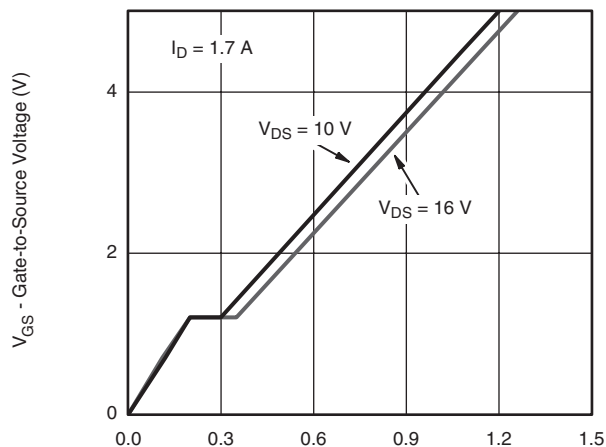
$V_{DS}$  - Drain-to-Source Voltage (V)  
**Output Characteristics**



$V_{GS}$  - Gate-to-Source Voltage (V)  
**Transfer Characteristics**



$I_D$  - Drain Current (A)  
**On-Resistance vs. Drain Current**



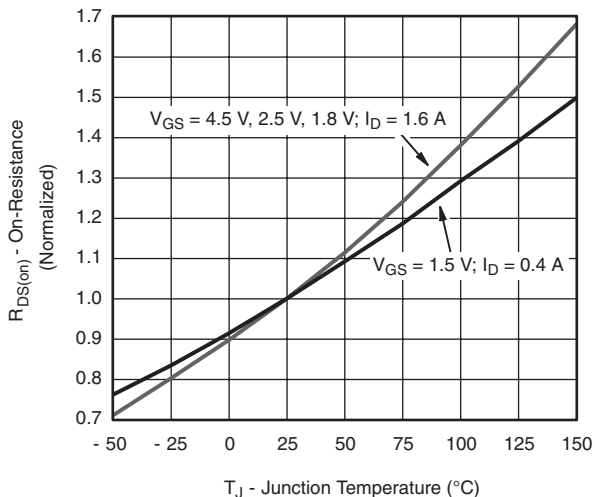
$Q_g$  - Total Gate Charge (nC)  
**Gate Charge**

# SiB900EDK

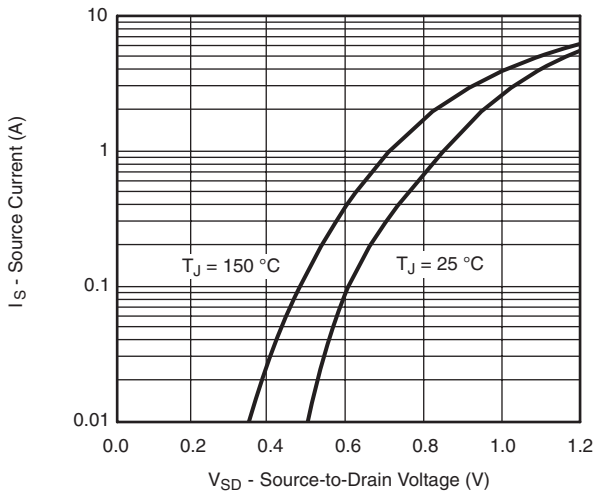
Vishay Siliconix



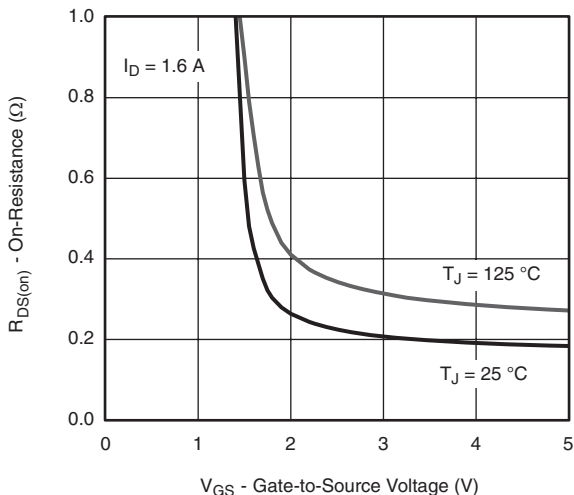
## TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



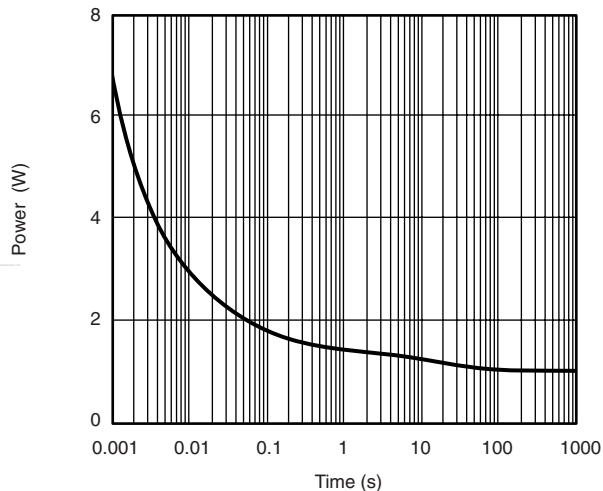
Normalized On-Resistance vs. Junction Temperature



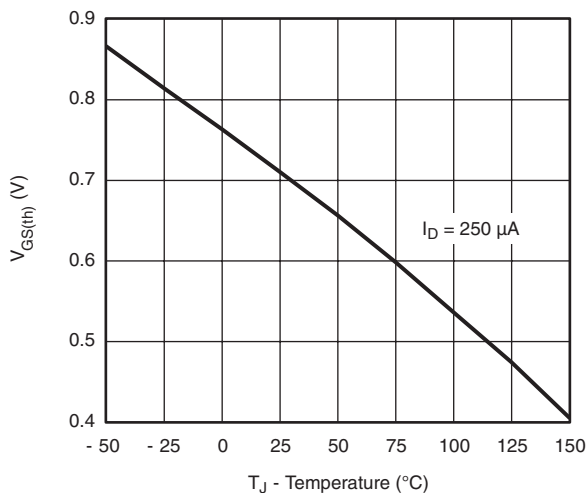
Source-Drain Diode Forward Voltage



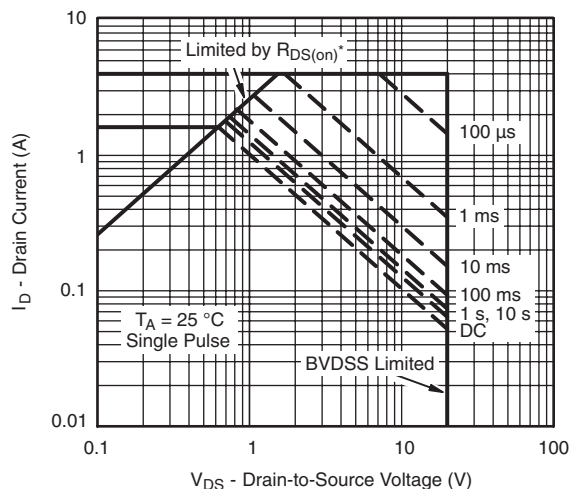
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Threshold Voltage

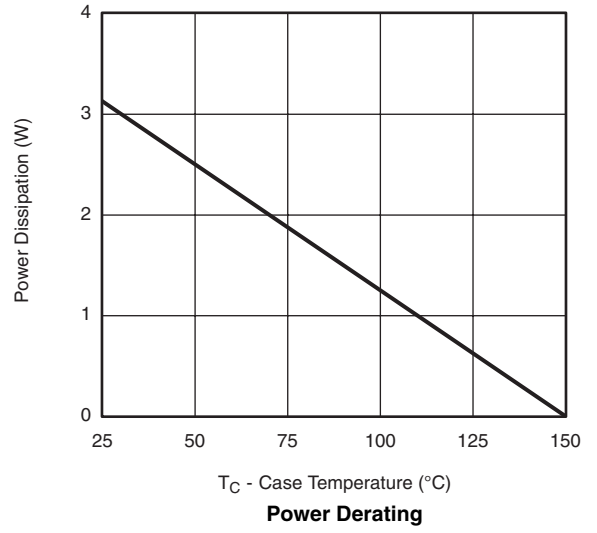
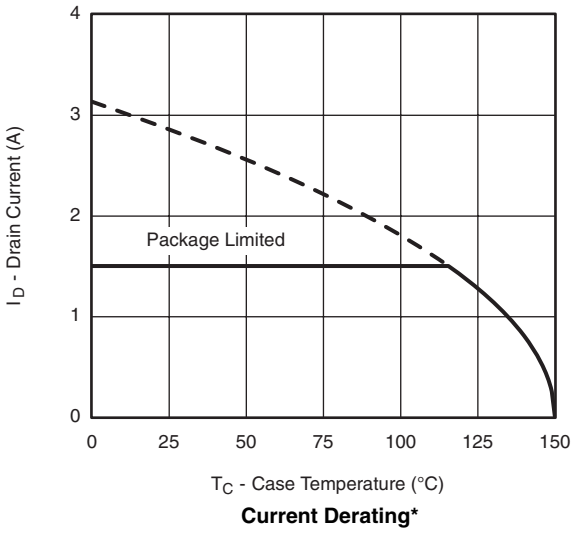


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient



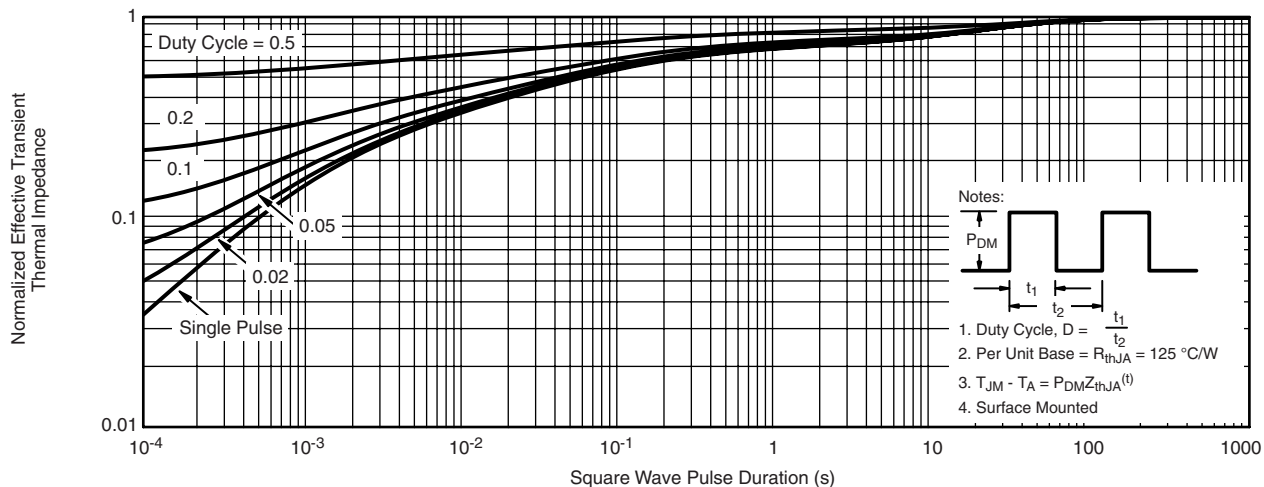
**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



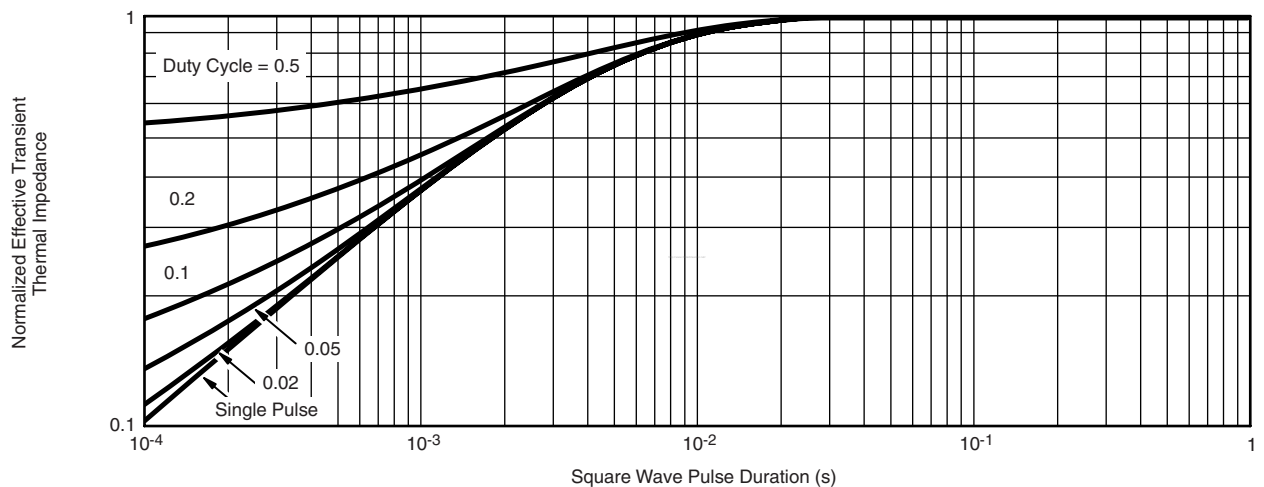
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?64808](http://www.vishay.com/ppg?64808).

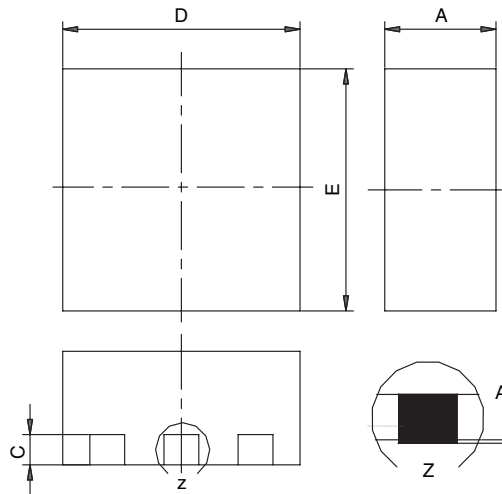


PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL

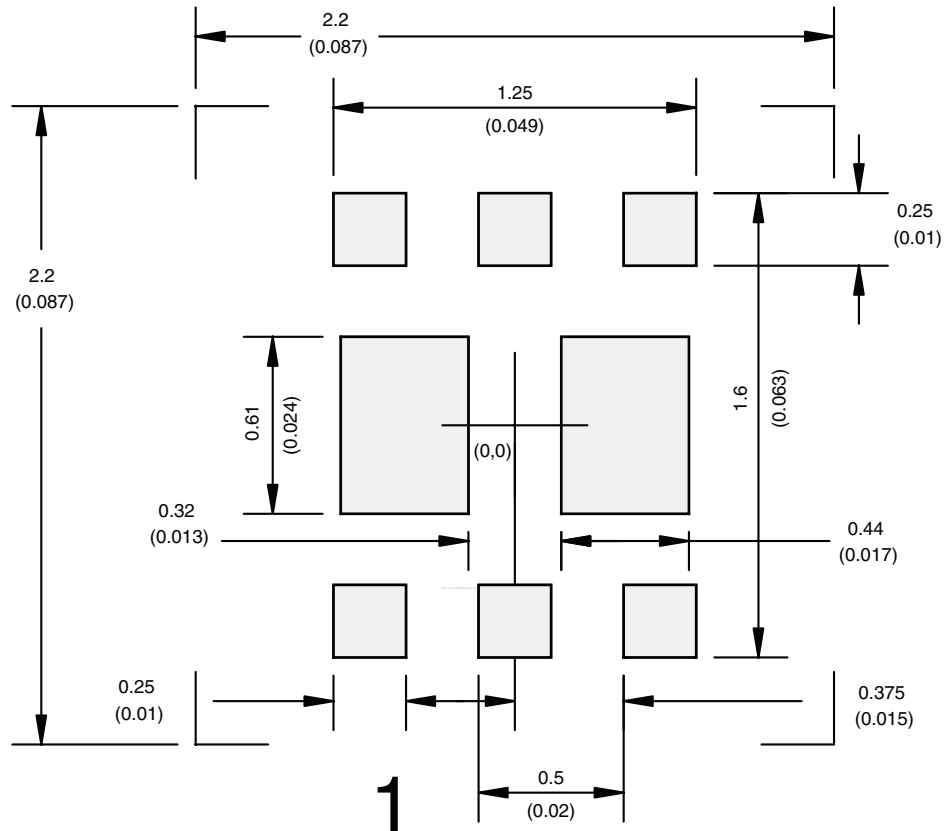


- Notes:  
 1. All dimensions are in millimeters  
 2. Package outline exclusive of mold flash and metal burr  
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07  
 DWG: 5935

## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Dual



Dimensions in mm/(Inches)

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