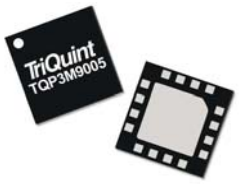
TQP3M9005

LNA Gain Block

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA
- General Purpose Wireless

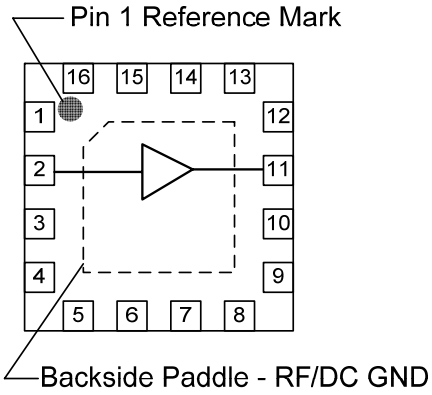


16-pin 3x3 QFN package

Product Features

- 50-4000 MHz
- 15.3 dB Gain @ 1.9 GHz
- 0.8 dB Noise Figure @ 1.9 GHz
- <1.5:1 I/O VSWR (>14 dB I/O Return Loss)
- +34 dBm Output IP3
- +22.3 dBm P1dB
- 50 Ohm Cascadable Gain Block
- Unconditionally Stable
- High Input Power Capability
- Single Supply, 50 mA Current

Functional Block Diagram



General Description

The TQP3M9005 is a high linearity low noise gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 15.3 dB gain, +34 dBm OIP3, and 0.8 dB Noise Figure while only drawing 50 mA current. The device is housed in a leadfree/green/RoHS-compliant industry-standard 16-pin 3x3mm QFN package.

The TQP3M9005 has the benefit of having high linearity while also providing very low noise across a broad range of frequencies. This allows the device to be used in both receive and transmit chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9005 covers the 0.05 - 4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Pin Configuration

Pin #	Symbol
2	RF Input
11	RF Output / Vdd
All Other Pins	N/C or GND
Backside Paddle	GND

Ordering Information

Part No.	Description
TQP3M9005	LNA Gain Block
TQP3M9005-PCB	0.5-4 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power,CW,50 Ω,T=25ºC	20 dBm
Device Voltage,Vdd	+7 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vdd	3	5	5.25	V
Tcase	-40		+85	°C
Tch (for>10^6 hours MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

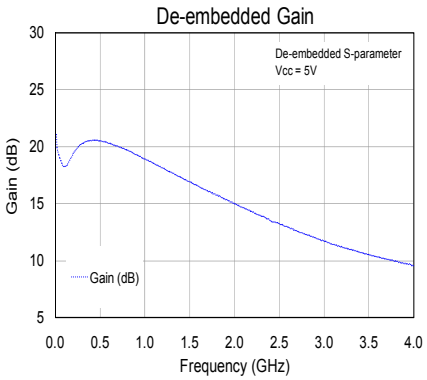
Electrical Specifications

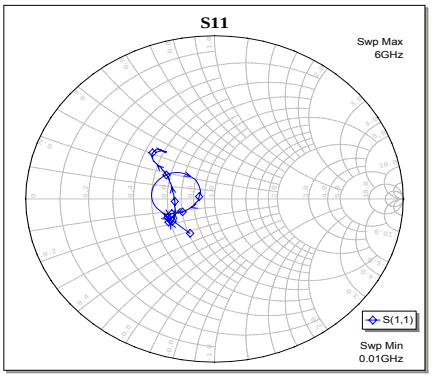
Test conditions unless otherwise noted: +25ºC, +5V, 50 Ω system.

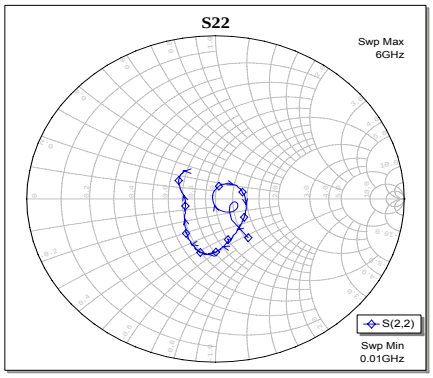
Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain		13.9	15.3	16.9	dB
Input Return Loss			12		dB
Output Return Loss			14		dB
Output P1dB			+22.3		dBm
Output IP3	See Note 1.	+30	+34		dBm
Noise Figure			0.8		dB
Supply Voltage, Vdd			+5		V
Current, Idd		35	50	68	mA
Thermal Resistance (junction to case) θ_{jc}			76.8		°C/W

Notes:
1. OIP3 is measured with two tones at an output power of +2 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule. 2:1 rule gives relative value with respect to fundamental tone.

Device Characterization Data





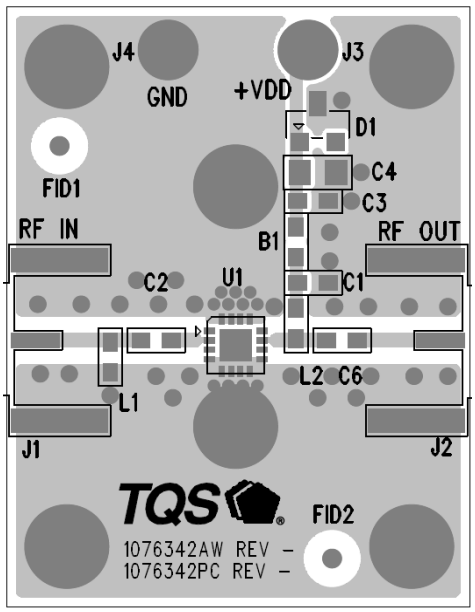


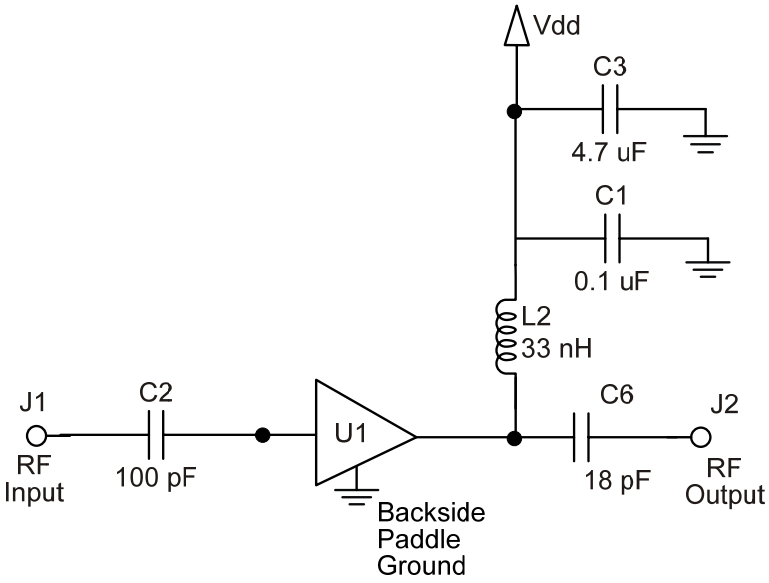
S-Parameter Data

V_{dd} = +5 V, I_{cq} = 50 mA, T = +25°C, unmatched 50 ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-10.60	-165.03	18.97	169.37	-28.21	3.31	-20.93	-16.62
100	-9.49	175.55	18.25	174.21	-28.93	7.02	-18.17	-16.66
200	-10.87	147.24	19.40	177.58	-27.58	15.94	-20.08	-53.04
400	-17.37	131.91	20.53	160.55	-26.03	13.26	-35.69	161.57
800	-19.08	-162.95	19.71	130.50	-25.55	10.38	-18.59	54.50
1000	-16.31	-155.70	18.89	118.70	-25.42	10.64	-17.17	35.91
1200	-14.56	-155.11	18.10	108.64	-25.21	11.47	-16.62	16.88
1500	-13.21	-157.04	16.88	94.87	-24.85	13.11	-15.65	-9.94
1900	-12.17	-158.41	15.32	79.10	-24.31	13.69	-14.06	-43.51
2000	-11.91	-158.36	14.97	75.77	-24.10	13.71	-13.59	-50.29
2200	-11.68	-157.13	14.26	68.76	-23.87	13.48	-12.60	-62.64
2500	-11.30	-155.40	13.24	59.49	-23.35	12.97	-11.28	-75.63
2600	-11.23	-154.34	12.92	56.53	-23.20	12.81	-10.96	-79.40
3000	-11.03	-150.07	11.67	45.14	-22.54	11.37	-9.77	-89.57
3500	-11.47	-147.07	10.53	31.94	-21.61	7.86	-9.39	-100.67
4000	-13.13	-160.94	9.56	16.71	-20.66	1.90	-10.56	-116.49

Application Circuit Configuration





Notes:

1. See PC Board Layout, under Applications information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. All components are of 0603 size unless stated on the schematic.
5. C6 and L2 value are critical for linearity performance.

Bill of Material: TQP3M9005-PCB

Reference Desg.	Value	Description	Manufacturer	Part Number
U1		High Linearity LNA Gain Block	TriQuint	TQP3M9005
C2	100 pF	Cap, Chip, 0603, 50V, NPO, 5%	various	
C6	18 pF	Cap, Chip, 0603, 50V, NPO, 5%	various	
C1	0.1 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
L2	33 nH	Ind, Chip, 0603, 5%	various	
C3	4.7 uF	Cap, Chip, 0603, 6.3V, X5R, 20%	various	
B1	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	
L1, D1, C4	Do Not Place		various	

Typical Performance TQP3M9005-PCB

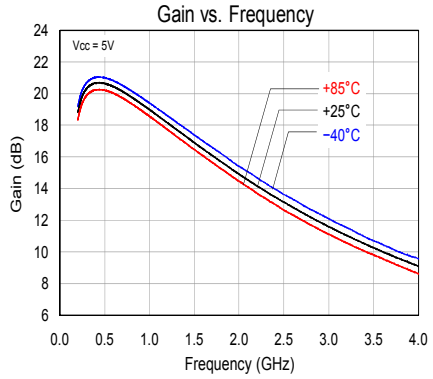
Test conditions unless otherwise noted: +25ºC, +5V, 50 mA, 50 Ω system. The data shown below is measured on TQP3M9005-PCB

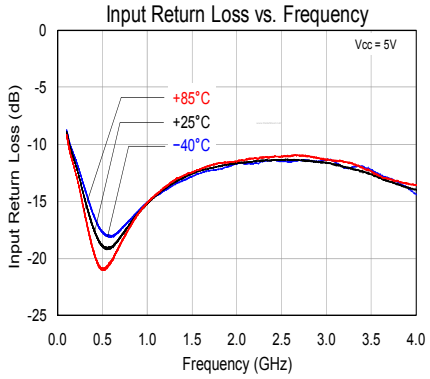
Frequency	MHz	500	900	1900	2100	2600
Gain	dB	20.6	19.4	15.3	14.5	12.8
Input Return Loss	dB	19	16	12	11	11
Output Return Loss	dB	17	16	14	13	11
Output P1dB	dBm	+22.2	+22.2	+22.3	+22.5	+22.5
OIP3 [1]	dBm	+32	+32.9	+34.0	+33.6	+33.8
Noise Figure [2]	dB	1.0	0.9	0.8	0.85	1.1

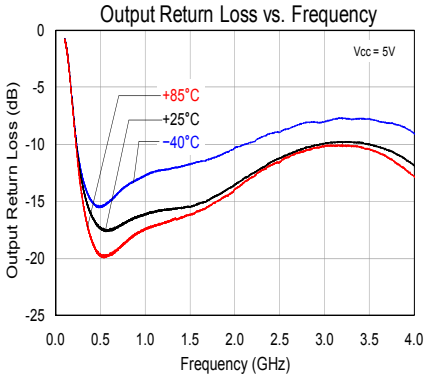
Notes:
1. OIP3 measured with two tones at an output power of +2 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board and corrected for the board loss of 0.11 dB @ 0.5 GHz, board loss of 0.08dB @ 0.9 GHz, board loss of 0.13dB @ 1.9 GHz, board loss of 0.14dB @ 2.1 GHz and board loss of 0.17dB @ 2.6 GHz.

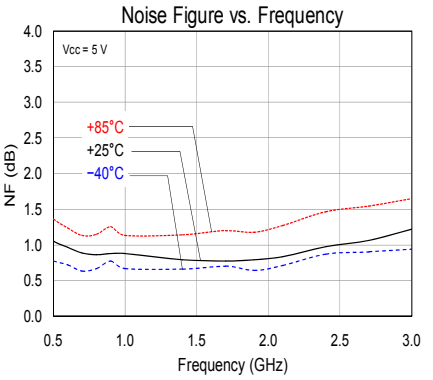
Performance Plots

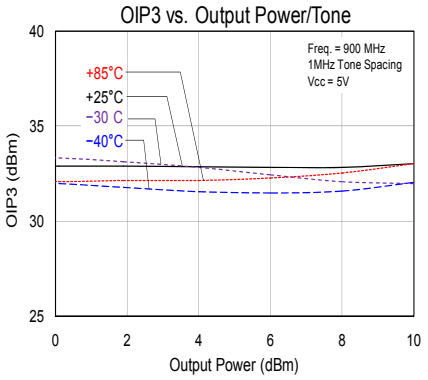
Performance plots data is measured using TQP3M9005-PCB. Noise figure plot has been corrected for evaluation board loss of around 0.13dB @ 1.9 GHz.

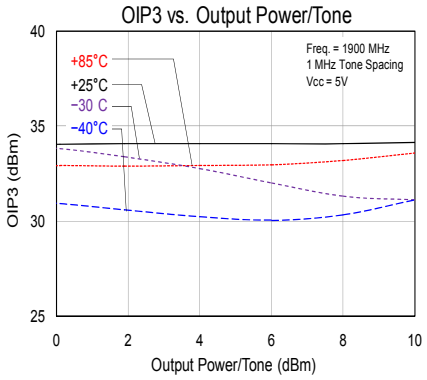




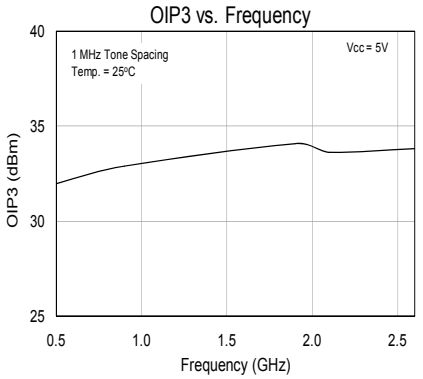


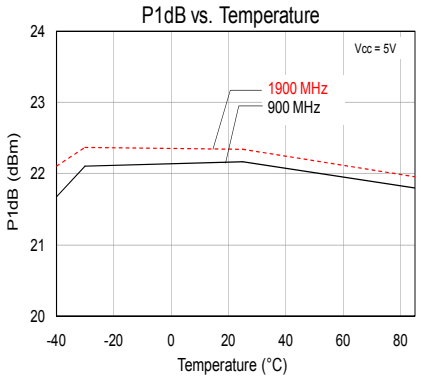


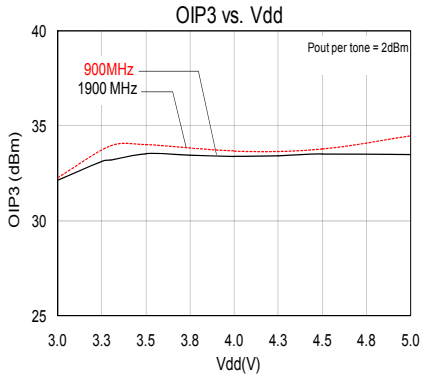


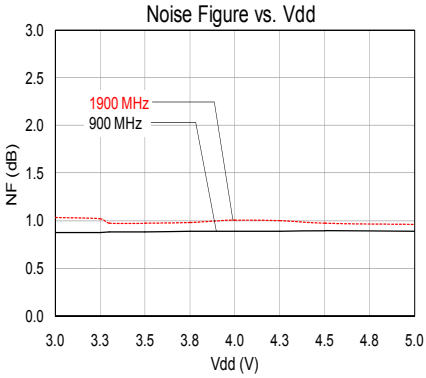


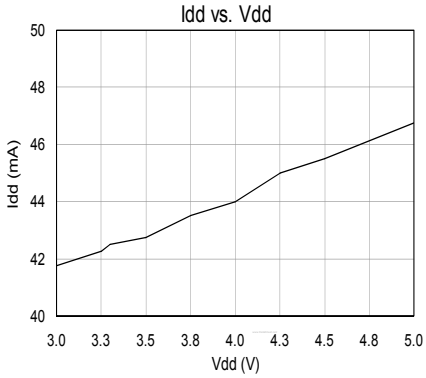
Performance Plots

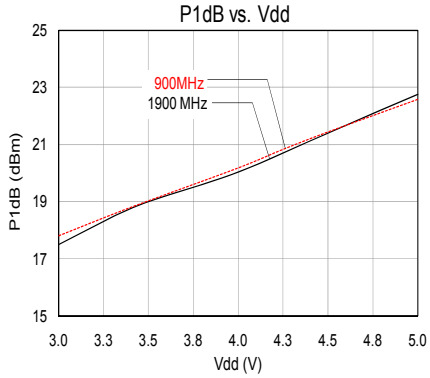








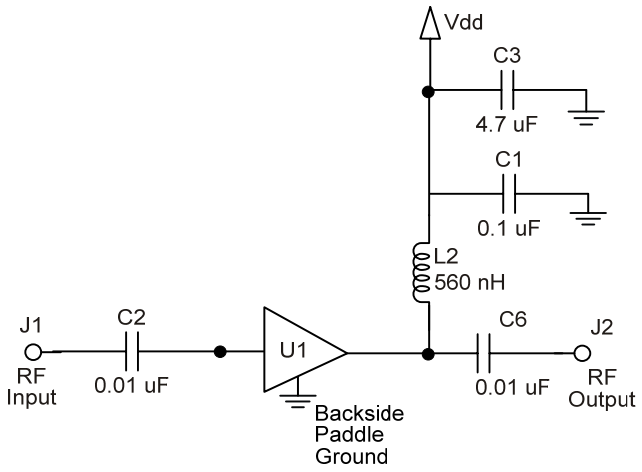




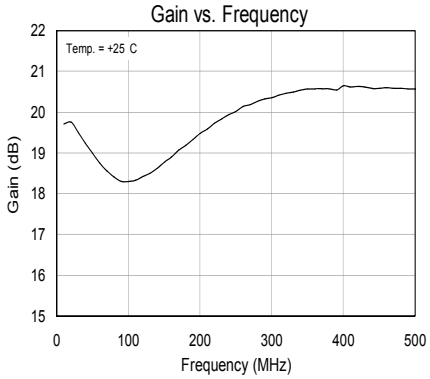
TQP3M9005 Low Frequency Performance

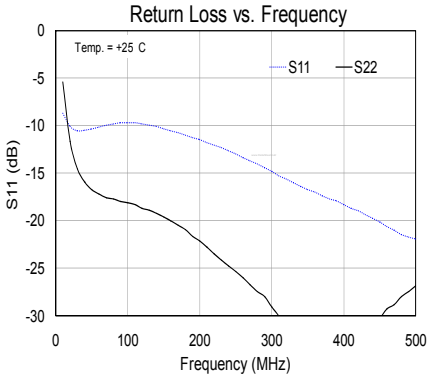
Test conditions unless otherwise noted: +25ºC, +5V, 50 mA, 50 Ω system.

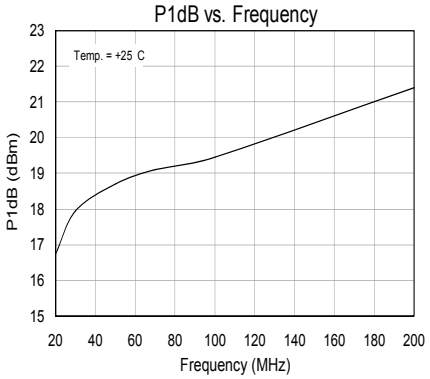
Frequency	MHz	50	100	200
Gain	dB	18.9	18.3	19.4
Input Return Loss	dB	10	9.7	11.5
Output Return Loss	dB	16	18	22
Output P1dB	dBm	+18.7	+19.45	+21.4
OIP3	dBm	+29.2	+29.7	+27.5
Noise Figure	dB	6.6	5.1	2.9

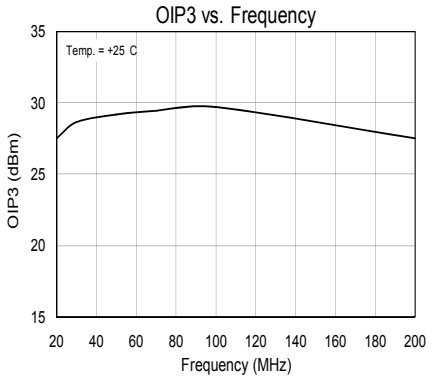


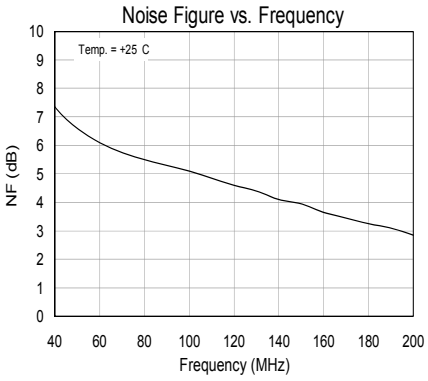
Performance Plots



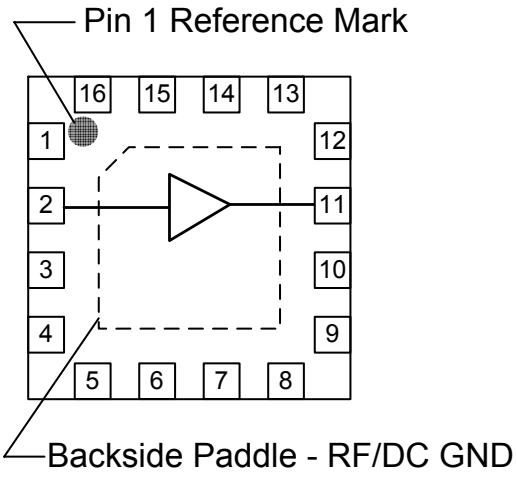








Pin Description



Pin	Symbol	Description
2	RF Input	Input, matched to 50 ohms. External DC Block is required.
11	Vdd / RFout	Output, matched to 50 ohms, External DC Block is required and supply voltage.
All other pins	GND	These pins are not connected internally but are recommended to be grounded on the PCB for optimal isolation.
	GND Paddle	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see PCB mounting pattern in Mechanical Information section.

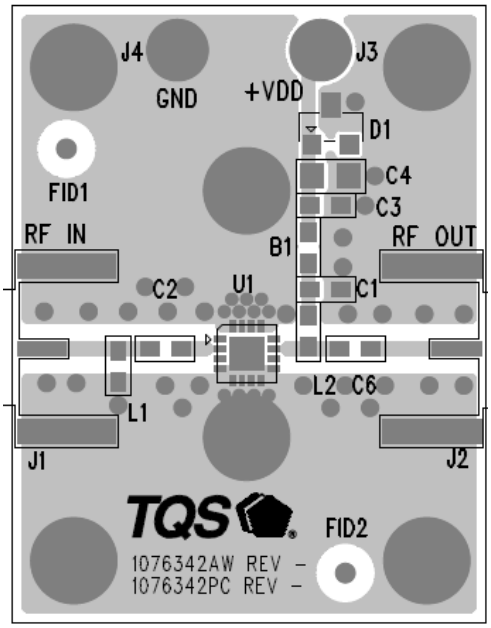
Applications Information

PC Board Layout

Top RF layer is .014" NELCO N4000-13, ϵ_r = 3.9, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035"

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

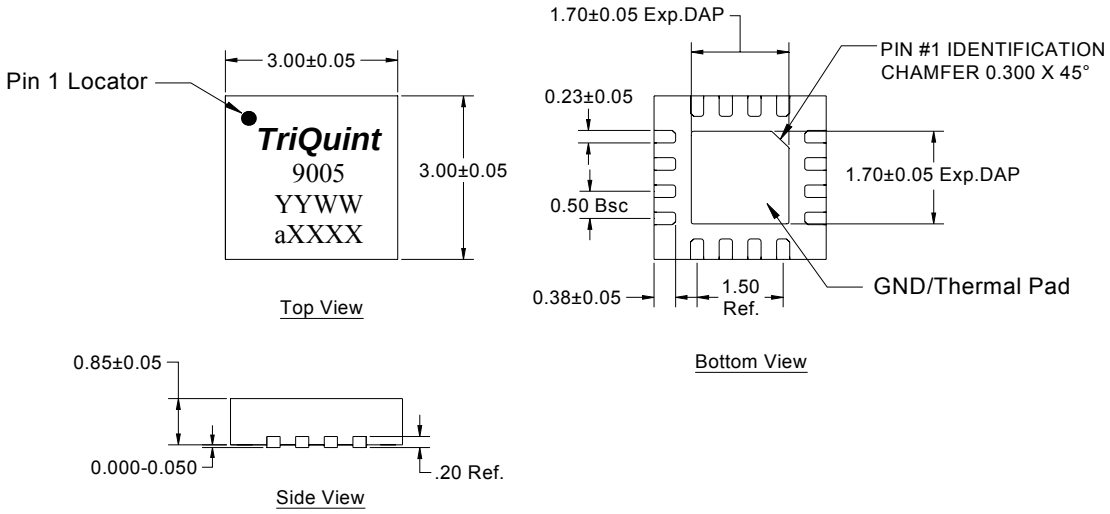
For further technical information, Refer to www.TriQuint.com



Mechanical Information

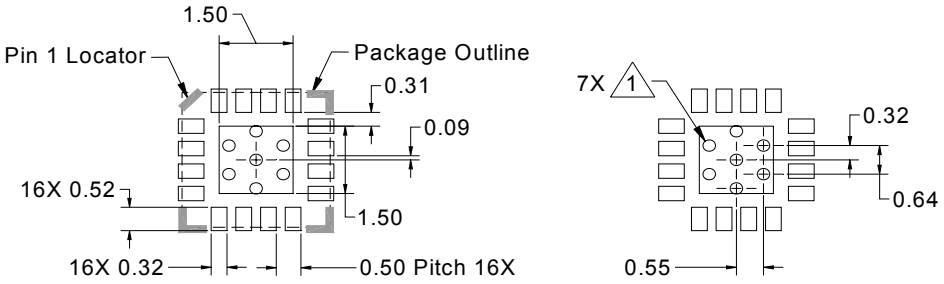
Package Information and Dimensions

Marking: Part number: 9005
Year, Week Code: YYWW
Assembly Code: aXXXX



NOTES:
1. All dimensions are in millimeters. Angles are in degrees.

PCB Mounting Pattern



COMPONENT SIDE

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance
3. Ground/thermal vias are required for the proper operation of this device. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250 V to < 500 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Moisture Sensitivity Level 1 at 260°C per IPC/JEDEC J-STD-020.

Solderability

Package contact plating: Annealed matte tin.

Compatible with both lead-free (maximum 260°C reflow temperature) and lead (maximum 245°C reflow temperature) soldering processes.

The part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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