P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package						
			TO-39	TO-52	TO-92	TO-220	Quad P-DIP	Quad C-DIP*	DICE†
-40V	8Ω	-0.5A	VP0104N2	VP0104N9	VP0104N3	VP0104N5	VP0104N6	VP0104N7	VP0104ND
-60V	8Ω	-0.5A	VP0106N2	VP0106N9	VP0106N3	VP0106N5	VP0106N6	VP0106N7	VP0106ND
-90V	8Ω	-0.5A	VP0109N2	VP0109N9	VP0109N3	VP0109N5	—	—	VP0109ND

* 14 pin side brazed ceramic DIP
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

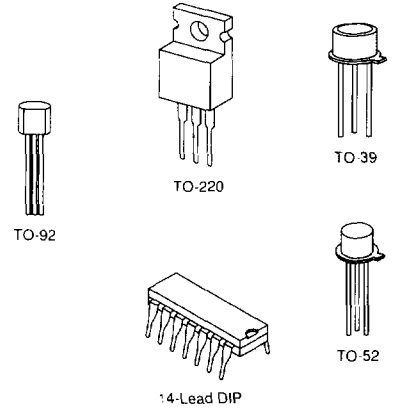
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed) @ T_C = 25°C	Power Dissipation °C/W	θ_{ja} °C/W	θ_{jc}	I_{DR}*	I_{DRM}
TO-39	-0.45A	-1.0A	3.5W	125	35	-0.5A	-1.0A
TO-52	-0.25A	-1.0A	1.0W	170	125	-0.4A	-1.0A
TO-92	-0.25A	-0.8A	1.0W	170	125	-0.4A	-0.8A
TO-220	-1.0A	-1.0A	15.0W	70	8.3	-1.0A	-1.0A
Plastic Dip	Refer to Arrays & Special Functions Section.						
Ceramic Dip							

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

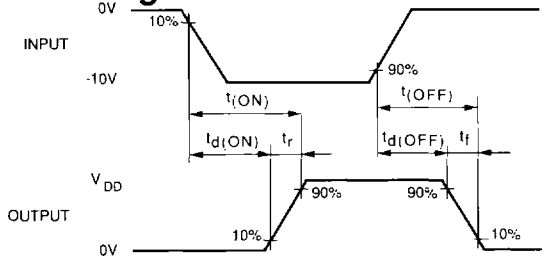
(Notes 1 and 2)

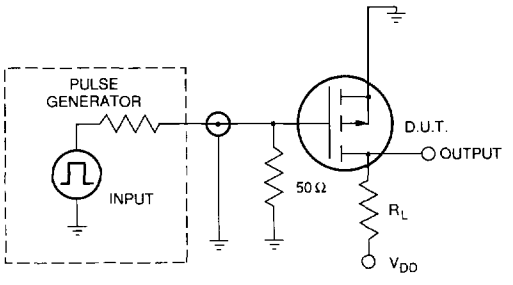
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0109	-90			V	I_D = -1.0mA, V_{GS} = 0
		VP0106	-60				
		VP0104	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			5.8	6.5	mV/°C	I_D = -1.0mA, V_{GS} = V_{DS}
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.15	-0.25		A	V_{GS} = -5V, V_{DS} = -25V
			-0.50	-1.0			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			11	15	Ω	V_{GS} = -5V, I_D = -0.1A
				5	8		V_{GS} = -10V, I_D = -0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	I_D = -0.5A, V_{GS} = -10V
G_{FS}	Forward Transconductance		150	200		m℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			22	30		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	6	ns	V_{DD} = -25V, I_D = -1A, R_S = 50Ω
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	5		
t_f	Fall Time			4	6		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I_{SD} = -1.0A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = -1.0A, V_{GS} = 0

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

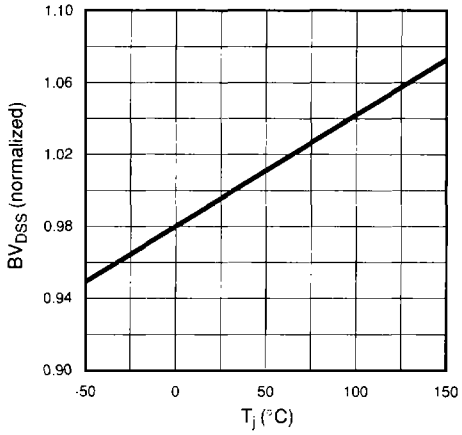
Switching Waveforms and Test Circuit



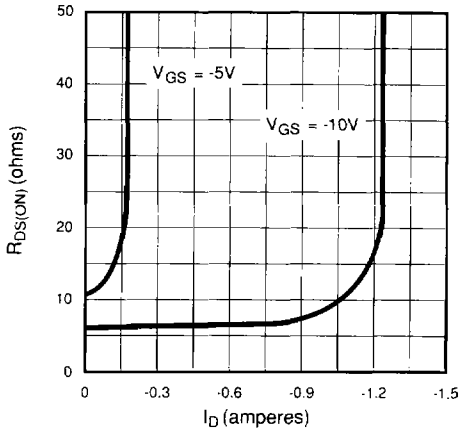


Typical Performance Curves

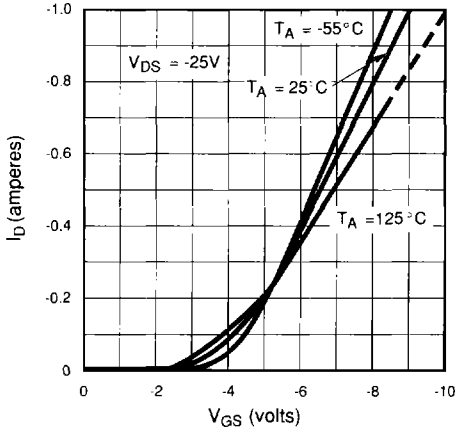
BV$_{DSS}$ Variation with Temperature



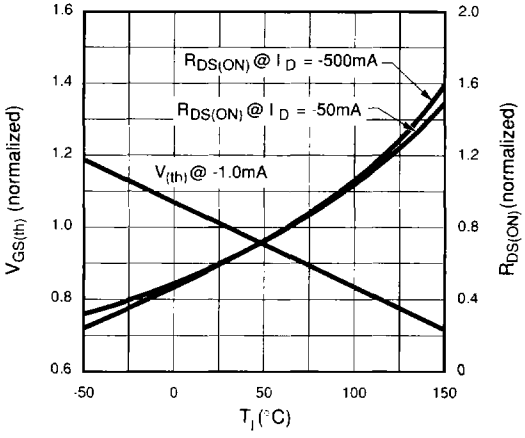
On-Resistance vs. Drain Current



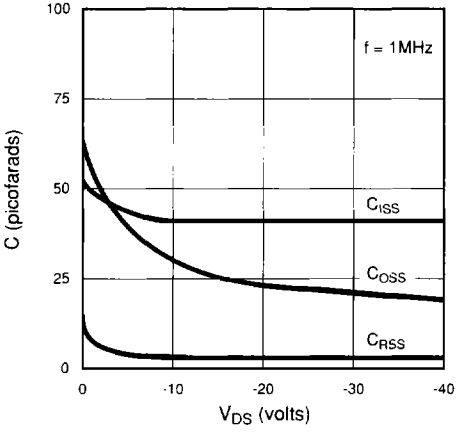
Transfer Characteristics



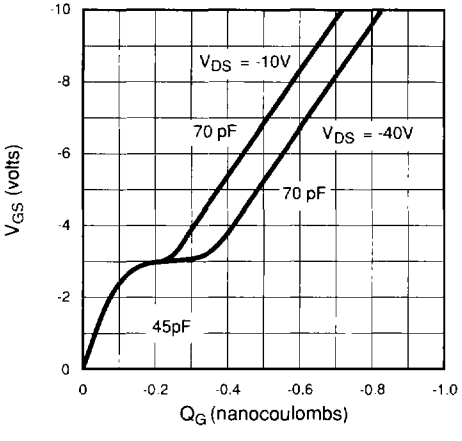
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



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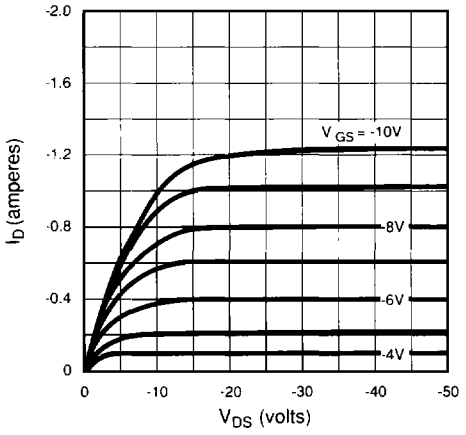
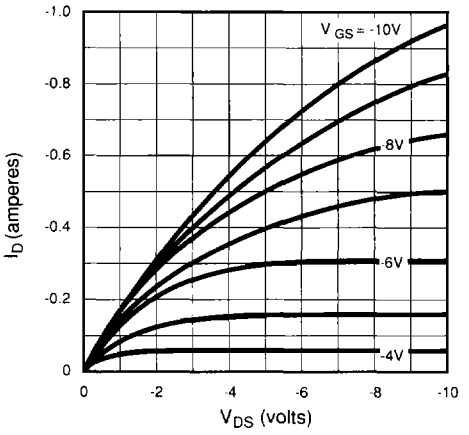
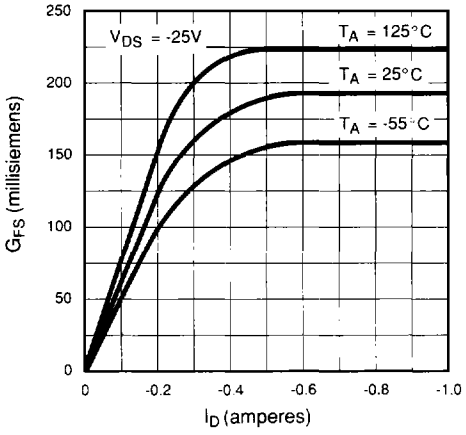
Output Characteristics



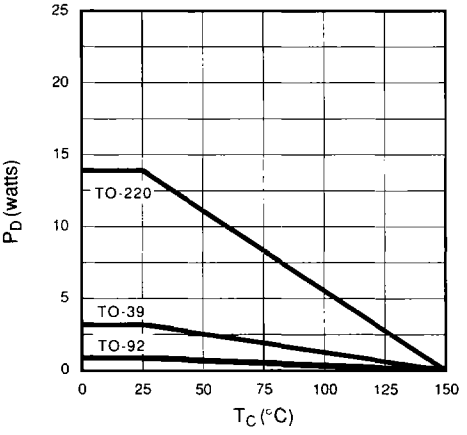
Saturation Characteristics



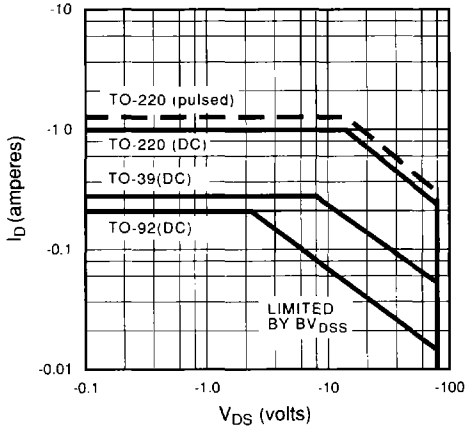
Transconductance vs. Drain Current



Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics