STD4N52K3, STF4N52K3, STP4N52K3, STU4N52K3

N-channel 525 V, 2.5 A, 2.1 Ω typ., SuperMESH3™ Power MOSFET in DPAK, TO-220FP, TO-220 and IPAK packages

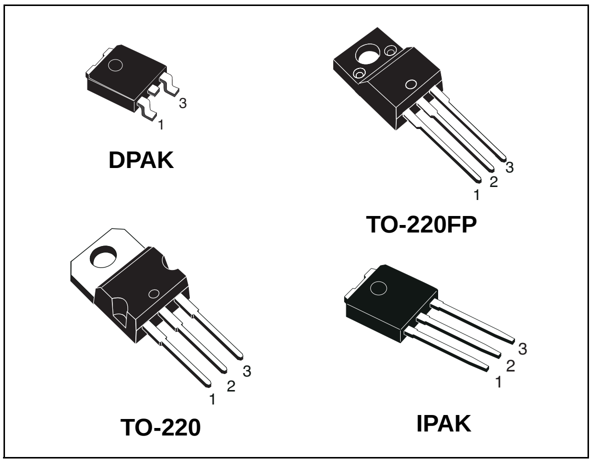
Datasheet — production data

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STD4N52K3	525 V	< 2.6 Ω	2.5 A	45 W
STF4N52K3			2.5 A	20 W
STP4N52K3			2.5 A (1)	45 W
STU4N52K3			2.5 A	45 W

1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected



Application

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Figure 1. Internal schematic diagram

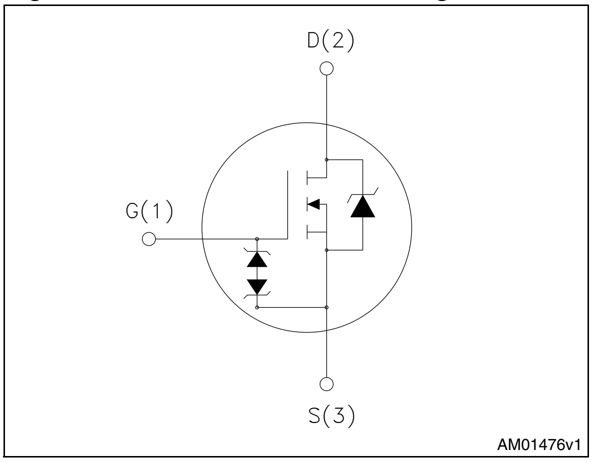


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD4N52K3	4N52K3	DPAK	Tape and reel
STF4N52K3	4N52K3	TO-220FP	Tube
STP4N52K3	4N52K3	TO-220	Tube
STU4N52K3	4N52K3	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	DPAK	IPAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	525				V
V_{GS}	Gate- source voltage	± 30				V
I_D	Drain current (continuous) at T_C = 25 °C	2.5			2.5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	2			2 (1)	A
I_{DM} (2)	Drain current (pulsed)	10			10 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	45			20	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	1.3				A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	110				mJ
dv/dt (3)	Peak diode recovery voltage slope	12				V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)				2500	V
T_{stg}	Storage temperature	-55 to 150				°C
T_j	Max. operating junction temperature	150				°C

1. Limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 2.5 A, di/dt = 400 A/μs, peak $V_{DD} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	DPAK	IPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	2.78			6.25	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb max		50			°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		100	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300		300		°C

1. When mounted on 1inch sq FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	525			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 525 V V_{DS} = 525 V, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.25 A		2.1	2.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	334 28 5	-	pF pF pF
$C_{oss(eq)}$ (1)	Equivalent output capacitance time related	V_{DS} = 0 to 420 V, V_{GS} = 0	-	20	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 2.5 A, V_{GS} = 10 V (see *Figure 19*)	-	11 2 7	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 260 V, I_D = 1.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 18*)	-	8 7 21 14	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		2.5 10	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 2.5 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 2.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 23*)	-	173 778 9		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 2.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 23*)	-	196 941 10		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-		V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

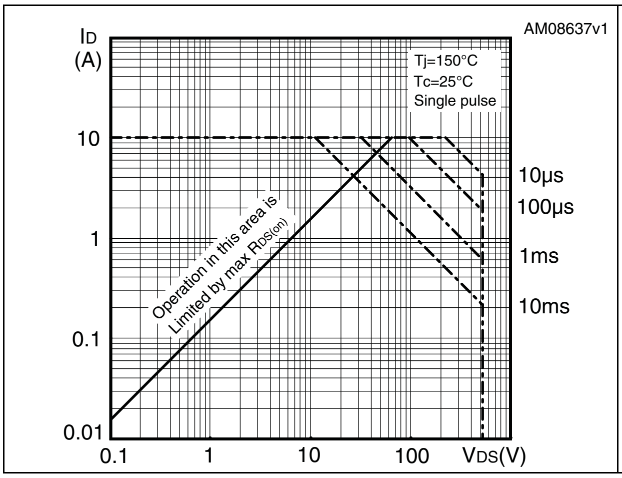


Figure 3. Thermal impedance for TO-220

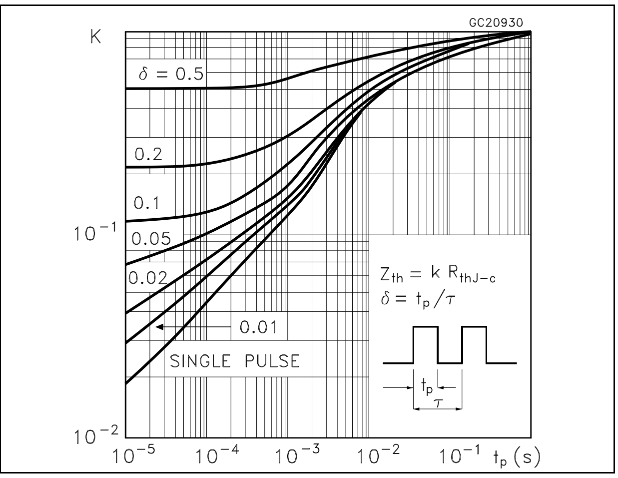


Figure 4. Safe operating area for TO-220FP

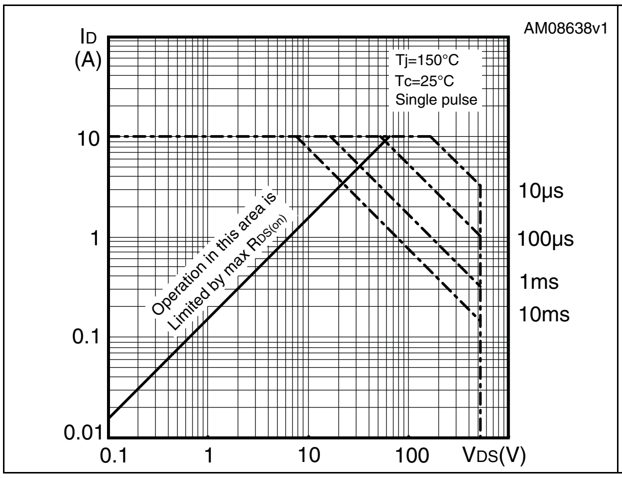


Figure 5. Thermal impedance for TO-220FP

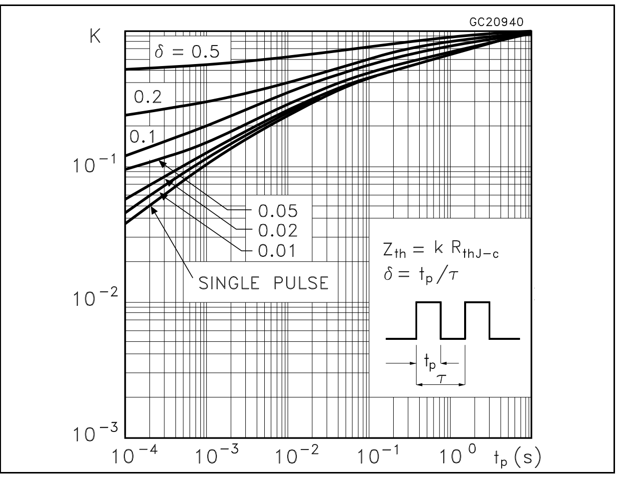


Figure 6. Safe operating area for DPAK, IPAK

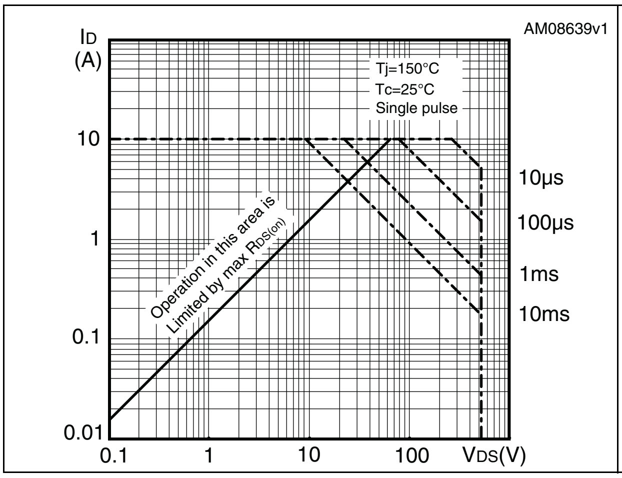


Figure 7. Thermal impedance for DPAK, IPAK

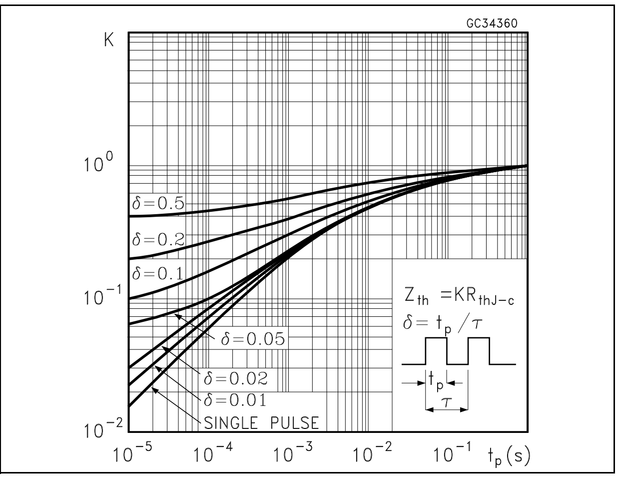


Figure 8. Output characteristics

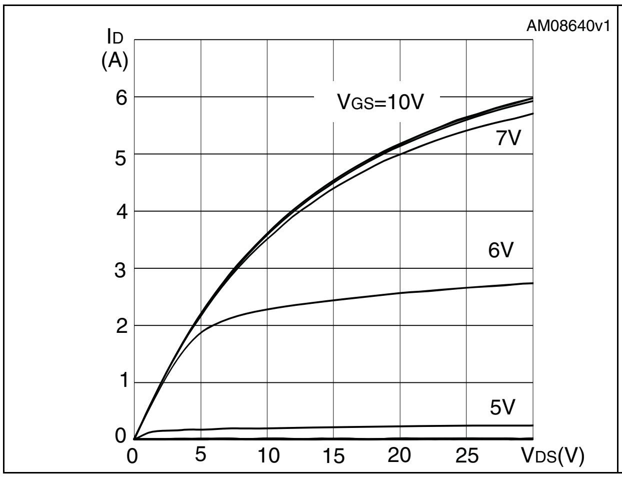


Figure 9. Transfer characteristics

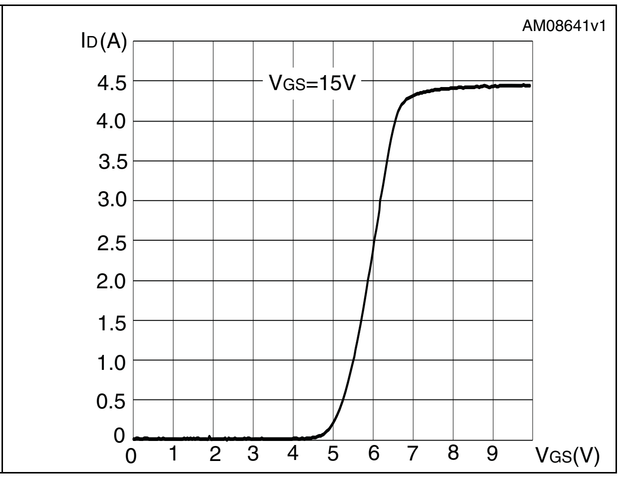


Figure 10. Normalized B_{VDSS} vs temperature

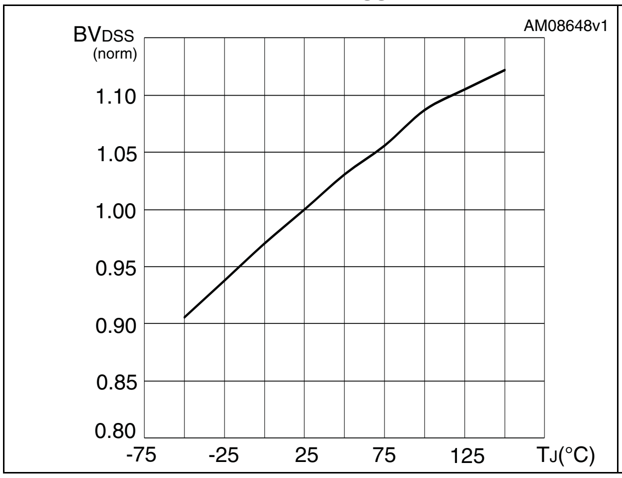


Figure 11. Static drain-source on-resistance

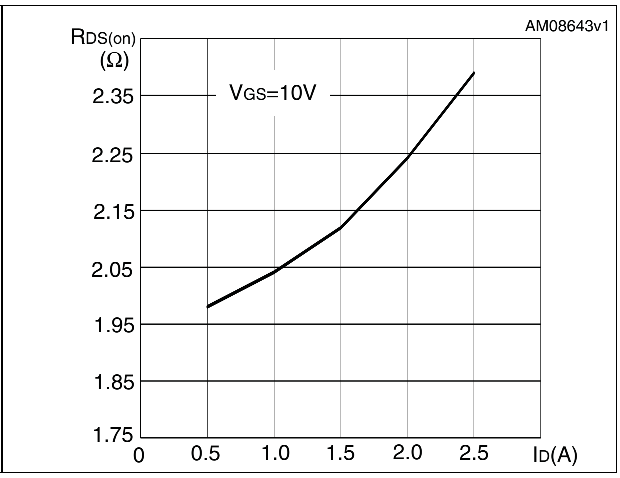


Figure 12. Capacitance variations

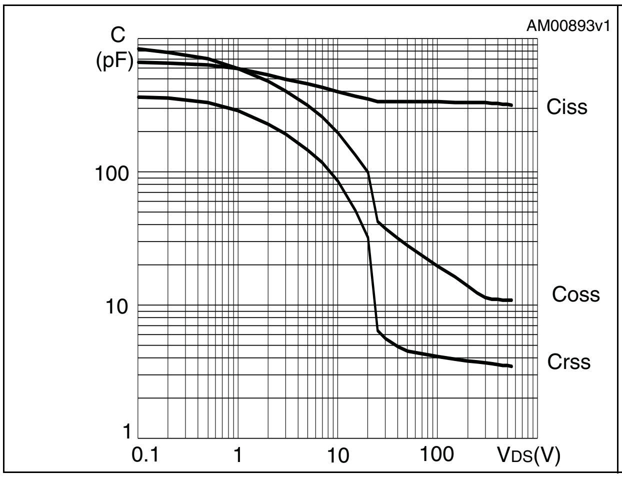


Figure 13. Gate charge vs gate-source voltage

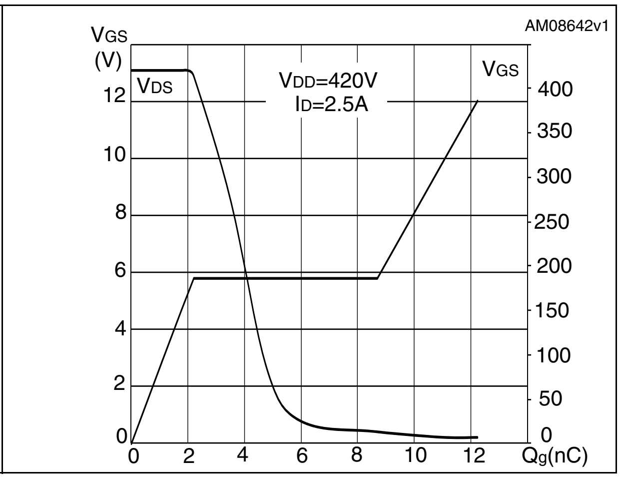


Figure 14. Normalized gate threshold voltage vs temperature

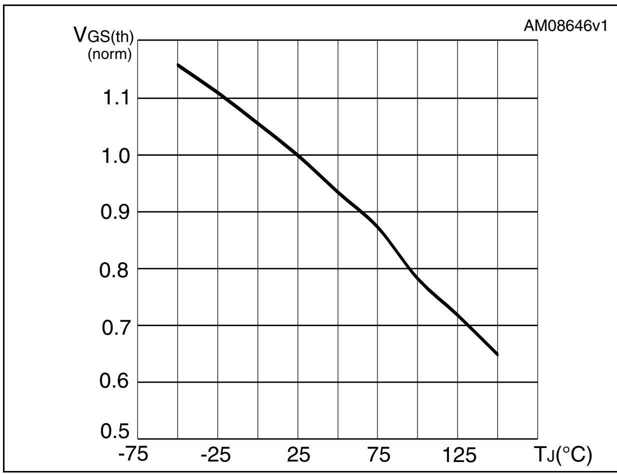


Figure 15. Normalized on-resistance vs temperature

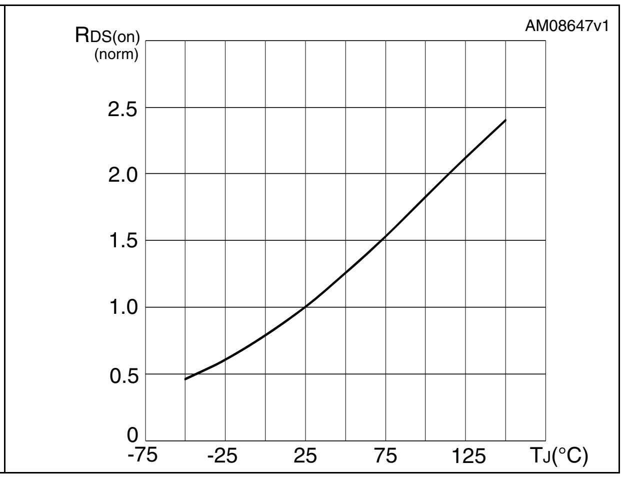


Figure 16. Source-drain diode forward characteristics

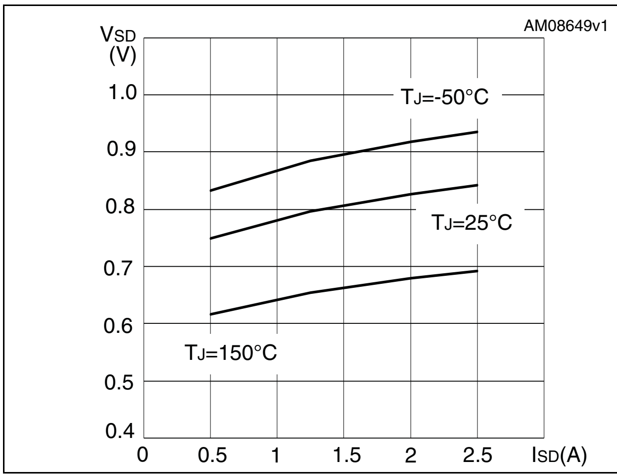
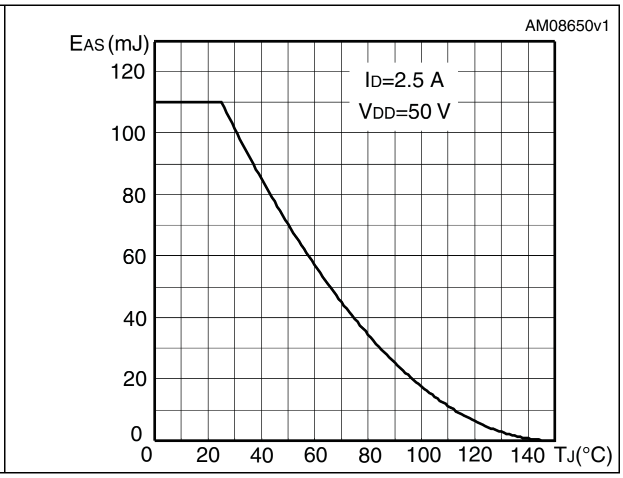


Figure 17. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 18. Switching times test circuit for resistive load

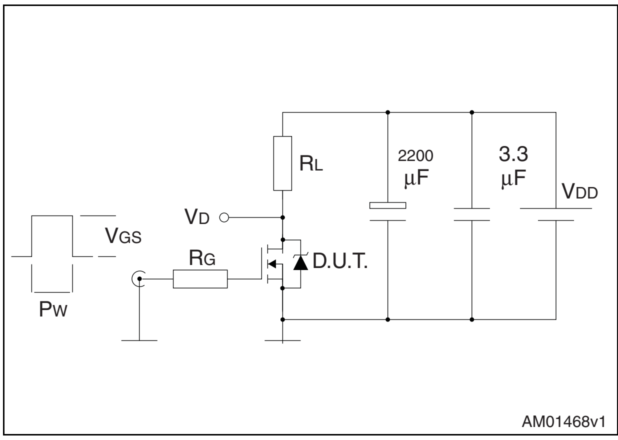


Figure 19. Gate charge test circuit

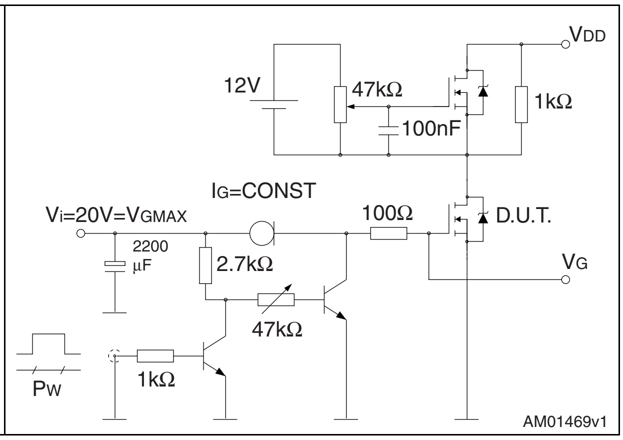


Figure 20. Test circuit for inductive load switching and diode recovery times

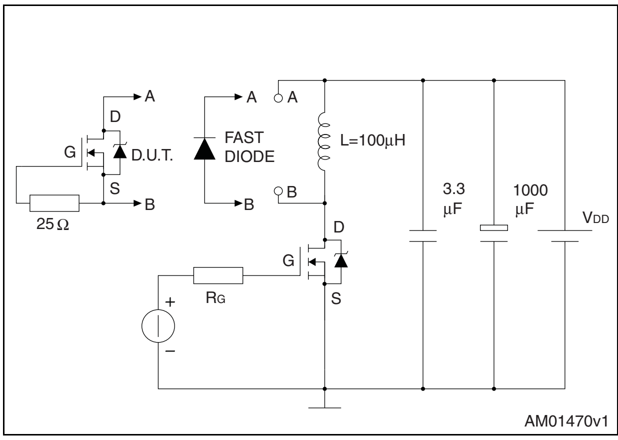


Figure 21. Unclamped Inductive load test circuit

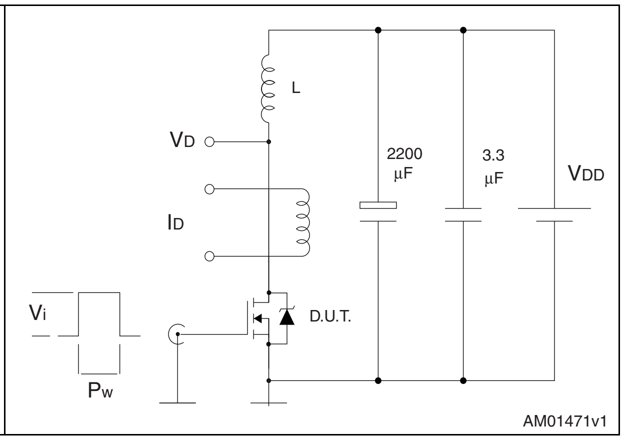


Figure 22. Unclamped inductive waveform

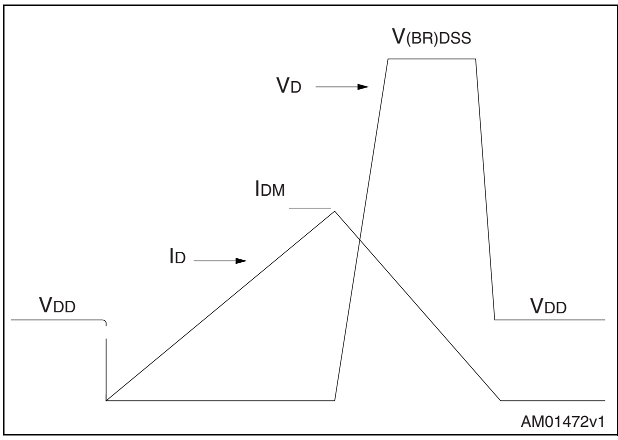
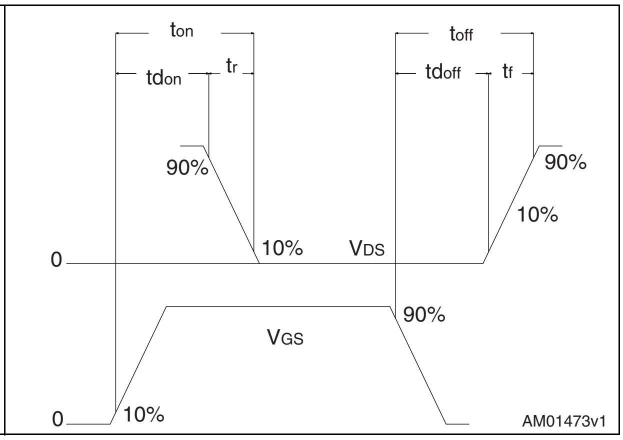


Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) drawing

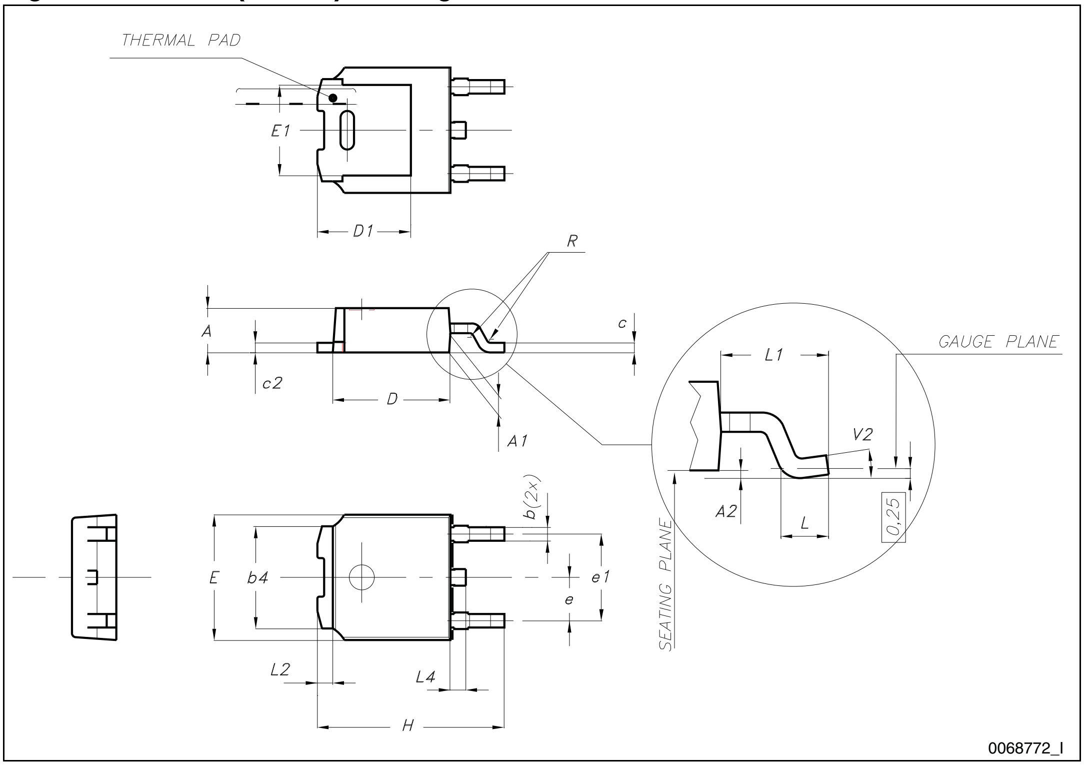
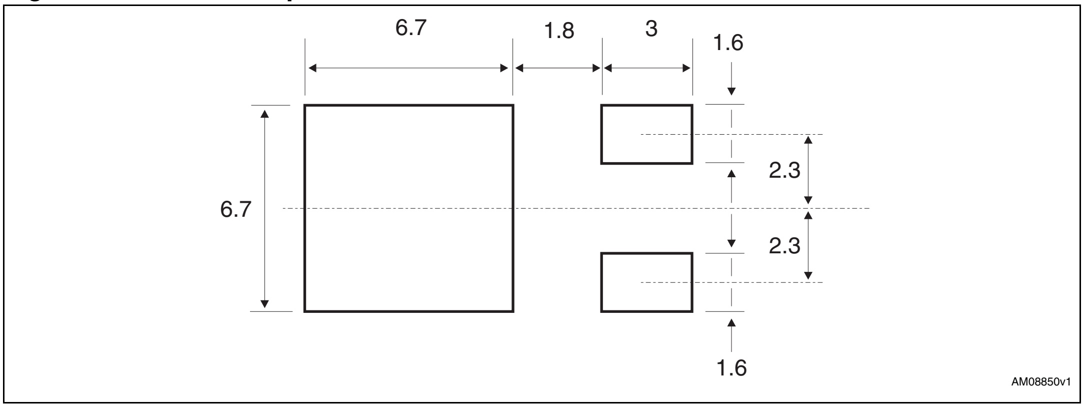


Figure 25. DPAK footprint[(a)]



a. All dimensions are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing

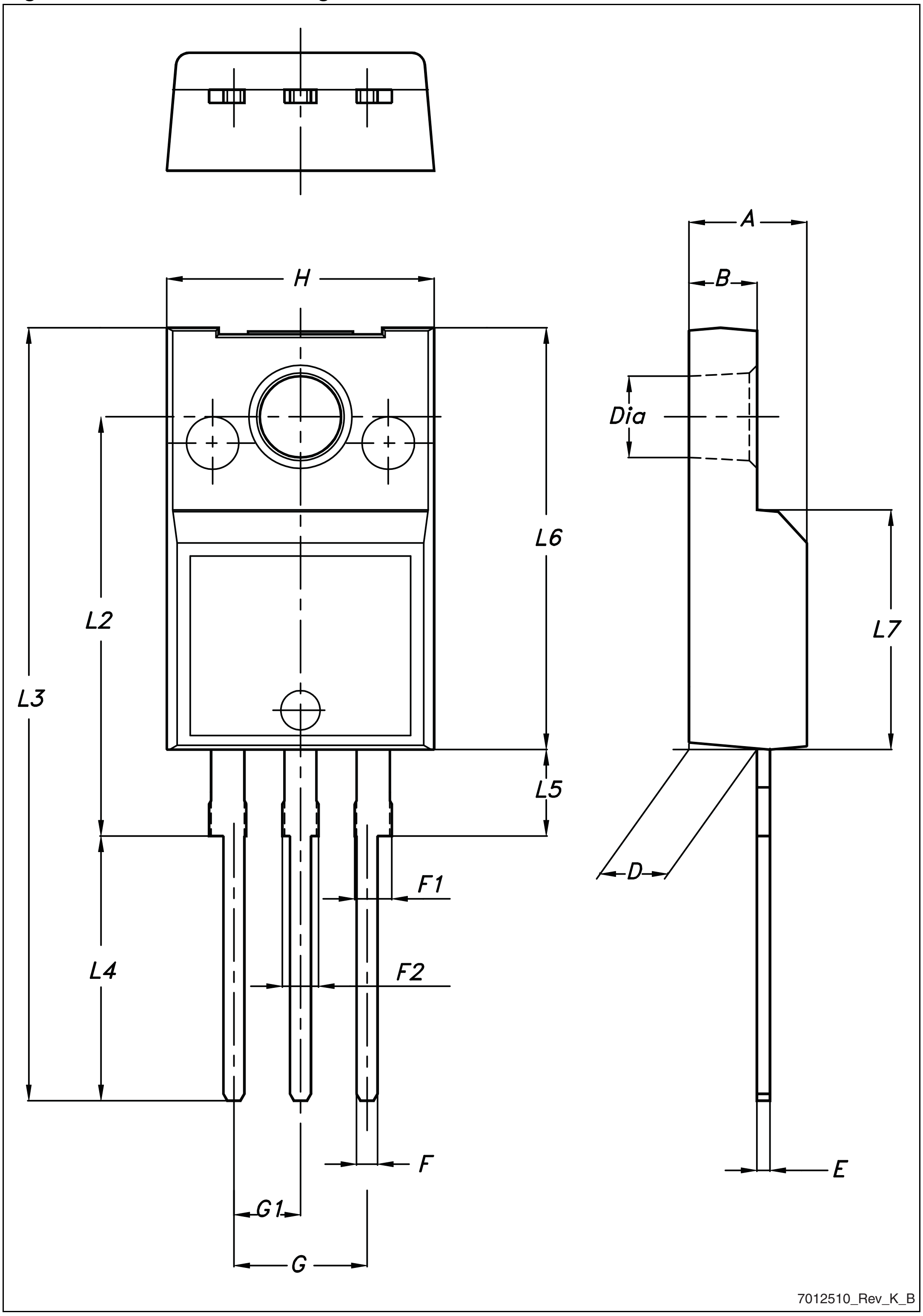


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

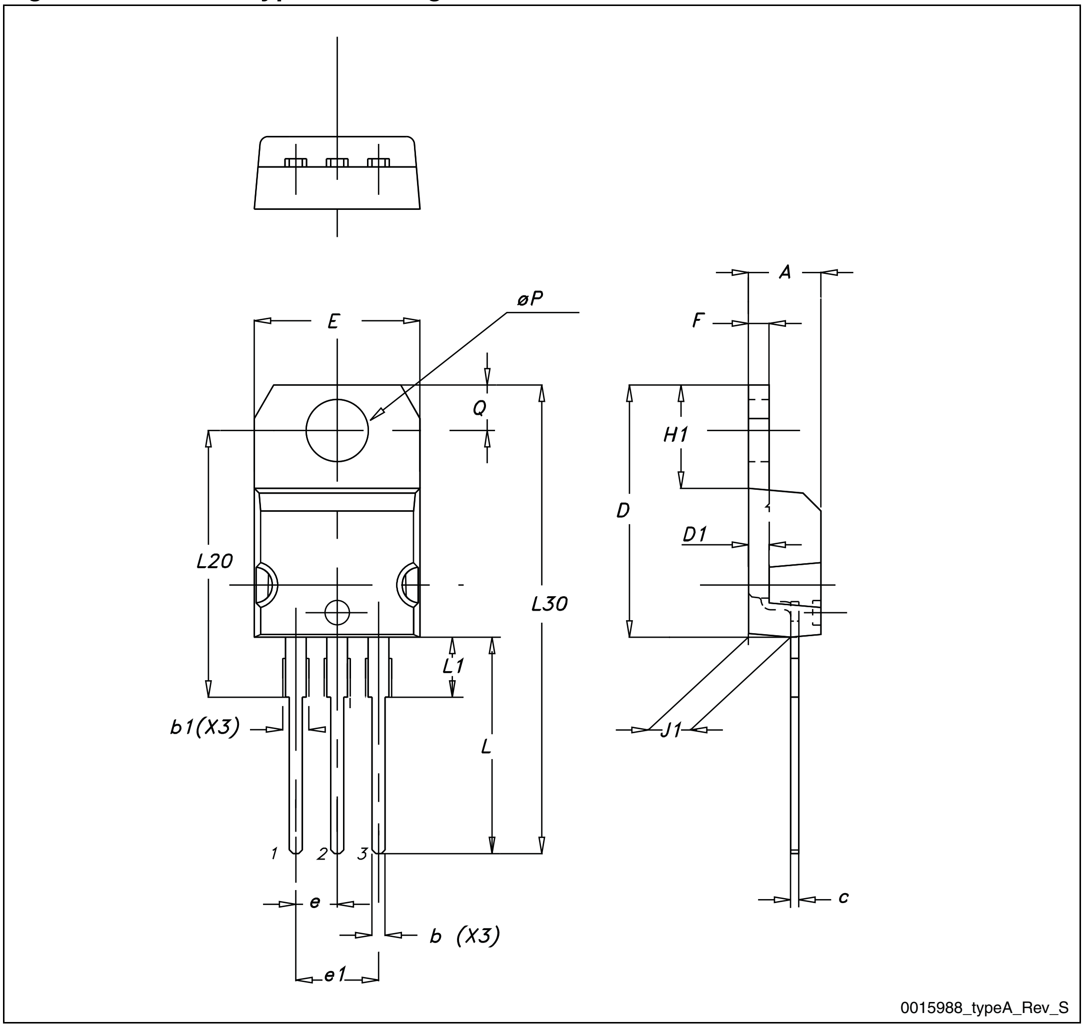
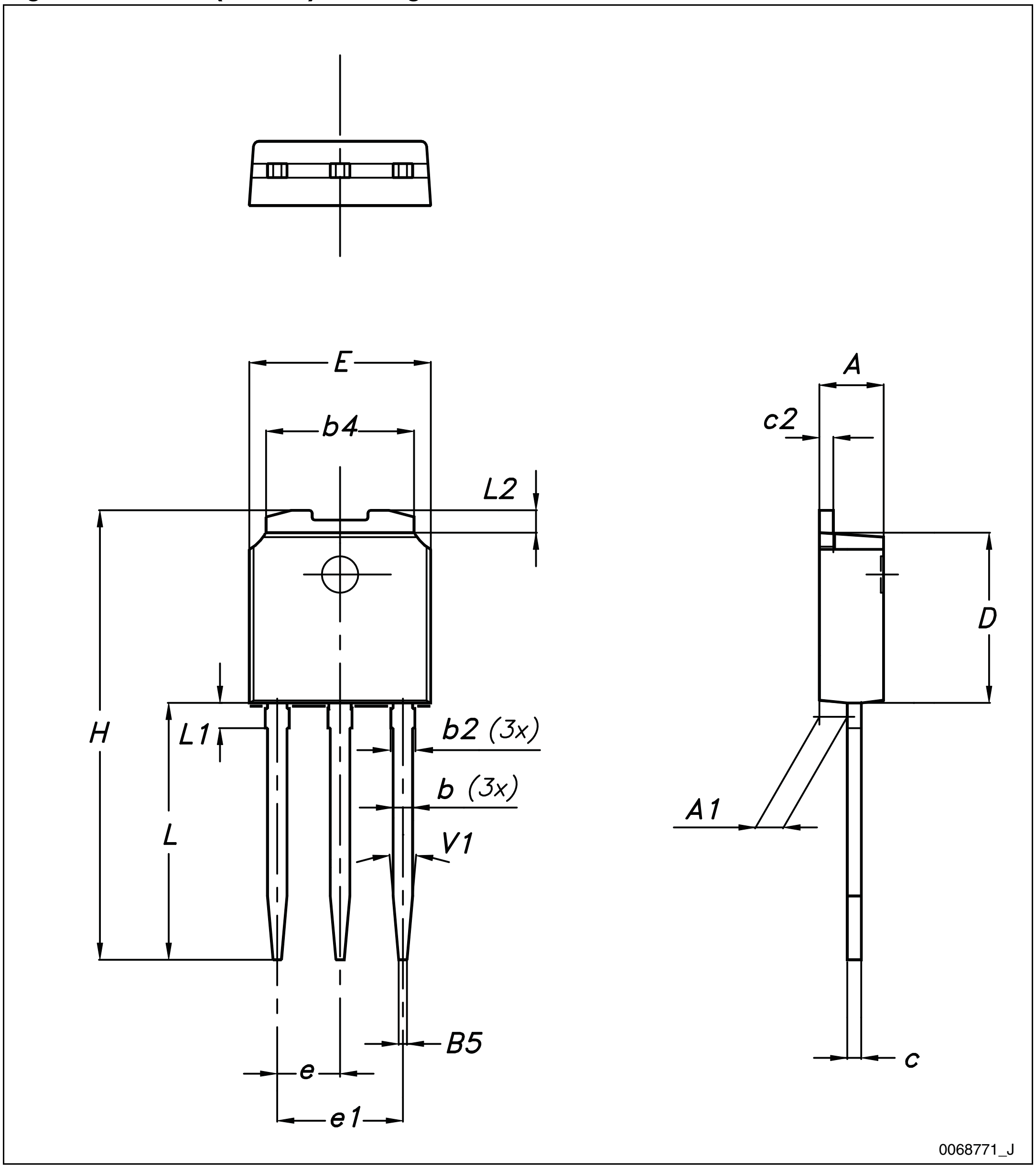


Table 12. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 28. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 29. Tape for DPAK (TO-252)

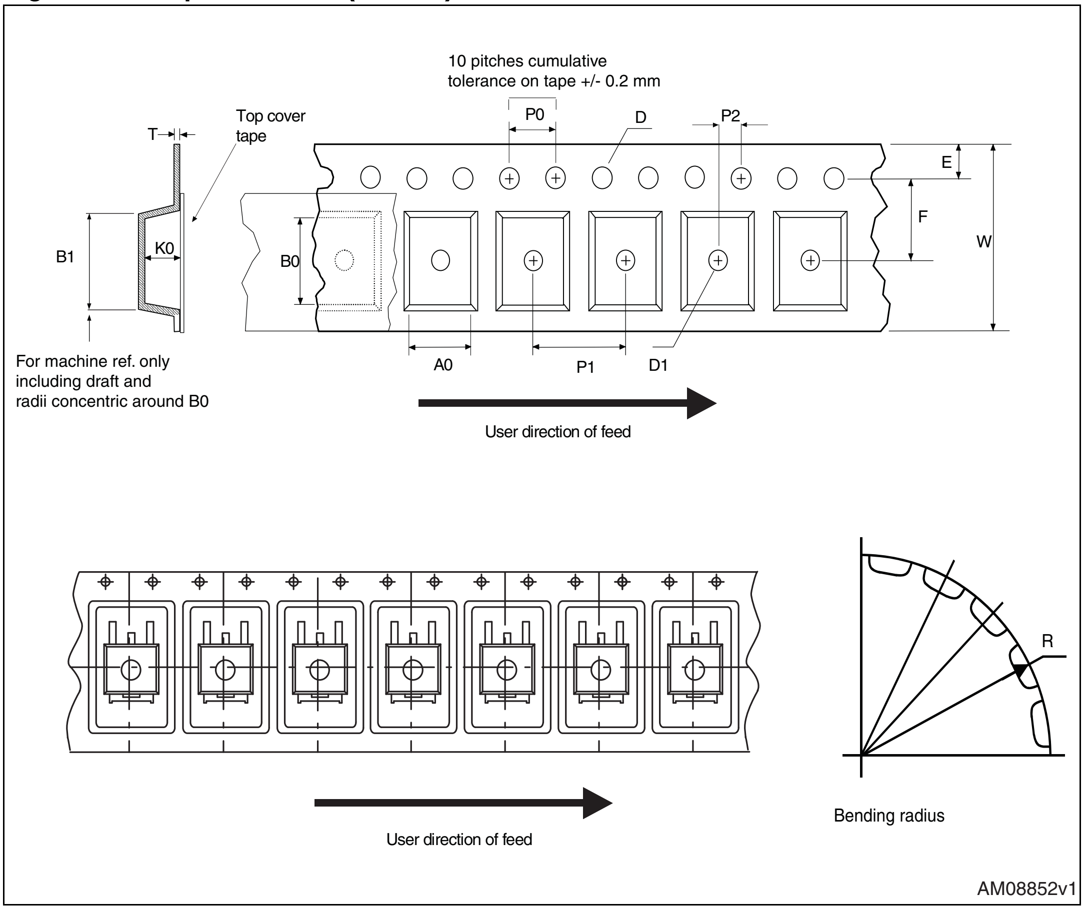
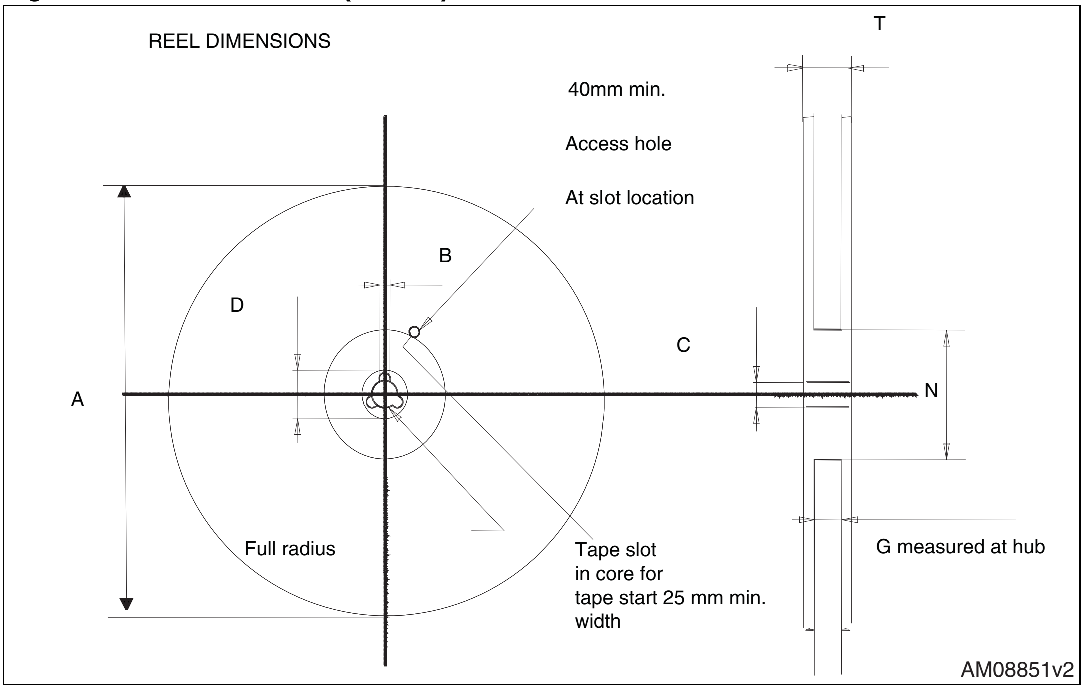


Figure 30. Reel for DPAK (TO-252)



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
09-Nov-2010	1	First release.
19-Feb-2013	2	Updated packages order in *Table 1: Device summary*. Updated *Table 4: Package mechanical data* and *Table 5: Packaging mechanical data*. Minor text changes on the cover page.