

**LOW COST 24 TO 36 MHZ 3.3 VOLT VCXO**

**ICS3727XP**

**Description**

The ICS3727XP combines the functions of a VCXO (Voltage Controlled Crystal Oscillator) and PLL (Phase-Locked Loop) frequency doubler onto a single chip. It is designed primarily for data and clock recovery applications within end products such as set-top box receivers.

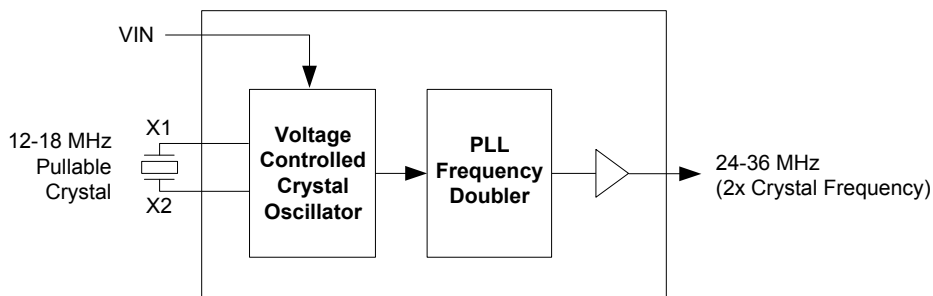
The ICS3727XP exhibits a moderate VCXO gain of 200 ppm/V typical, when used with a high quality external pullable quartz crystal.

The frequency of the on-chip VCXO is adjusted by an external control voltage input into pin VIN. Because VIN is a high impedance input, it can be driven directly from an PWM RC integrator circuit. Frequency output increases with VIN voltage input. The usable range of VIN is 0 to 3.3 V.

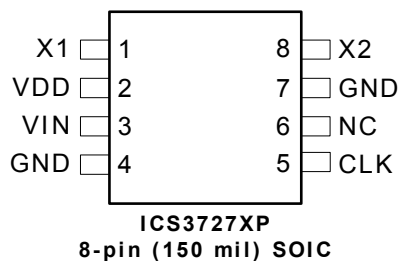
**Features**

- ICS3727XP offers 24 to 36 MHz output frequency range (output frequency = 2x crystal frequency) and improved power supply noise rejection
- Uses an inexpensive 12 to 18 MHz external crystal
- Ideal for DV CODEC applications using 27 MHz external pullable crystal with extended pull range to generate locked 27 MHz clock transport video clock
- On-chip VCXO with guaranteed pull range of  $\pm 200$  ppm minimum
- VCXO input tuning voltage 0 to 3.3 V
- Packaged in 8-pin SOIC (150 mil wide)

**Block Diagram**



## Pin Assignment



## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Crystal connection — Connect to the external pullable crystal.
2	VDD	Power	Connect to +3.3 V (0.01uf decoupling capacitor recommended).
3	VIN	Input	Voltage input to VCXO — 0 to 3.3 V analog input which controls the oscillation frequency of the VCXO.
4	GND	Power	Connect to ground.
5	CLK	Output	Clock output.
6	NC	—	No internal connection (may connect to ground or VDD).
7	GND	Power	Connect to ground.
8	X2	Input	Crystal connection — Connect to the external pullable crystal.

## External Component Selection

The ICS3727XP requires a minimum number of external components for proper operation.

### Decoupling Capacitor

A decoupling capacitor of 0.01 $\mu$ F must be connected between VDD (pin 2) and GND (pin 4), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

When the PCB trace between the clock output (CLK, pin 5) and the load is over 1 inch, series termination should be used. To series terminate a 50 $\Omega$  trace (a commonly used trace impedance) place a 33 $\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 $\Omega$ .

### Quartz Crystal

The ICS3727XP VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The ICS3727XP incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the ICS3727XP is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

### Recommended Crystal Parameters:

Initial Accuracy at 25° C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
Load Capacitance	14 pf
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	250 Max
Equivalent Series Resistance	35 $\Omega$ Max

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS3727XP. There should be no via's between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

### Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the ICS3727XP to 3.3 V. Connect pin 3 of the ICS3727XP to the second power supply. Adjust the voltage on pin 3 to 0V. Measure and record the frequency of the CLK output.
2. Adjust the voltage on pin 3 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$\text{Error} = 10^6 \times \left[ \frac{(f_{3.0V} - f_{\text{target}}) + (f_{0V} - f_{\text{target}})}{f_{\text{target}}} \right] - \text{error}_{\text{xtal}}$$

Where:

$f_{\text{target}}$  = nominal crystal frequency

$\text{error}_{\text{xtal}}$  = actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than  $\pm 25$  ppm, no adjustment is needed. If the centering error is more than 25ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact IDT for details.) If the centering error is more than 25 ppm positive, add identical fixed centering capacitors from each crystal pin to ground.

The value for each of these caps (in pF) is given by:  
 $\text{External Capacitor} = 2 \times (\text{centering error}) / (\text{trim sensitivity})$

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than  $\pm 25$  ppm).

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS3727XP. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

## DC Electrical Characteristics

VDD=3.3 V  $\pm$ 5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -12 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	Output = 27 MHz, no load		10		mA
Short Circuit Current	I <sub>OS</sub>			$\pm$ 50		mA
VIN, VCXO Control Voltage	V <sub>IA</sub>		0		3.3	V

## AC Electrical Characteristics

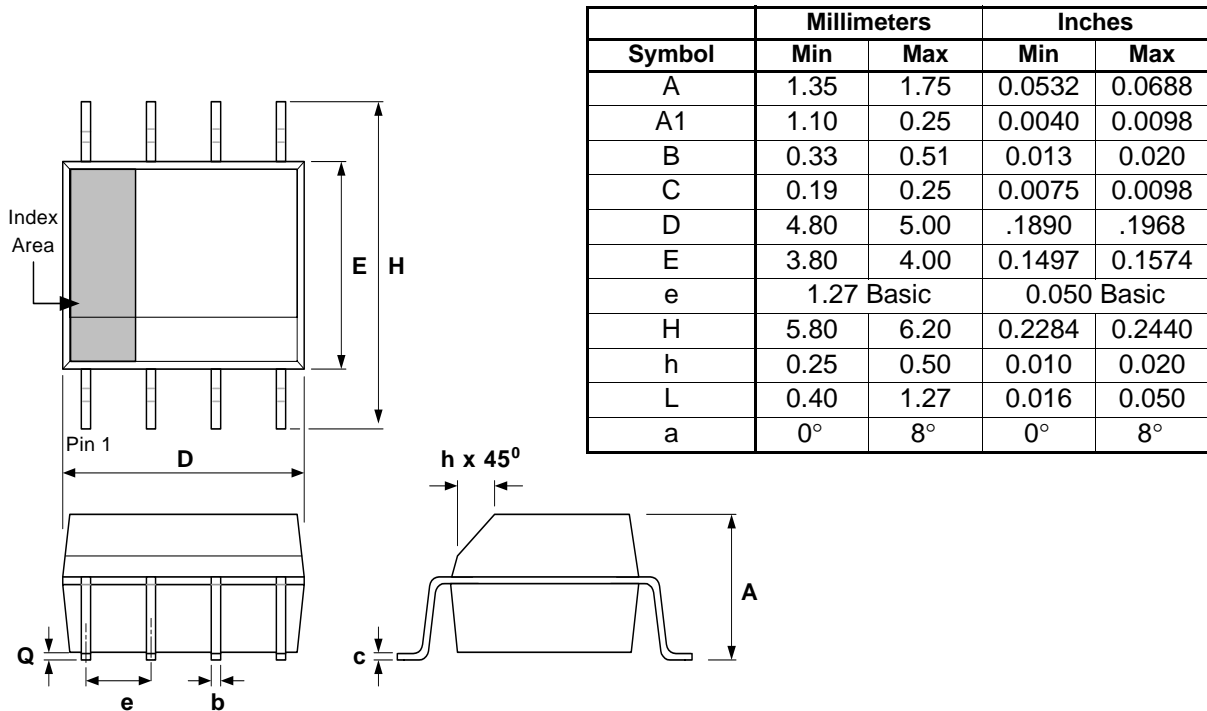
VDD = 3.3 V  $\pm$ 5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	F <sub>O</sub>	VCXO Crystal frequency = 1/2 Output	24		36	MHz
Crystal Pullability	F <sub>P</sub>	0V $\leq$ VIN $\leq$ 3.3 V, Note 1	$\pm$ 200			ppm
VCXO Gain		VIN = VDD/2 $\pm$ 1 V, Note 1		200		ppm/V
Output Rise Time	t <sub>OR</sub>	0.8 to 2.0 V, C <sub>L</sub> =15 pF			1.5	ns
Output Fall Time	t <sub>OF</sub>	2.0 to 0.8 V, C <sub>L</sub> =15 pF			1.5	ns
Output Clock Duty Cycle	t <sub>D</sub>	Measured at 1.4 V, C <sub>L</sub> =15 pF	40	50	60	%
Maximum Output Jitter, short term	t <sub>J</sub>	C <sub>L</sub> =15 pF		100		ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
3727XPM	3727XPM	Tubes	8-pin SOIC	0 to +70° C
3727XPMT	3727XPM	Tape and Reel	8-pin SOIC	0 to +70° C

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## Revision History

Rev.	Originator	Date	Description of Change
A	P.Griffith	10/20/04	New device/datasheet.

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