

NCP5661, NCV5661

Low Output Voltage, Ultra-Fast 1.0 A Low Dropout Linear Regulator with Enable

The NCP5661/NCV5661 is a high performance, low dropout linear regulator designed for high power applications that require up to 1.0 A current. It is offered in both fixed and adjustable output versions. With output voltages as low as 0.9 V and ultra-fast response times for load transients, the NCP5661/NCV5661 also provides additional features such as Enable and Error Flag (for the fixed output version), increasing the utility of these devices. A thermally robust, 5 pin DPAK or DFN 3x3.3 mm, combined with an architecture that offers low ground current (independent of load), provides for a superior high-current LDO solution.

Features

- Ultra-Fast Transient Response (Settling Time: 1–3 μ s)
- Low Noise Without Bypass Capacitor (26 μ V_{rms})
- Low Ground Current Independent of Load (3.0 mA Maximum)
- Fixed/Adjustable Output Voltage Versions
- Enable Function
- Error Flag (Fixed Output Version)
- Current Limit Protection
- Thermal Protection
- 0.9 V Reference Voltage for Ultra-Low Output Operation
- Power Supply Rejection Ratio > 65 dB
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These are Pb-Free Devices

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Applications

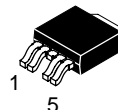
- Servers
- ASIC Power Supplies
- Post Regulation for Power Supplies
- Constant Current Source
- Networking Equipment
- Gaming and STB Modules



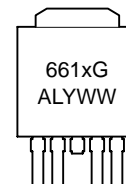
ON Semiconductor®

<http://onsemi.com>

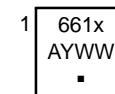
MARKING DIAGRAMS



DPAK-5
CENTER LEAD CROP
CASE 175AA



DFN6
MN SUFFIX
CASE 506AX



- x = A for Adjustable Version
- B for Fixed 1.2 V
- C for Fixed 3.3 V
- D for Fixed 1.5 V
- E for Fixed 1.8 V
- F for Fixed 2.5 V
- G for Fixed 2.8 V
- H for Fixed 3.0 V
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free
- = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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PIN FUNCTION DESCRIPTION

| Pin Adj/Fixed DFN6 | Pin Adj/Fixed DPAK-5 | Pin Name | Description |
|--------------------|----------------------|----------------------------|---|
| 1 | 1 | Enable | This pin allows for on/off control of the regulator. To disable the device, connect to Ground. If this function is not in use, connect to V_{in} . |
| 2,3 | 2 | V_{in} | Positive Power Supply Input Voltage |
| 4, EPAD | 3, TAB | Ground | Power Supply Ground |
| 5 | 4 | V_{out} | Regulated Output Voltage |
| 6 | 5 | Adj (Adjustable Version) | This pin is connected to the resistor divider network and programs the output voltage. |
| 6 | 5 | Error Flag (Fixed Version) | An Error Flag is triggered when the output voltage is out of regulation excluding transient signals that may occur. Requires a pullup resistor $\approx 100\text{ k}\Omega$. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|------------------------------------|-----------------------|-----------------------------|
| Input Voltage | V_{in} | 18 | V |
| Output Pin Voltage | V_{out} | -0.3 to V_{in} +0.3 | V |
| Adjust Pin Voltage | V_{adj} | -0.3 to V_{in} +0.3 | V |
| Enable Pin Voltage | V_{en} | -0.3 to V_{in} +0.3 | V |
| Error Flag Voltage | V_{ef} | -0.3 to V_{in} +0.3 | V |
| Error Flag Current | I_{ef} | 3.0 | mA |
| Thermal Characteristics, DPAK-5 (Note 1) Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case | $R_{\theta JA}$ $R_{\theta JC}$ | 100 8.0 | $^{\circ}\text{C}/\text{W}$ |
| Thermal Characteristics, DFN6 (Note 2) Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Lead (Note 3) | $R_{\theta JA}$ $R_{\theta JL}$ | 82 18 | $^{\circ}\text{C}/\text{W}$ |
| Operating Junction Temperature Range | T_J | -40 to +150 | $^{\circ}\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^{\circ}\text{C}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTE: This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) JESD 22-A114-B

Machine Model (MM) JESD 22-A115-A.

The maximum package power dissipation is:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The bipolar process employed for this IC is fully characterized and rated for reliable 18 V V_{CCmax} operation. To avoid damaging the part or degrading its reliability, power dissipation transients should be limited to under 20 W for DPAK.

For open-circuit to short-circuit transient,

$$P_{DTransient} = V_{CCmax} \cdot I_{SC}$$

1. 1 oz copper, 0.26 in² copper area (minimum pad)
2. 1 oz copper, 1 in² copper area
3. Lead 2

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ELECTRICAL CHARACTERISTICS

($V_{in} - V_{out} = 1.5$ V, for typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to 125°C , $C_{in} = C_{out} = 150$ μF unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------------|---------------------|---------------|---------------------|----------------------------|
| ADJUSTABLE OUTPUT VERSION | | | | | |
| Input Voltage | V_{in} | 2.0 | – | 9.0 | V |
| Output Noise Voltage (f = 10 Hz to 100 kHz) | V_n | – | 26 | – | μV_{rms} |
| Output Voltage Accuracy $T_J = 25^\circ\text{C}$ ($I_{out} = 10$ mA to 1.0 A) $T_J = -20$ to $+125^\circ\text{C}$ ($I_{out} = 10$ mA to 1.0 A) $T_J = -40$ to $+150^\circ\text{C}$ ($I_{out} = 10$ mA to 1.0 A) | V_{out} | -1% -1.5% -2% | – 0.9 – | +1% +1.5% +2% | V |
| Adjustable Pin Input Current | I_{adj} | – | 40 | – | nA |
| Line Regulation ($I_{out} = 10$ mA, $V_{out} + 1.5$ V < V_{in} < 7.0 V) | REG_{line} | – | 0.03 | – | % |
| Load Regulation (10 mA < I_{out} < 1.0 A) | REG_{load} | – | 0.03 | – | % |
| Dropout Voltage ($I_{out} = 1.0$ A) | V_{DO} | – | 1.0 | 1.3 | V |
| Peak Output Current Limit | I_{out} | 1.0 | – | – | A |
| Internal Current Limitation | I_{lim} | – | 1.5 | – | A |
| Ripple Rejection (120 Hz) | RR | – | 70 | – | dB |
| Ripple Rejection (1.0 kHz) | | – | 65 | – | |
| Thermal Shutdown (Guaranteed by Design) | T_{SHD} | – | 160 | – | $^\circ\text{C}$ |
| Ground Current $I_{out} = 1.0$ A Disabled State | I_q I_{qds} | – – | 1.3 10 | 3.0 300 | mA μA |
| Enable Input Threshold Voltage Voltage Increasing, On State, Logic High Voltage Decreasing, Off State, Logic Low | V_{en} | 1.3 – | – – | – 0.3 | V |
| Enable Input Current Enable Pin Voltage = $0.3 V_{\text{max}}$ Enable Pin Voltage = $1.3 V_{\text{min}}$ | I_{en} | – – | 0.5 0.5 | – – | μA |

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ELECTRICAL CHARACTERISTICS

($V_{in} - V_{out} = 1.5$ V, for typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to 125°C , $C_{in} = C_{out} = 150$ μF unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------------|--|--|--|----------------------------|
| FIXED OUTPUT VOLTAGE | | | | | |
| Input Voltage | V_{in} | 2.0 | – | 9.0 | V |
| Output Noise Voltage ($V_{out} = 0.9$ V) | V_n | – | 26 | – | μV_{rms} |
| Output Voltage Accuracy (Note 1) $T_J = 25^\circ\text{C}$ ($I_{out} = 10$ mA to 1.0 A) $T_J = -20$ to $+125^\circ\text{C}$ ($I_{out} = 10$ mA to 1.0 A) $T_J = -40$ to $+150^\circ\text{C}$ ($I_{out} = 10$ mA to 1.0 A) | V_{out} | -1% -1.5% -2% | – V_{out} – | +1% +1.5% +2% | V |
| Line Regulation ($I_{out} = 10$ mA, $V_{out} + 1.5$ V < V_{in} < 7.0 V) | REG _{line} | – | 0.03 | – | % |
| Load Regulation (10 mA < I_{out} < 1.0 A) | REG _{load} | – | 0.2 | – | % |
| Dropout Voltage ($I_{out} = 1.0$ A) | V_{DO} | – | 1.0 | 1.3 | V |
| Peak Output Current Limit | I_{out} | 1.0 | – | – | A |
| Internal Current Limitation | I_{lim} | – | 1.5 | – | A |
| Ripple Rejection (120 Hz) | RR | – | 70 | – | dB |
| Ripple Rejection (1.0 kHz) | | – | 65 | – | |
| Thermal Shutdown (Guaranteed by Design) | T_{SHD} | – | 160 | – | $^\circ\text{C}$ |
| Ground Current $I_{out} = 1.0$ A Disabled State | I_q I_{qds} | – – | 1.3 30 | 3.0 300 | mA μA |
| Enable Input Threshold Voltage Voltage Increasing, On State, Logic High Voltage Decreasing, Off State, Logic Low | V_{en} | 1.3 – | – – | – 0.3 | V |
| Enable Input Current Enable Pin Voltage = $0.3 V_{max}$ Enable Pin Voltage = $1.3 V_{min}$ | I_{en} | – – | 0.5 0.5 | – – | μA |
| Error Flag (Fixed Output) 1.2 V Output 1.5 V Output 1.8 V Output 2.5 V Output 2.8 V Output 3.0 V Output 3.3 V Output | V_{eflt} | 88 88 88 88 88 88 90 | 92 92 92 92 92 92 94 | 97 97 97 97 97 97 97 | % of V_{out} |
| Error Flag Output Low Voltage Saturation ($I_{ef} = 1.0$ mA) | V_{efdo} | – | 200 | – | mV |
| Error Flag Leakage | I_{efleak} | – | 1.0 | – | μA |
| Error Flag Blanking Time (Note 2) | T_{ef} | – | 50 | – | μs |

1. Fixed output voltages available at 0.9 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V per request.
2. Can be disabled per customer request.

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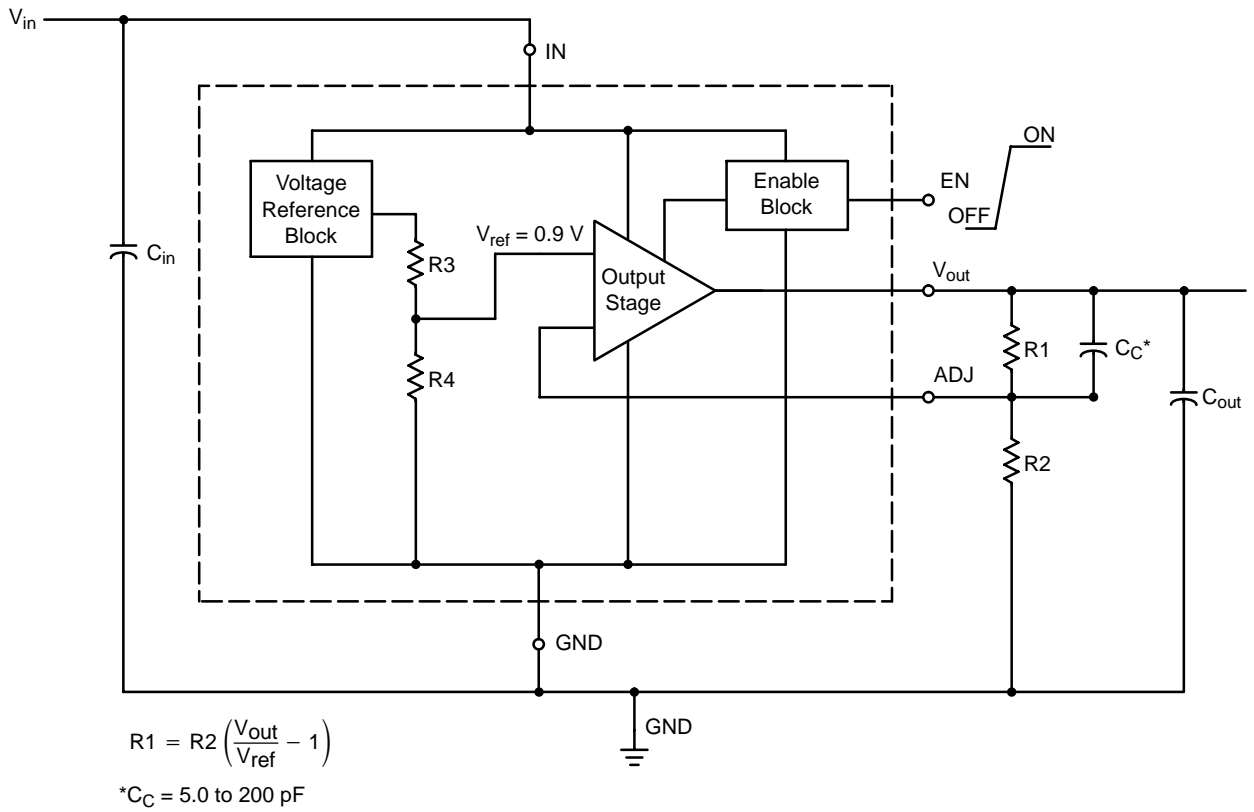


Figure 1. Typical Schematic, Adjustable Output Version

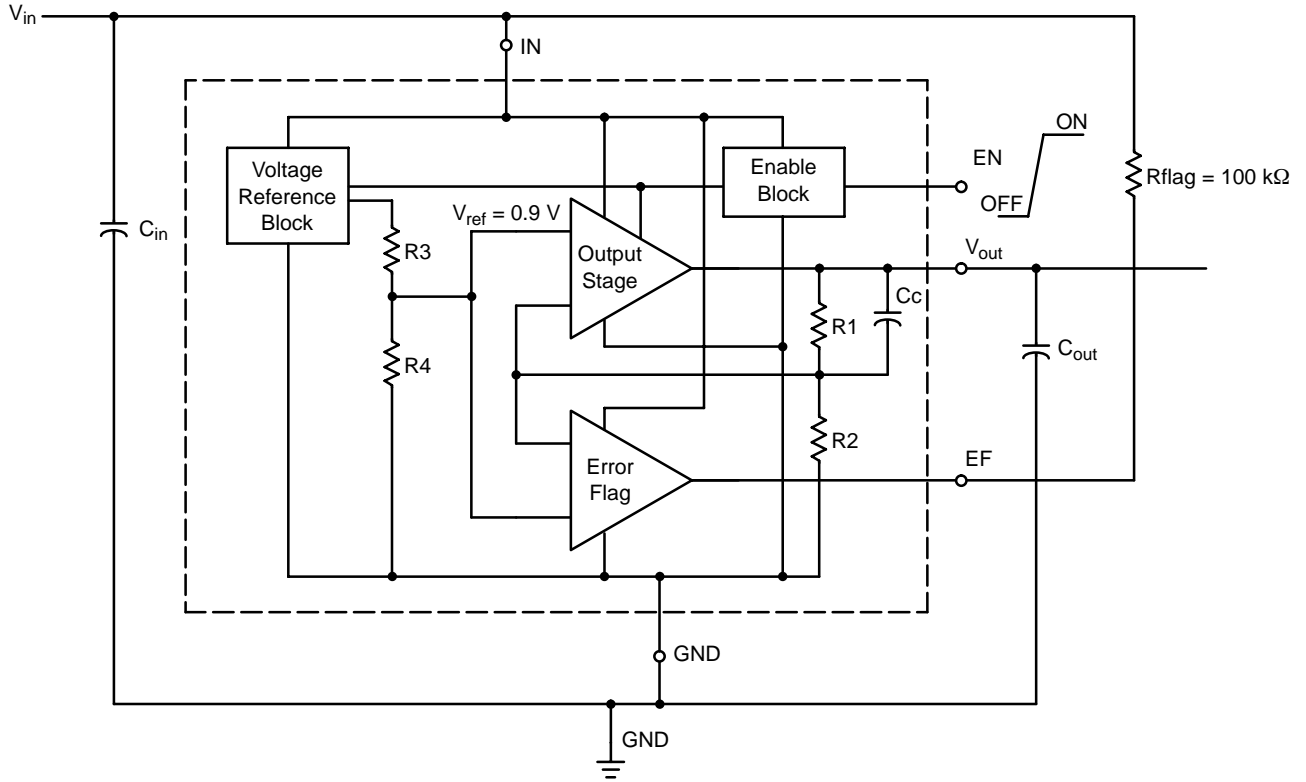


Figure 2. Typical Schematic, Fixed Output Version

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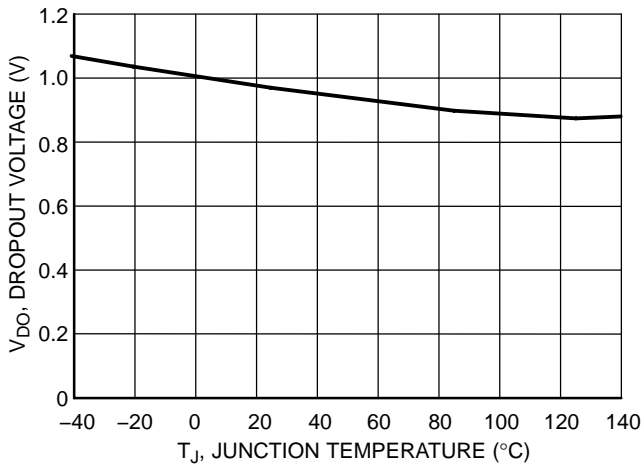


Figure 3. Dropout Voltage vs. Temperature

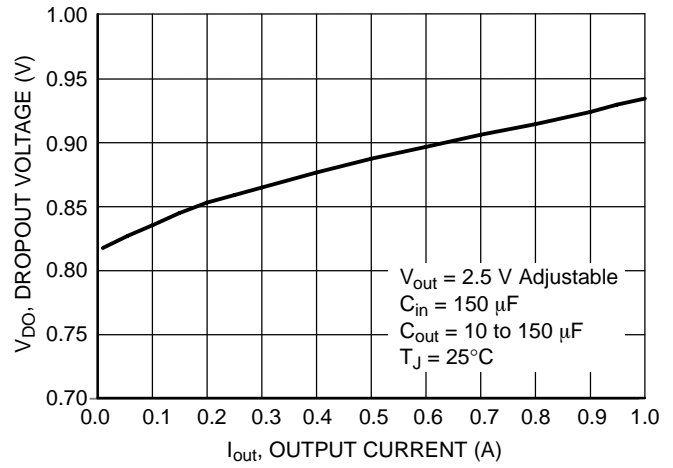


Figure 4. Dropout Voltage vs. Output Current

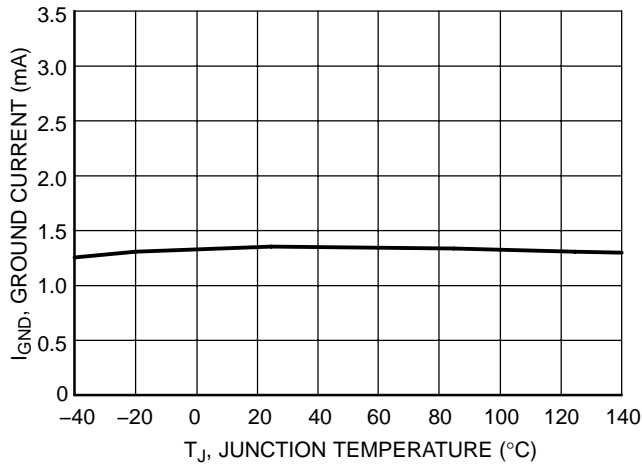


Figure 5. Ground Current vs. Temperature

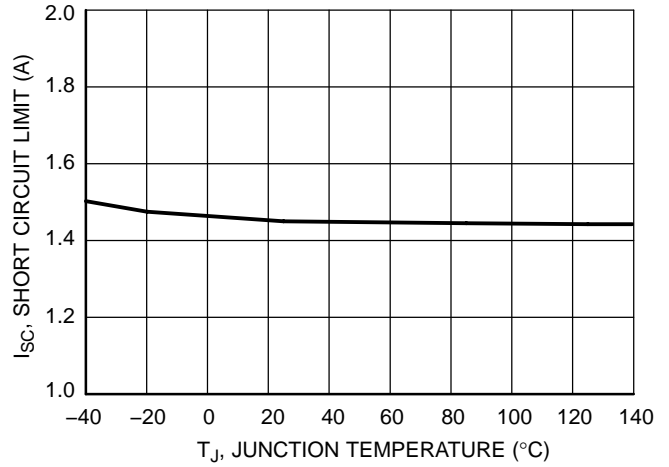


Figure 6. Short Circuit Current Limit vs. Temperature

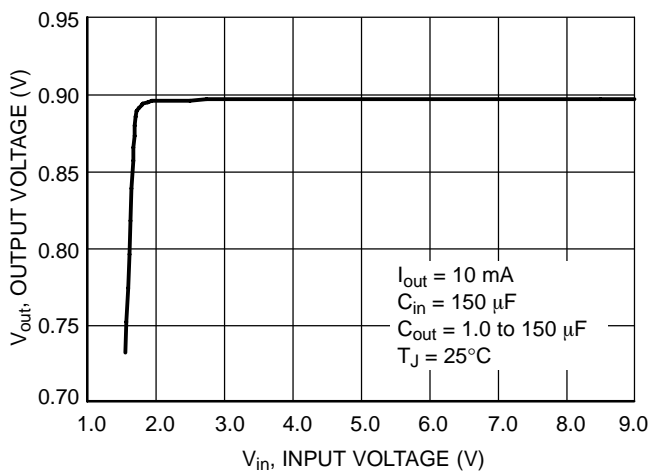


Figure 7. Output Voltage vs. Input Voltage

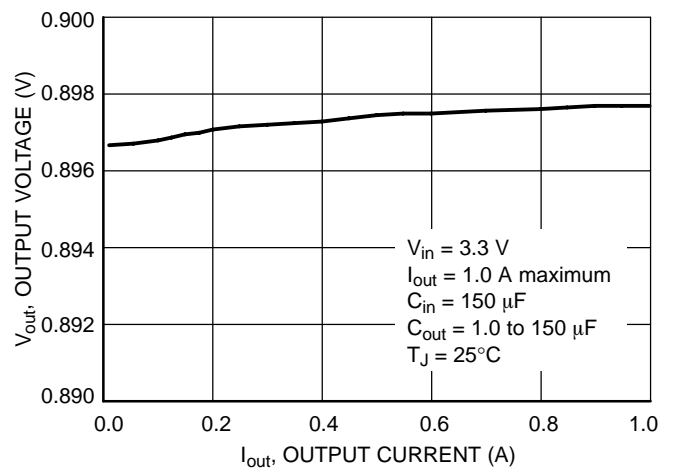


Figure 8. Output Voltage vs. Output Load Current

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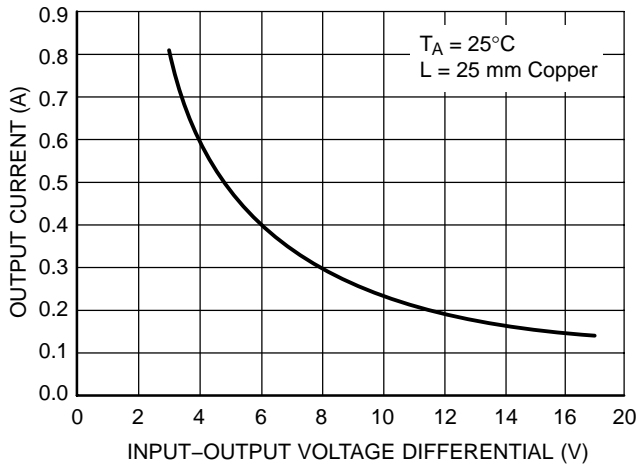


Figure 9. Output Current vs. Input-Output Voltage Differential

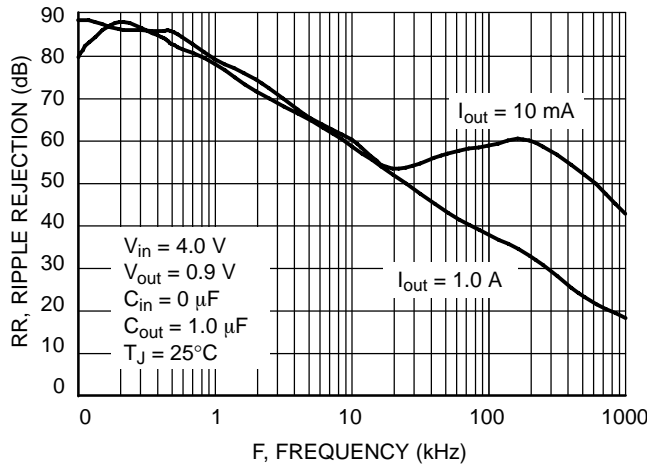


Figure 10. Ripple Rejection vs. Frequency

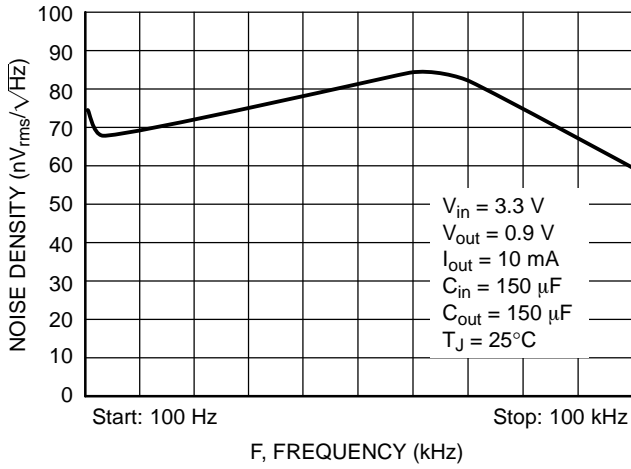


Figure 11. Noise Density vs. Frequency

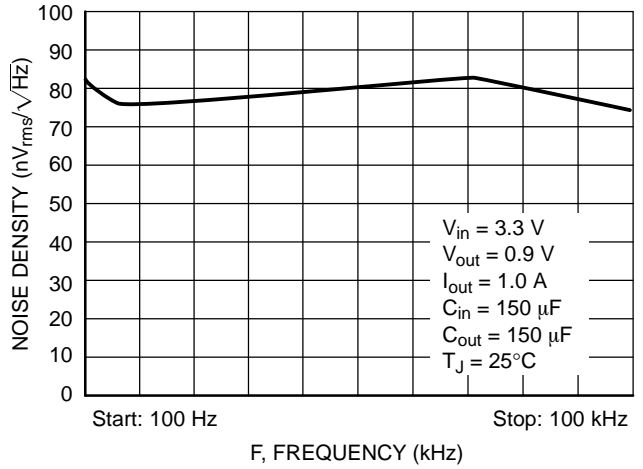


Figure 12. Noise Density vs. Frequency

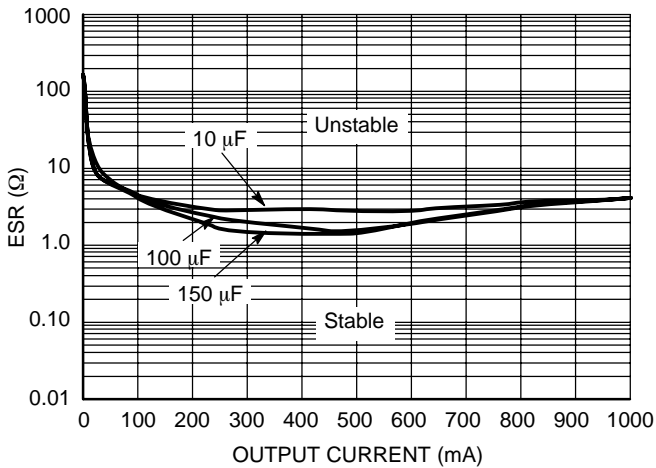


Figure 13. 1.2 Volt Output Stability with Output Capacitor ESR

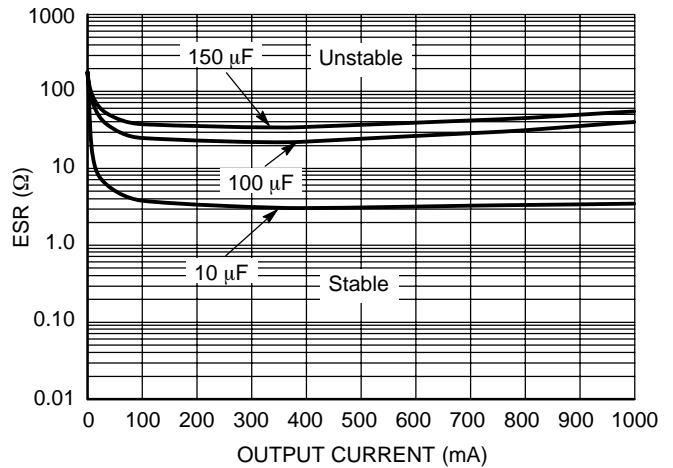


Figure 14. 3.3 Volt Output Stability with Output Capacitor ESR

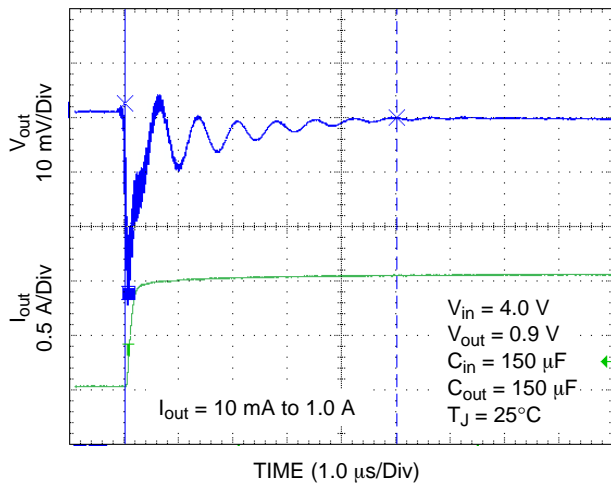


Figure 15. Load Transient Response

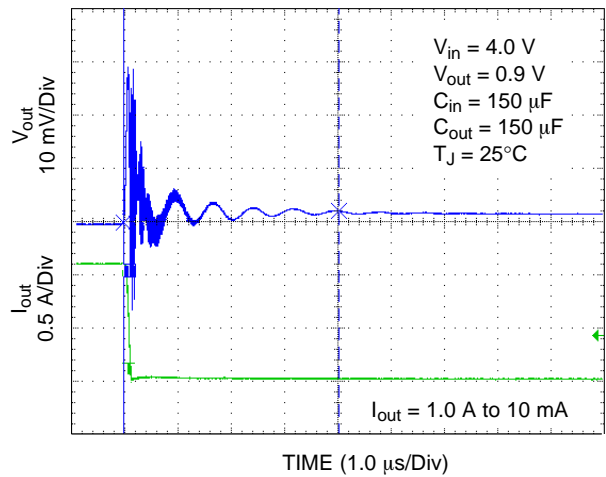


Figure 16. Load Transient Response

APPLICATION INFORMATION

The NCP5661 is a high performance low dropout 1.0 A linear regulator suitable for high power applications, featuring an ultra-fast response time and low noise without a bypass capacitor. It is offered in both fixed and adjustable output versions with voltages as low as 0.9 V. Additional features, such as Enable and Error Flag (fixed output version) increase the utility of the NCP5661. It is thermally robust and includes the safety features necessary during a fault condition, which provide for an attractive high current LDO solution for server, ASIC power supplies, networking equipment applications, and many others.

Input Capacitor

The recommended input capacitor value is a 150 μF OSCON with an Equivalent Series Resistance (ESR) of 50 mΩ. It is especially required if the power source is located more than a few inches from the NCP5661. This capacitor will reduce device sensitivity and enhance the output transient response time. The PCB layout is very important and in order to obtain the optimal solution, the Vin and GND traces should be sufficiently wide to minimize noise and unstable operation.

Output Capacitor

Proper output capacitor selection is required to maintain stability. The NCP5661 is guaranteed to be stable at an output capacitance of, $C_{out} > 10 \mu\text{F}$ with an ESR $< 300 \text{ m}\Omega$ over the output current range of 10 mA to 1.0 A. For PCB layout considerations, place the recommended ceramic capacitor close to the output pin and keep the leads short. This should help ensure ultra-fast transient response times.

Adjustable Output Operation

The application circuit for the adjustable output version is shown in Figure 1. The reference voltage is 0.9 V and the adjustable pin current is typically 40 nA. A resistor divider network, R1 and R2, is calculated using the following formula:

$$R1 = R2 \left(\frac{V_{out}}{V_{ref}} - 1 \right)$$

Current Limit Operation

As the peak output current increases beyond its limitation, the device is internally clamped to 1.5 A, thus causing the output voltage to decrease and go out of regulation. This allows the device never to exceed the maximum power dissipation.

Error Flag Operation

The Error Flag pin on the NCP5661 will produce a logic Low when it drops below the nominal output voltage. Refer to the electrical characteristics for the threshold values at which point the Error Flag goes Low. When the NCP5661 is above the nominal output voltage, the Error Flag will remain at logic High.

The external pullup resistor needs to be connected between Vin (Pin 1) and the Error Flag pin (Pin 5). A resistor of approximately 100 kΩ is recommended to minimize the current consumption. No pullup resistor is required if the Error Flag output is not being used.

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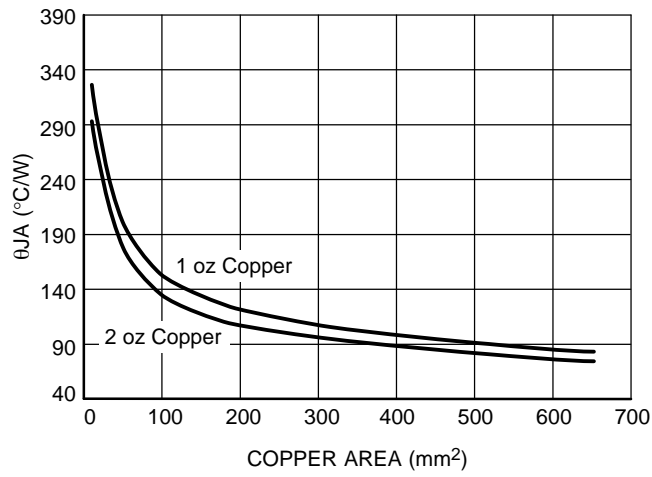


Figure 17. DFN6 Thermal Resistance vs. Copper Area

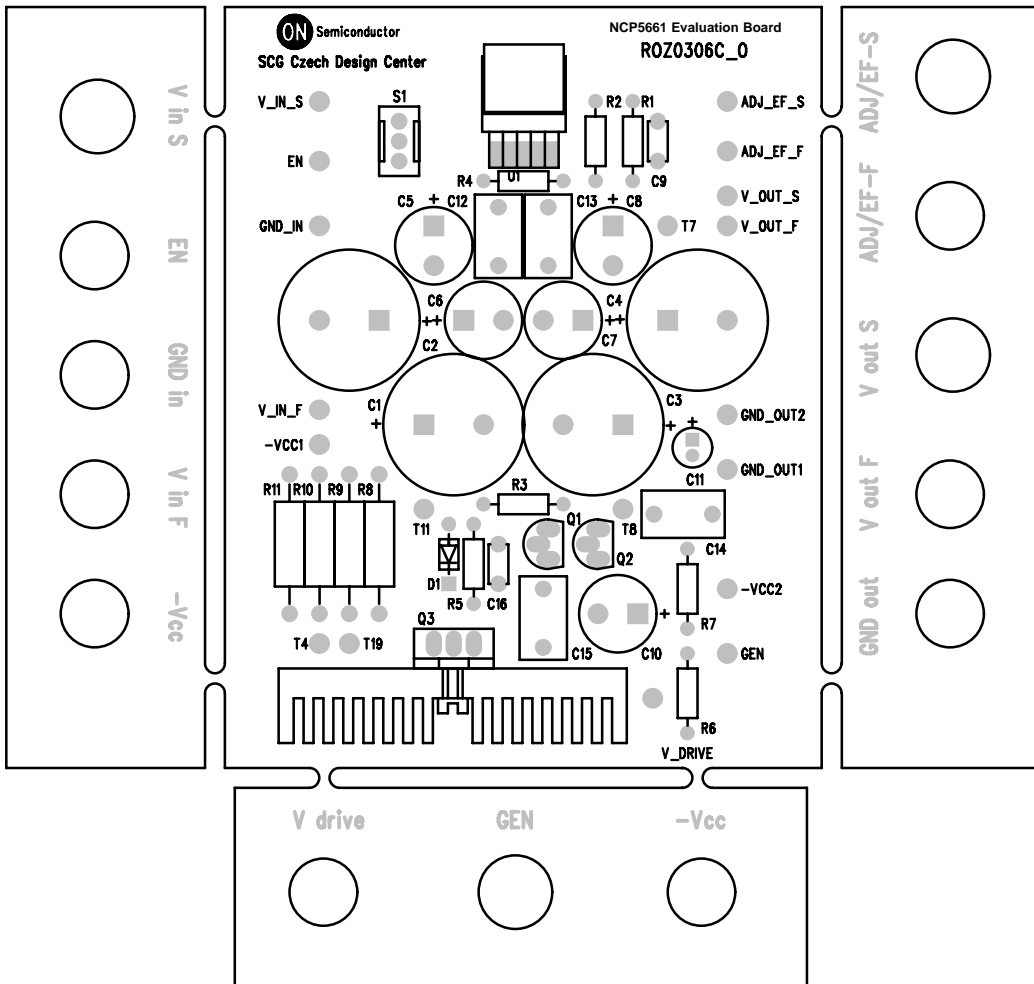


Figure 18. Test Board used for Evaluation

NCP5661, NCV5661

ORDERING INFORMATION

| Device | Nominal Output Voltage | Package | Shipping† |
|-------------------------|---------------------------|------------------|------------------|
| NCP5661DTADJRKG | Adj (Pb-Free) | DPAK | 2500/Tape & Reel |
| NCP5661DT12RKG (Note 3) | Fixed, 1.2 V (Pb-Free) | | |
| NCP5661DT33RKG (Note 3) | Fixed, 3.3 V (Pb-Free) | | |
| NCV5661DTADJRKG | Adj (Pb-Free) | | |
| NCV5661DT12RKG (Note 3) | Fixed, 1.2 V (Pb-Free) | | |
| NCV5661DT33RKG (Note 3) | Fixed, 3.3 V (Pb-Free) | | |
| NCP5661MNADJT2G | Adj (Pb-Free) | DFN6 3x3.3 mm | 3000/Tape & Reel |
| NCP5661MN12T2G | Fixed, 1.2 V (Pb-Free) | | |
| NCP5661MN15T2G | Fixed, 1.5 V (Pb-Free) | | |
| NCP5661MN18T2G | Fixed, 1.8 V (Pb-Free) | | |
| NCP5661MN25T2G | Fixed, 2.5 V (Pb-Free) | | |
| NCP5661MN28T2G | Fixed, 2.8 V (Pb-Free) | | |
| NCP5661MN30T2G | Fixed, 3.0 V (Pb-Free) | | |
| NCP5661MN33T2G | Fixed, 3.3 V (Pb-Free) | | |

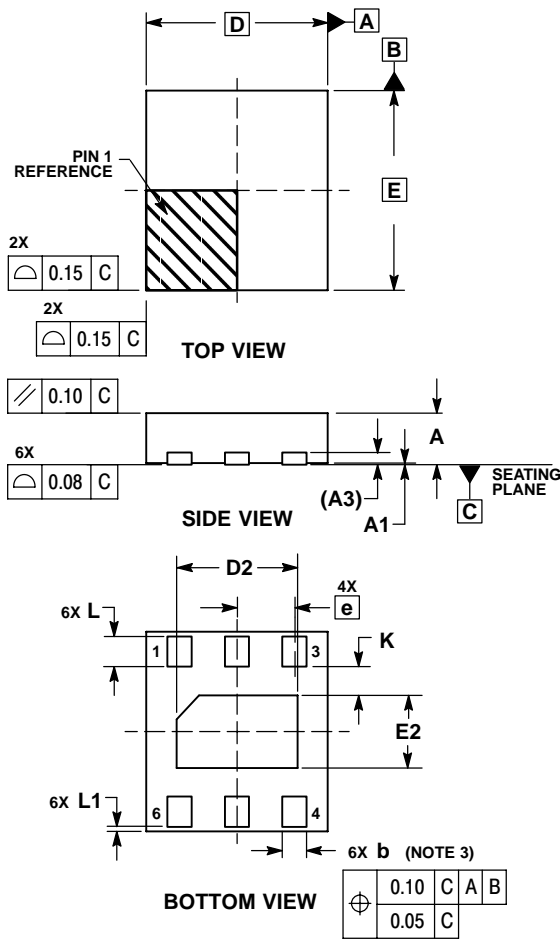
3. Fixed output voltages available at 0.9 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V per request.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

DFN6 3x3.3 MM, 0.95 PITCH
CASE 506AX-01
ISSUE O

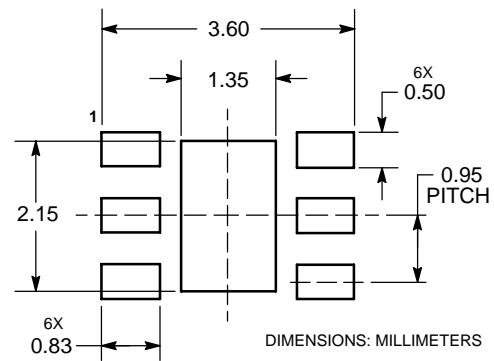


NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | | |
|-------------|----------|-----|------|
| DIM | MIN | NOM | MAX |
| A | 0.80 | --- | 0.90 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.30 | --- | 0.40 |
| D | 3.00 BSC | | |
| D2 | 1.90 | --- | 2.10 |
| E | 3.30 BSC | | |
| E2 | 1.10 | --- | 1.30 |
| e | 0.95 BSC | | |
| K | 0.20 | --- | --- |
| L | 0.40 | --- | 0.60 |
| L1 | 0.00 | --- | 0.15 |

SOLDERING FOOTPRINT*

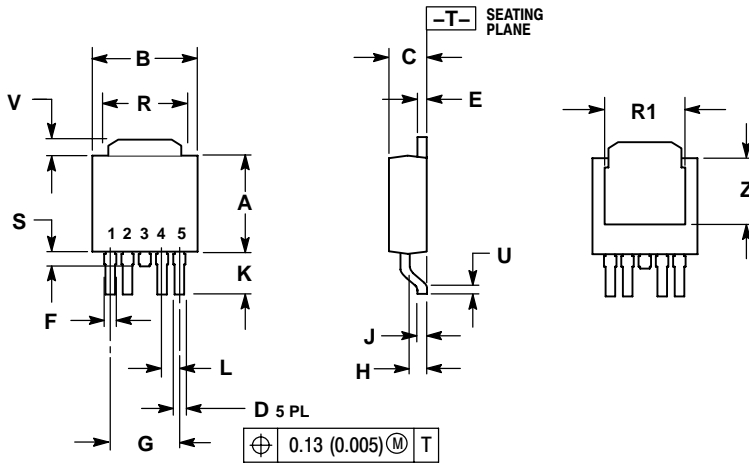


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

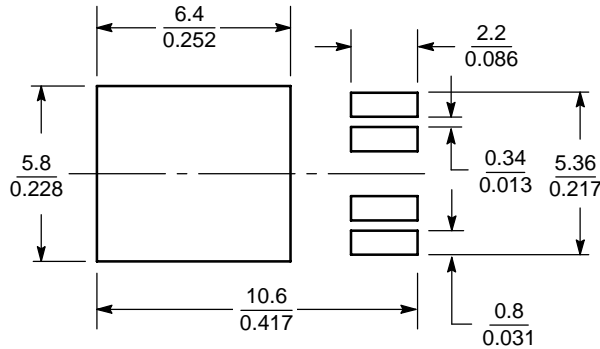
DPAK-5 CENTER LEAD CROP CASE 175AA-01 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.020 | 0.028 | 0.51 | 0.71 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.024 | 0.032 | 0.61 | 0.81 |
| G | 0.180 BSC | | 4.56 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.045 BSC | | 1.14 BSC | |
| R | 0.170 | 0.190 | 4.32 | 4.83 |
| R1 | 0.185 | 0.210 | 4.70 | 5.33 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | --- | 0.51 | --- |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | 0.170 | 3.93 | 4.32 |

SOLDERING FOOTPRINT*



SCALE 4:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NCP5661/NCV5661), may be covered by one or more of the following U.S. patents: 5,920,184; 5,834,926. There may be other patents pending.

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