

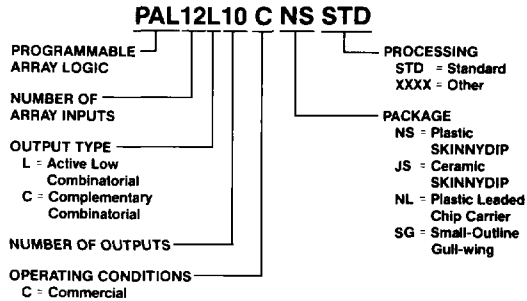
Combinatorial PAL12L10 Series

12L10, 14L8, 16L6 18L4, 20L2, 20C1

Features/Benefits

- Combinatorial architecture
- Security fuse

Ordering Information



PAL12L10 Series

DEVICE	INPUTS	OUTPUTS	POLARITY	t _{PD} (ns)	I _{CC} (mA)
PAL12L10	12	10	LOW	40	100
PAL14L8	14	8	LOW	40	100
PAL16L6	16	6	LOW	40	100
PAL18L4	18	4	LOW	40	100
PAL20L2	20	2	LOW	40	100
PAL20C1	20	2	BOTH	40	100

Description

The PAL12L10 Series is made up of six combinatorial 24-pin PAL devices. They implement simple combinatorial logic, with no feedback.

Performance

The standard series has a propagation delay (t_{PD}) of 40 nanoseconds (ns). Standard supply current is 100 milliamps (mA).

Packages

The commercial PAL12L10 Series is available in the plastic SKINNYDIP (NS), ceramic SKINNYDIP (JS), plastic leaded chip carrier (NL), and small outline (SG) packages.

Package Drawings

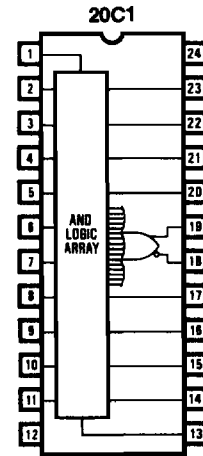
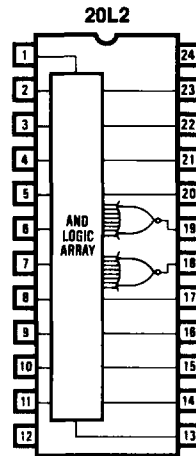
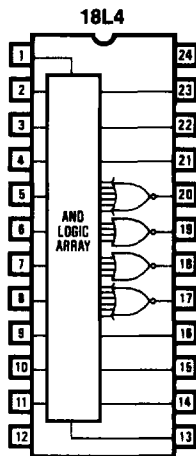
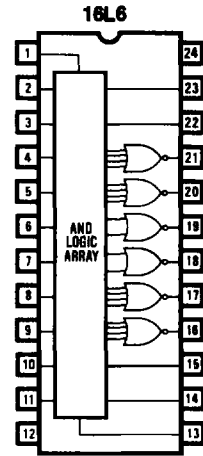
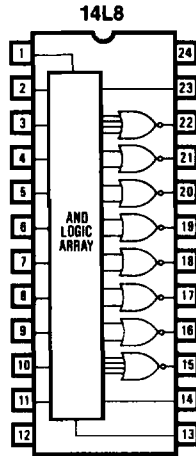
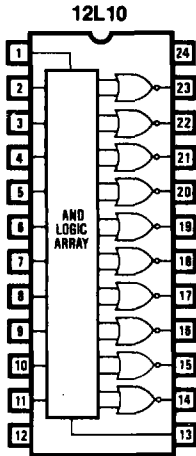
(refer to PAL Device Package Outlines, page 3-179)

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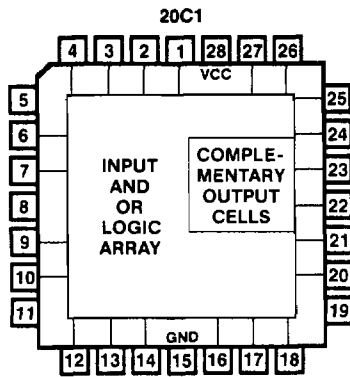
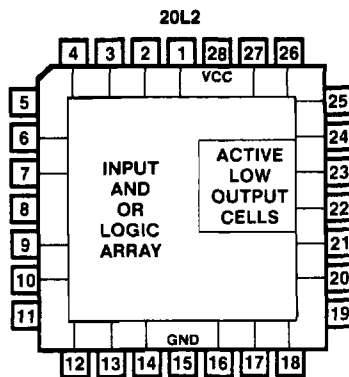
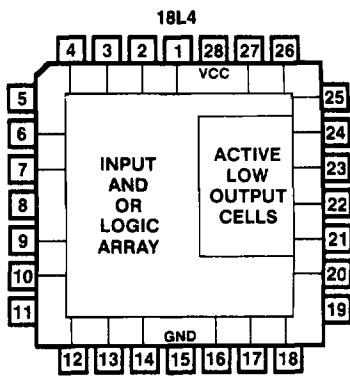
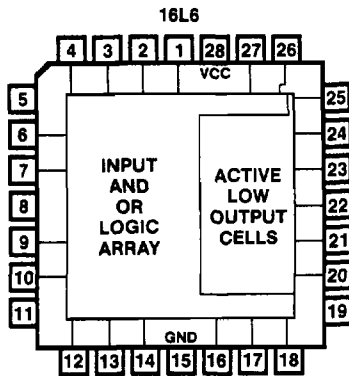
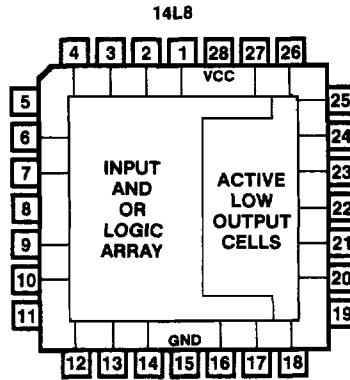
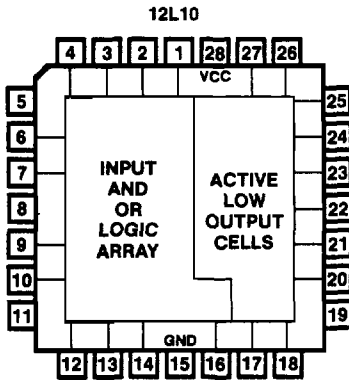
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DIP/SO Pinouts



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PLCC Pinouts



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Combinatorial PAL12L10 Series

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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7.0 V	-0.5 V to 12.0 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			UNIT
		MIN	TYP	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free-air temperature	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN TYP MAX			UNIT
V_{IL}^1	Low-level input voltage				0.8		V
V_{IH}^1	High-level input voltage			2			V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$	-0.8	-1.5		V
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$	-0.02	-0.25		mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4 \text{ V}$		25		μA
I_I	Maximum input current	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$		100		μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 8 \text{ mA}$	0.3	0.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -3.2 \text{ mA}$	2.4	2.8		V
I_{OS}^2	Output short-circuit current	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$	-30	-70	-130	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$		60	100		mA

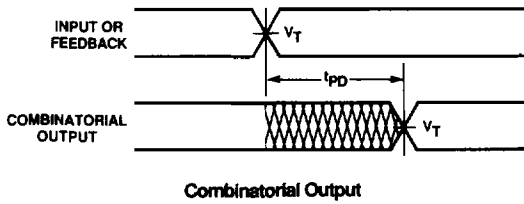
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN TYP MAX			UNIT
t_{PD}	Input or feedback to output	$R1 = 560 \Omega, R2 = 1.1 \text{ K}\Omega$	25	40		ns

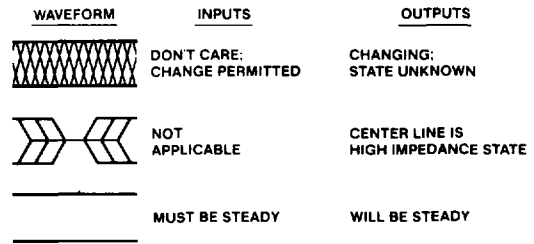
- 1 These are absolute values with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- 2 No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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Switching Waveforms



Key to Timing Diagrams



- Notes:
1. $V_T = 1.5$ V.
 2. Input pulse amplitude 0 V to 3.0 V.
 3. Input rise and fall times 2-5 ns typical.

Switching Test Load

(refer to page 5-164)

Programmers/Development Systems

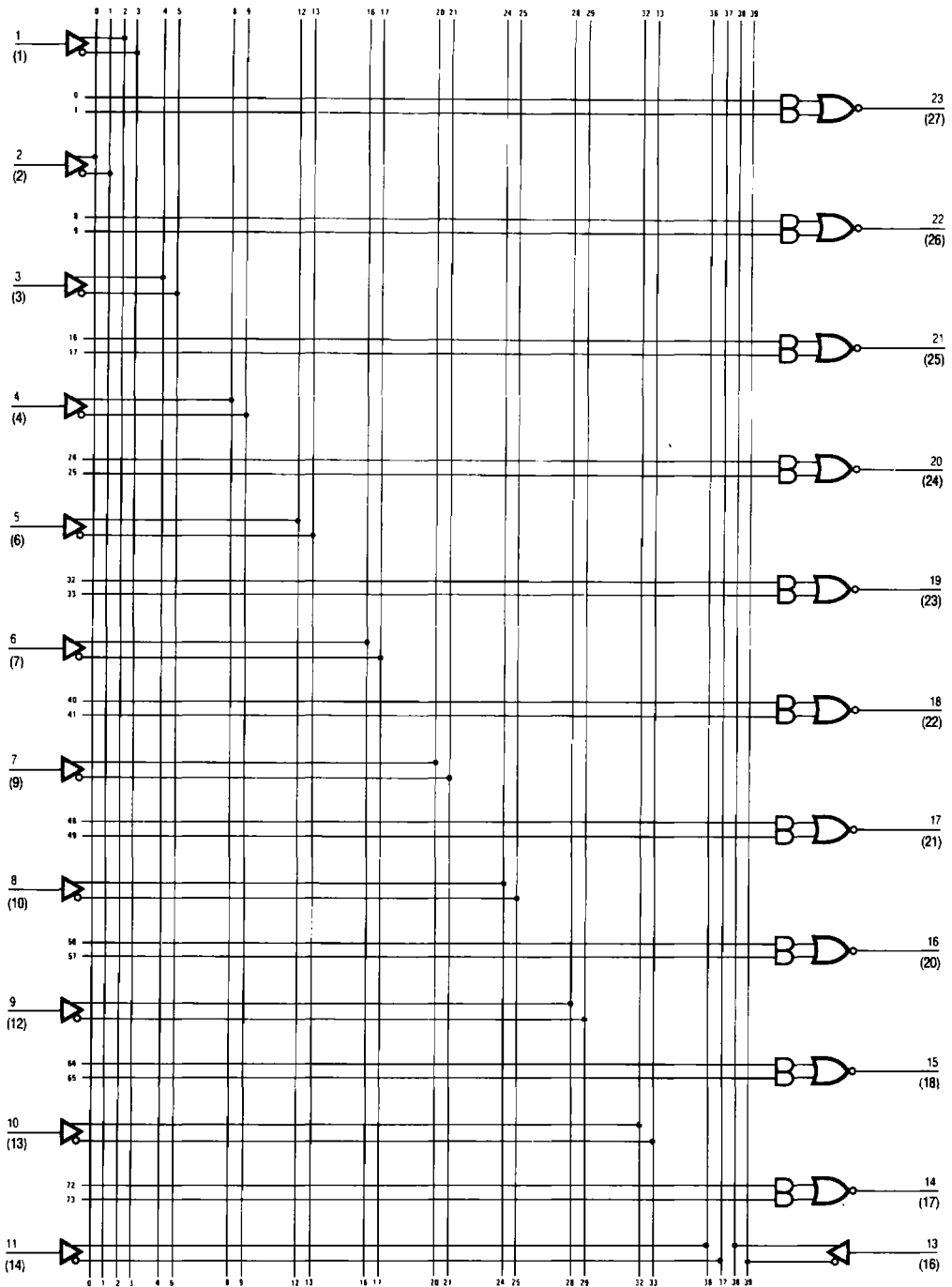
(refer to Programmer Reference Guide, page 3-81)

Schematic of Inputs and Outputs

(refer to page 5-164)

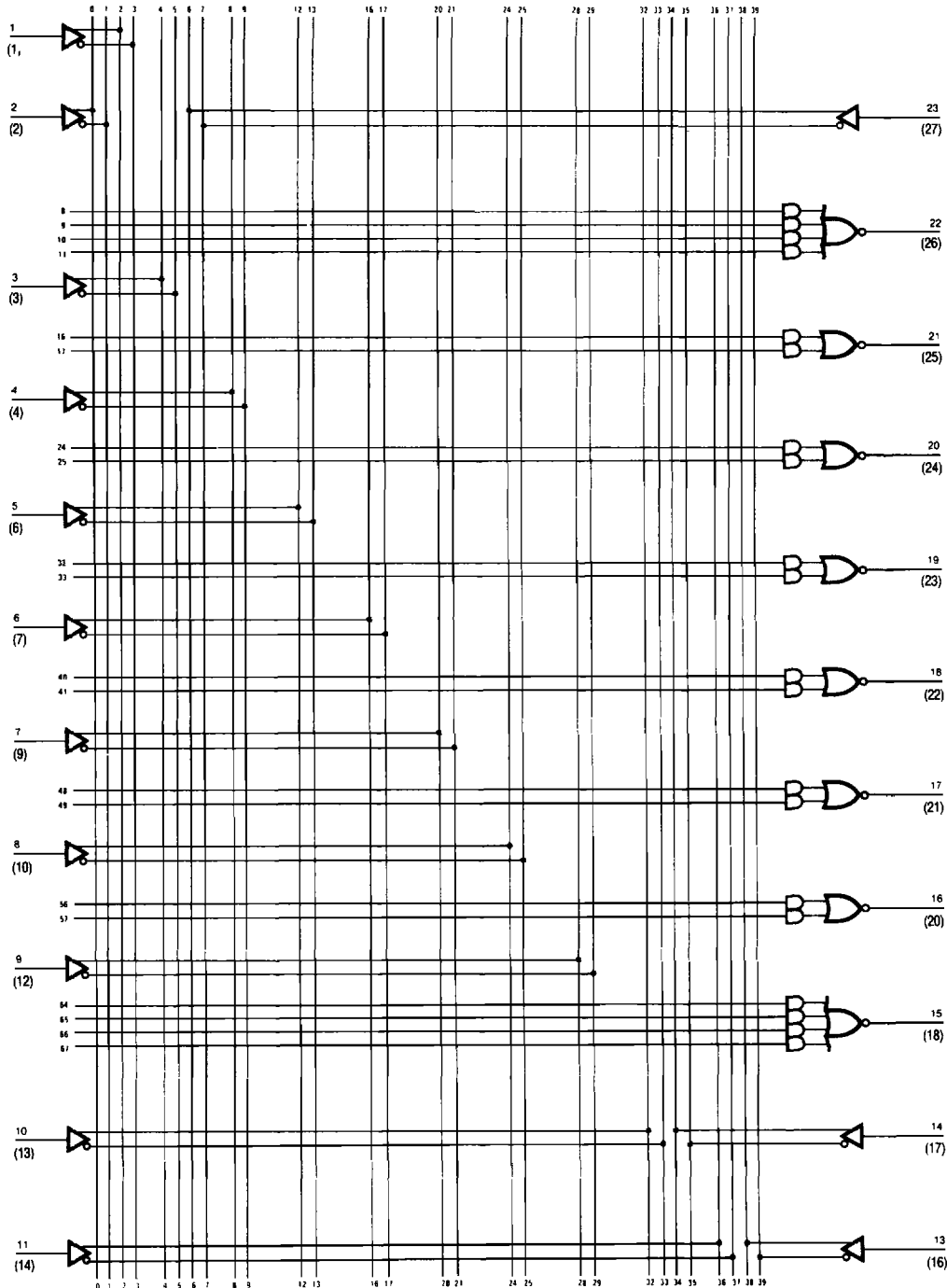
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Logic Diagram DIP (PLCC) Pinouts 12L10



Combinatorial PAL12L10 Series
12L10, 14L8, 16L6, 18L4, 20L2, 20C1

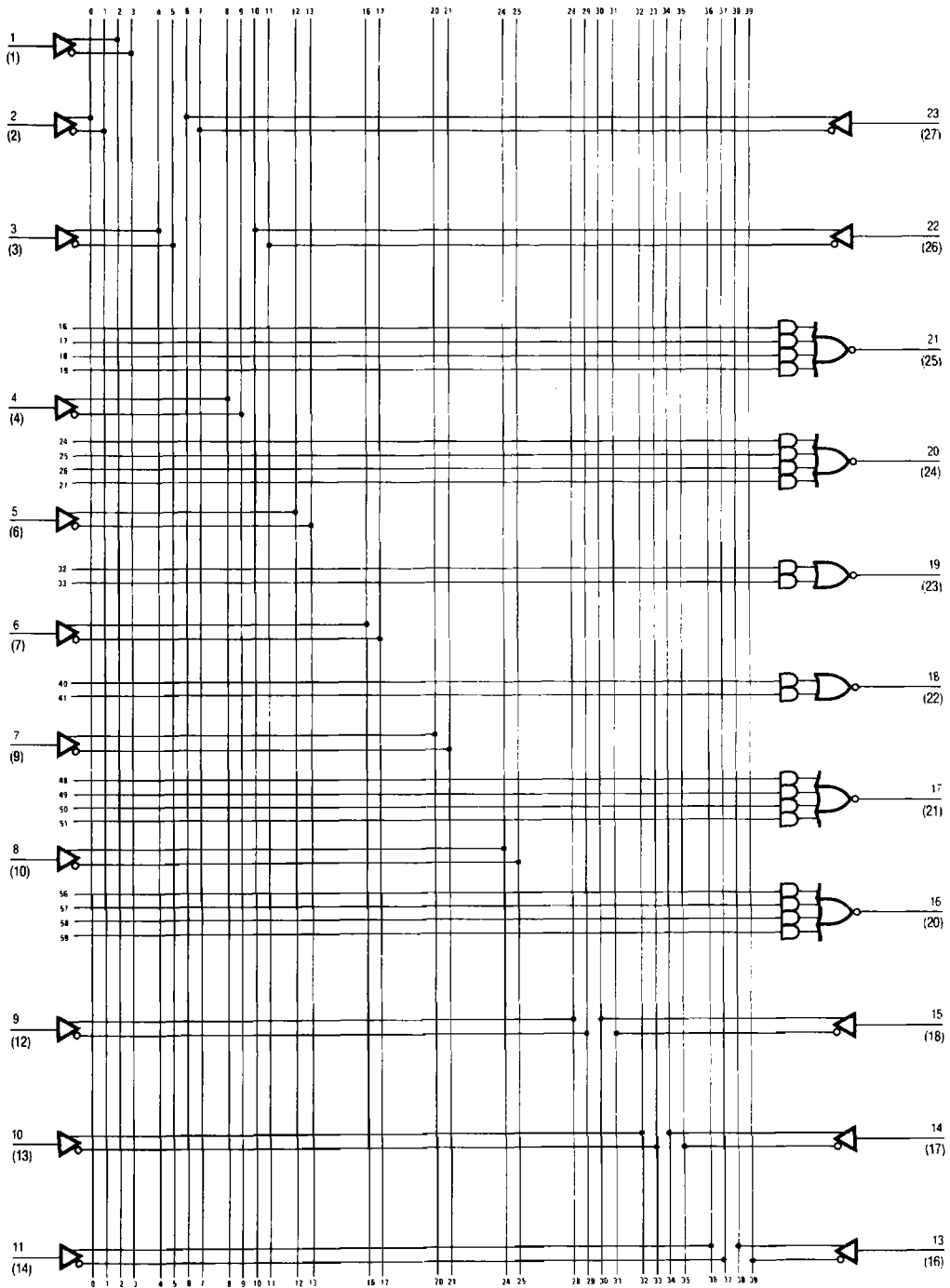
Logic Diagram DIP (PLCC) Pinouts 14L8



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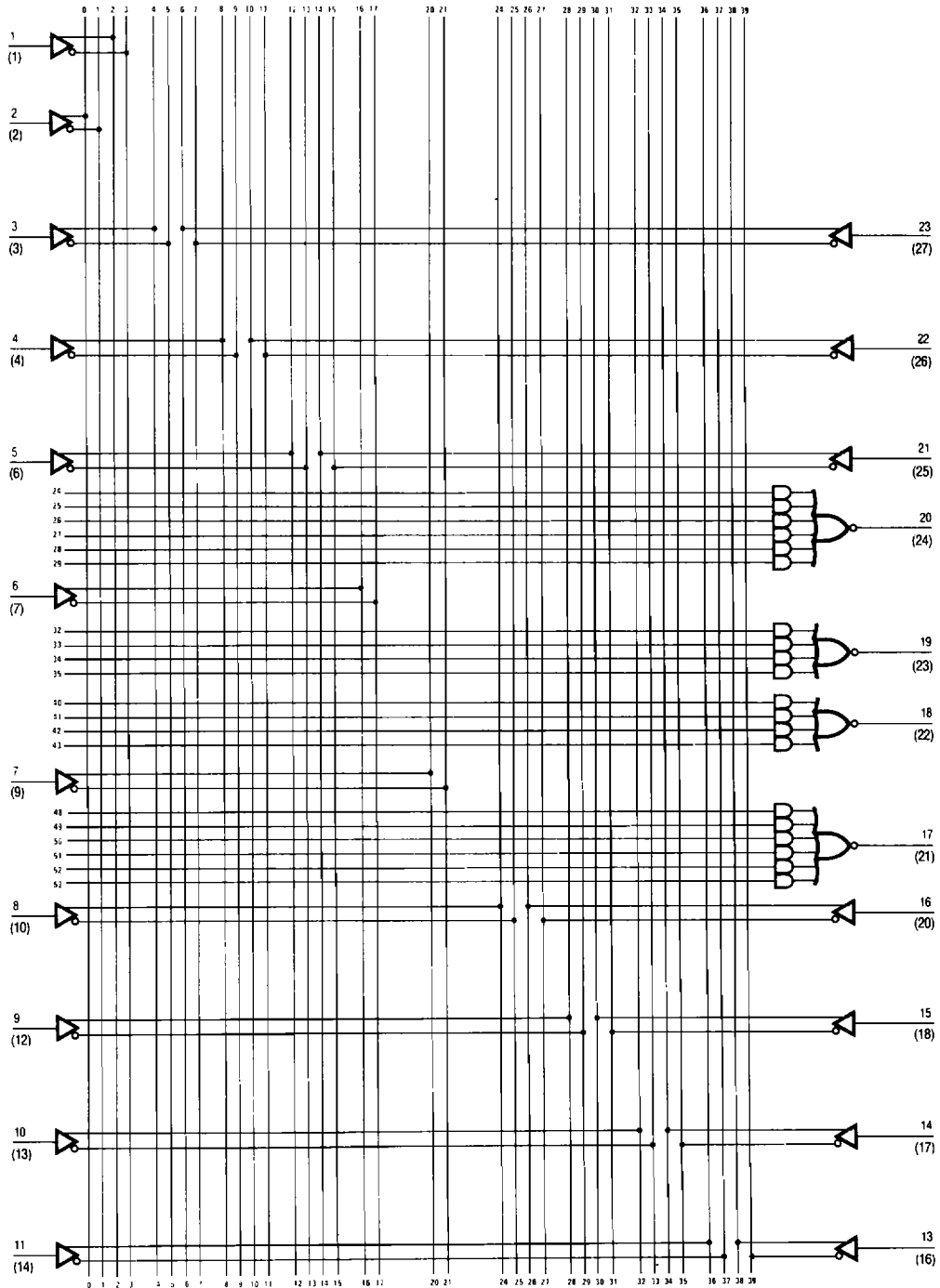
Combinatorial PAL12L10 Series
12L10, 14L8, 16L6, 18L4, 20L2, 20C1

Logic Diagram DIP (PLCC) Pinouts 16L6



Combinatorial PAL12L10 Series
12L10, 14L8, 16L6, 18L4, 20L2, 20C1

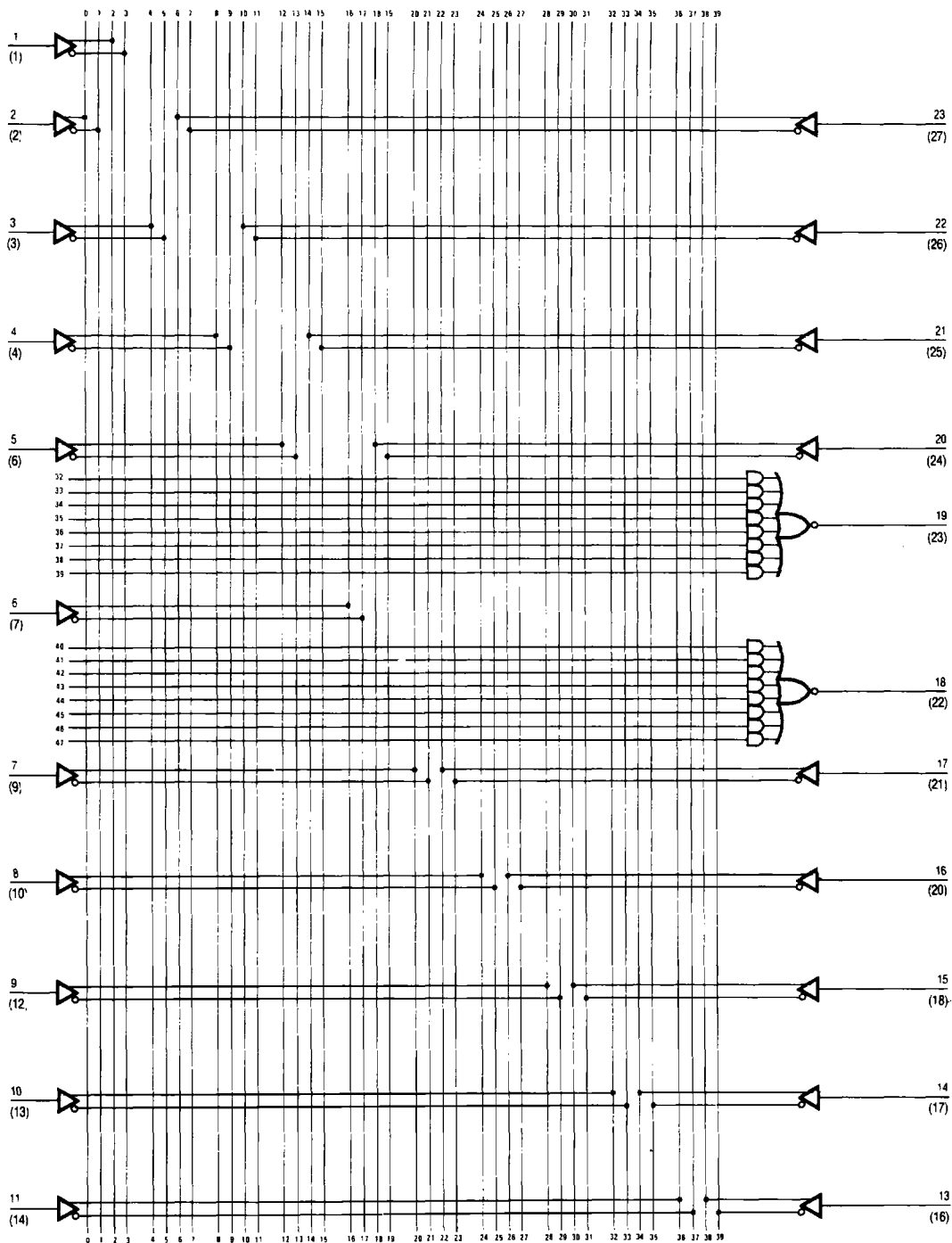
Logic Diagram DIP (PLCC) Pinouts 18L4



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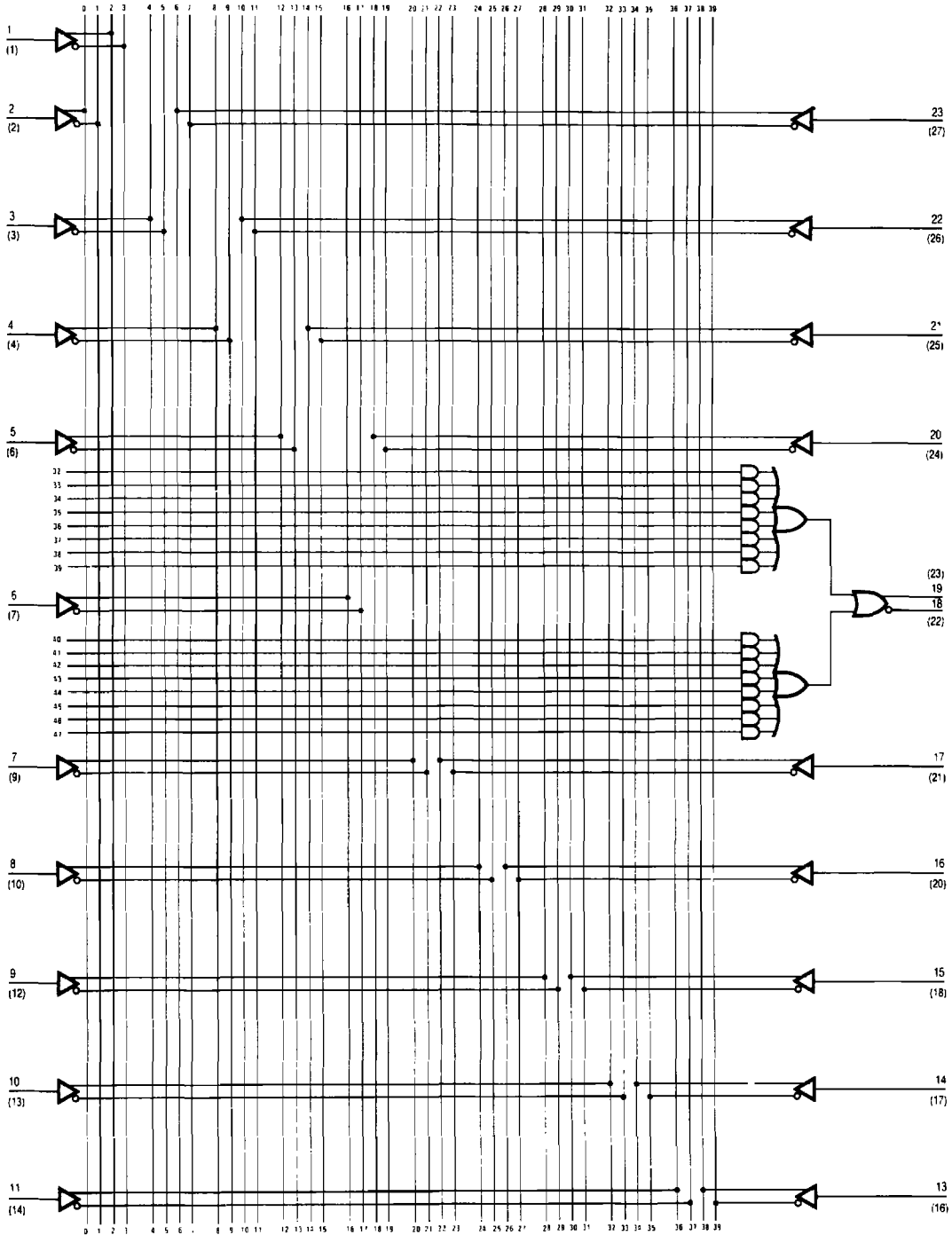
Combinatorial PAL12L10 Series
12L10, 14L8, 16L6, 18L4, 20L2, 20C1

Logic Diagram DIP (PLCC) Pinouts **20L2**



**Combinatorial PAL12L10 Series
12L10, 14L8, 16L6, 18L4, 20L2, 20C1**

Logic Diagram DIP (PLCC) Pinouts 20C1



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