SP8908 (MP)



5GHZ ÷ 8 Fixed Modulus Divider

Preliminary Information

The SP8908 is one of a range of very high speed low power prescalers for professional applications. The dividing elements are static D type flip flops and therefore allow operation down to DC if the drive signal is a pulse waveform with fast risetime. The output stage has a differential current output and provides a direct drive into a 50 ohm load.

Ordering Information SP8908/KG/MP1S (tubes) SP8908/KG/MP1T (tape and reel)

Features

- · Very High Operating Speed
- Operation down to DC with Square Wave Input
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 1KHz)
- 5V Single Supply Operation
- Low Power Dissipation: 360mW (Typ.)
- · Surface Mount Plastic Package

Absolute Maximum Ratings

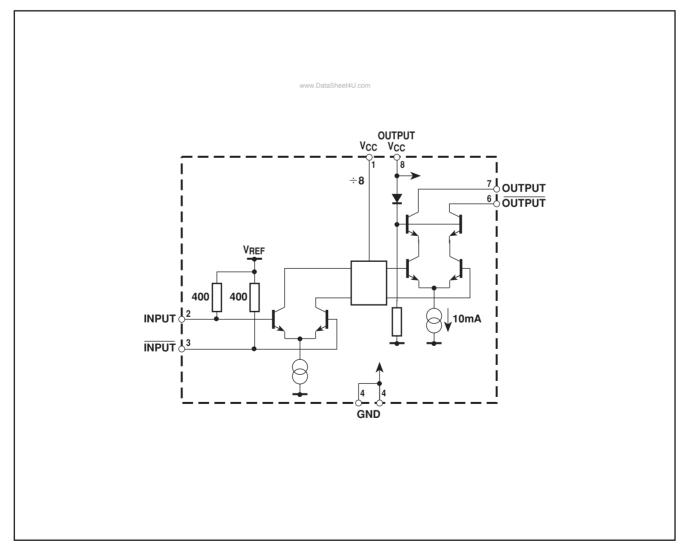


Figure 1 - Block Diagram

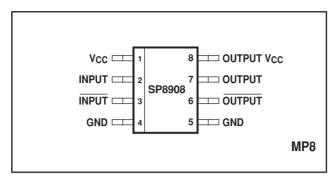


Figure 2 - Pin connections - top view

Electrical Characteristics

These characteristics are guaranteed by either production test or design over the following range of operating conditions unless otherwise stated: $T_{AMB} = -40$ °C to +85 °C, $V_{CC} = 4.75$ V to 5.25V

| | Pin | Value | | | | | |
|-------------------|------|-------|------|------|-------|---------------------------------------|--|
| Characteristic | | Min. | Тур. | Max. | Units | Conditions | |
| Supply current | 1, 8 | - | 72 | 96 | mA | | |
| Input frequency | 2, 3 | 1.0 | - | 5∙0 | GHz | RMS sinewave | |
| Input sensitivity | 2, 3 | - | - | 180 | mVrms | f _{IN} = 1GHz and 4.2GHz | |
| Input sensitivity | 2, 3 | - | - | 570 | mVrms | f _{IN} = 5GHz | |
| Input overload | 2, 3 | 440 | - | - | mVrms | f _{IN} = 1GHz and 3GHz | |
| Input overload | 2, 3 | 700 | - | - | mVrms | $f_{IN} = 5.0GHz$ and $3.8GHz$ | |
| Output voltage | 6, 7 | - | 0.5 | - | Vp-р | Into 50Ω pullup resistor | |
| Output power | 6, 7 | -10∙0 | 0 | +2.0 | dBm | $f_{IN} = 1GHz$ and 5GHz (see note 1) | |

NOTE

1. Measured into 50Ω measuring instrument in parallel with 50Ω pullup resistor. See Figure 5.

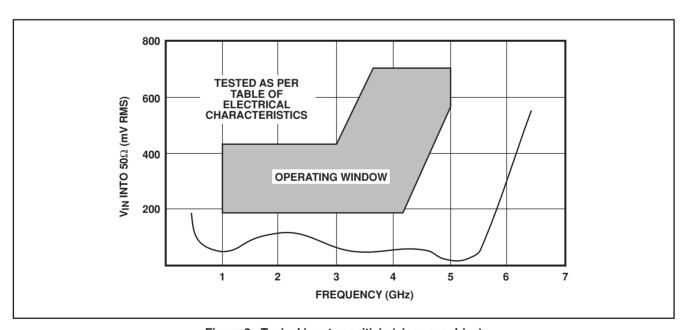


Figure 3 - Typical input sensitiviy (sinewave drive)

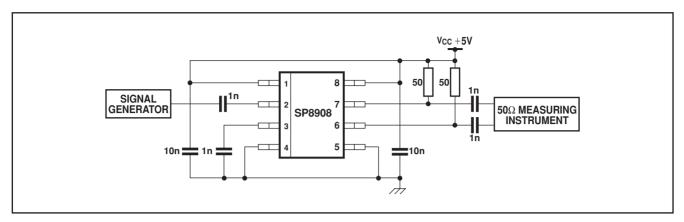


Figure 4 - Typical application and test circuit

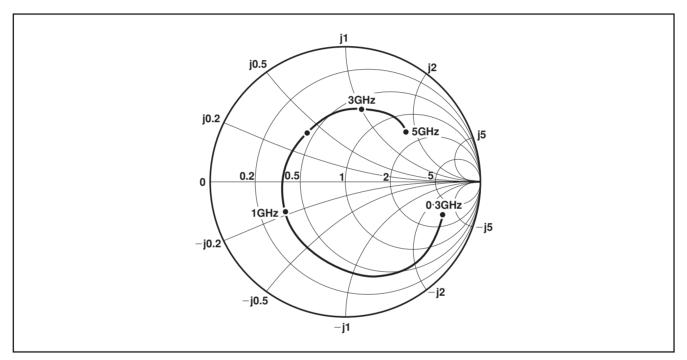


Figure 5 - Typical input impedance

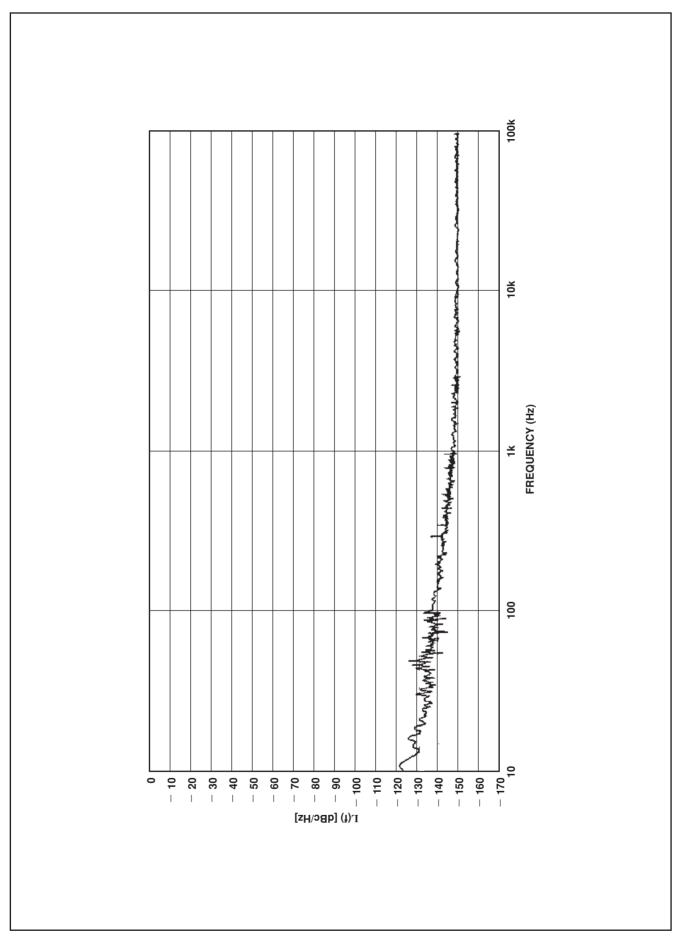
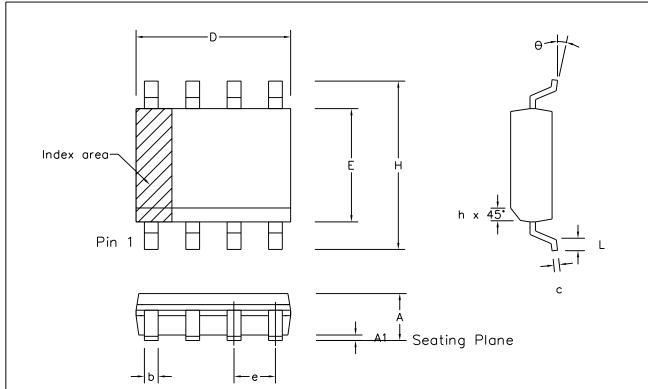


Figure 6 - Typical phase noise, input frequency = 3GHz



| | Min | Max | Min | Max | | |
|-----------------------------------|--------------|------------|-----------|-------|--|--|
| | mm | mm | inch | inch | | |
| Α | 1.35 | 1.75 | 0.053 | 0.069 | | |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 | | |
| D | 4.80 | 5.00 | 0.189 | 0.197 | | |
| Н | 5.80 | 6.20 | 0.228 | 0.244 | | |
| E | 3.80 | 4.00 | 0.150 | 0.157 | | |
| L | 0.40 | 1.27 | 0.016 | 0.050 | | |
| е | 1.27 | BSC | 0.050 BSC | | | |
| b | 0.33 | 0.51 | 0.013 | 0.020 | | |
| С | 0.19 | 0.25 | 0.008 | 0.010 | | |
| 0 | O° | 8 ° | 0° | 8° | | |
| h | 0.25 | 0.50 | 0.010 | 0.020 | | |
| | Pin Features | | | | | |
| N | 3 | 3 | 8 | | | |
| Conforms to JEDEC MS-012AA Iss. C | | | | | | |

Notes:

- 1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross—hatched area.
- 2. Controlling dimensions are in inches.
- 3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
- 4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
- 5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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|---|--------|---------|---------|--------|---------|-----------------------|------------------------|------------------------------------|
| ISSUE | 1 | 2 | 3 | 4 | 5 | | Previous package codes | Package Outline for |
| ACN | 6745 | 201936 | 202595 | 203705 | 212424 | ZARLINK SEMICONDUCTOR | | 8 lead SOIC (0.150" Body width) |
| DATE | 5Apr95 | 27Feb97 | 12Jun97 | 9Dec97 | 22Mar02 | | , | , |
| APPRD. | | | | | | | | GPD00010 |



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